A 5-GHz CMOS Wireless LAN Receiver Front End

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***Abstract*—This paper presents a 12.4-mW front end for a 5-GHz wireless LAN receiver fabricated in a 0.24-μm CMOS technology. It consists of a low-noise amplifier (LNA), mixers, and an automatically tuned third-order filter controlled by a low-power phase-locked loop. The filter attenuates the image signal by an additional 12 dB beyond what can be achieved by an image-reject architecture. The filter also reduces the noise contribution of the cascode devices in the LNA core. The LNA/filter combination has a noise figure of 4.8 dB, and the overall noise figure of the signal path is 5.2 dB. The overall IIP3 is −2 dBm.**

***Index Terms*—Automatic tuning, CMOS analog integrated circuits, high-frequency filters, HIPERLAN, image-reject circuits, low-noise amplifier (LNA), notch filter, receiver front end.**

I. Introduction

THE GROWING popularity of notebook computers demands high data-rate wireless LAN systems. Many existing wireless LAN systems operate in the 2.4-GHz ISM band. These products currently achieve maximum data rates of 1–2 Mbits/s. The need for higher data-rate wireless LAN products prompted the Federal Communications Commission (FCC) to release 300 MHz of spectrum for the unlicensed national information infrastructure (U-NII)[1]. Using this newly released frequency band, wireless LAN systems can provide data rates of several tens of megabits per second. The allocated frequencies overlap the European standard for the high-performance radio LAN (HIPERLAN) frequency band as shown in Fig. 1(a).

The superheterodyne architecture is the most widely used architecture for wireless receivers. Monolithic image cancellation has always been a challenge due to the design problems of on-chip filters. The use of image-reject architectures alleviates this problem to some extent. Typically, these architectures can practically achieve 30–40 dB of image cancellation [2], [3].

This paper describes the design and implementation of a 12.4-mW CMOS front-end receiver for a 5-GHz wireless LAN system. The receiver uses a tunable third-order filter, which is automatically tuned by an image-reject phase-lock loop (PLL), to alter the transfer function of the low-noise amplifier (LNA). The LNA/filter combination provides an additional 12 dB of image rejection beyond what can be achieved by an image-reject architecture.

II. Receiver Architecture

Wireless LAN systems require receiver architectures with wide dynamic range. When a transmitter and receiver are close to each other, the received signal strength can be as high as −20 dBm. A highly linear receiver is needed to accommodate such strong signals. On the other hand, the received signal can be quite weak due to fading. The receiver must be sensitive enough to detect signals as small as −148 dBm/Hz. (i.e., −74 dBm for a 24-MHz bandwidth signal [7]). To have a predetection signal-to-noise ratio (SNR) of at least 12 dB, the overall noise figure of the receiver must be better than

$$NF = -148\ \text{dBm/Hz} - 12\ \text{dB} - (-174\ \text{dBm/Hz}) = 14\ \text{dB}$$

where −174 dBm/Hz is the available noise power of the source. This noise figure is readily achievable in CMOS with a reasonably low power consumption.

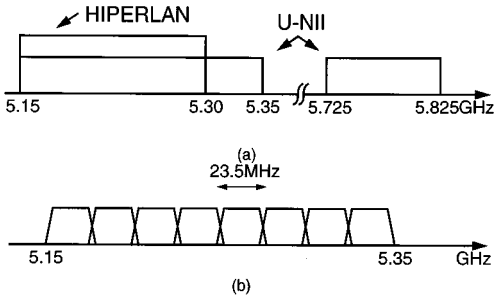

Fig. 1. (a) U-NII and HIPERLAN frequency bands (b) proposed channel allocation.

The receiver uses the channel allocation depicted in Fig. 1(b) where the lower 200 MHz of the U-NII band is divided into eight channels, each 23.5 MHz wide. This choice of channel spacing is fully compatible with the HIPERLAN standard.

Fig. 2 shows the block diagram of the receive path. The system uses two sets of local oscillators (LO's) to implement an image reject architecture commonly known as the Weaver architecture. The LNA is followed by a first set of mixers to produce the I and Q components of the intermediate-frequency (IF) signal. A tunable third-order filter alters the transfer characteristic of the LNA to achieve further attenuation of the image signal. A PLL automatically tunes the image-reject band of the filter to the image frequency [4]–[6].

It is important to mention that the circuit implementations of the voltage-controlled oscillator (VCO) and the filter are exactly the same. Because of this similarity, the locations of the pole and zero of the filter are closely related to the oscillation frequency of the VCO. The VCO and the filter share the same control voltage, and since they are topologically identical, locking the VCO frequency to the frequency of the image signal tunes the notch frequency of the filter to the image frequency.

A passive mixer downconverts the VCO output by mixing it with the first LO. A phase/frequency detector (PFD) compares the downconverted signal against the second LO. A charge-pump circuit and loop filter complete the PLL. The lock

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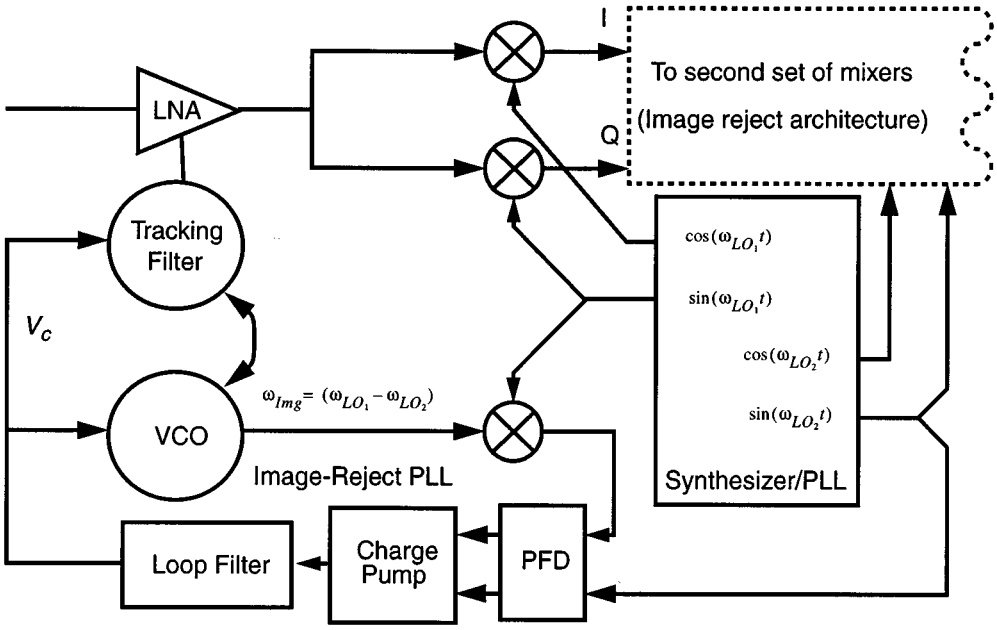

Fig. 2. Block diagram of the receive path.

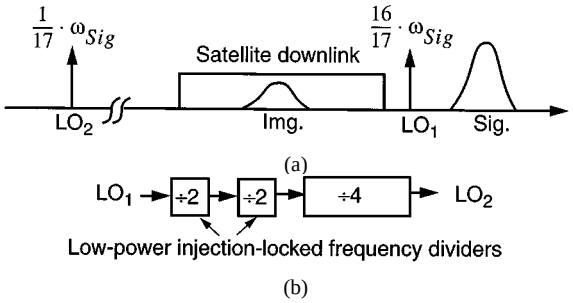

Fig. 3. (a) Frequency planning and (b) ease of implementation of the second LO.

TABLE I
MEASURED SIGNAL-PATH PERFORMANCE

LNA performance	
Noise figure	4.8dB
Voltage gain	18dB
S_{11}	-12dB
Image-rejection (filter only)	12dB
Receive path (LNA+mixers) performance	
Total noise figure	5.2dB
Total voltage gain	12dB
Input-referred IP3	-2dBm
1-dB compression point	-14dBm
Power dissipation	
LNA	7.2mW
Image-reject filter	1.0mW
Image-reject PLL/VCO	3.2mW
Bias circuitry	1.0mW
Total power @ 2V	12.4mW
Implementation	
Die area	1mm^2
Technology	0.24-µm CMOS

condition is reached when the downconverted VCO output has the same frequency as that of the second LO. That is, the PLL locks when the VCO output is tuned to the image frequency.

This particular PLL structure eliminates the need for frequency dividers in the loop by using the pregenerated LO signals. Since there are no power-hungry dividers in this structure, the image-reject PLL consumes little power (Table I).

An on-chip synthesizer generates the two sets of LO frequencies, LO_1 and LO_2, with a PLL. The synthesizer architecture is beyond the scope of this paper but is described in a companion article [8]. The radio-frequency (RF) input lies in the 5.15–5.35-GHz frequency band. The frequency of the first LO is 16/17 of the RF input, and the frequency of the second LO is 1/17 of the RF input, as shown in Fig. 3(a). Because of these choices of the LO signals, the image signal lies within the downlink frequency spectrum of a satellite system and is relatively weak. It is also fairly easy to obtain the second LO from the first LO using low-power injection-locked frequency dividers, shown in Fig. 3(b) [9]. The frequency of the second LO is chosen to be fairly low (around 300 MHz) to alleviate some well-known problems of the direct conversion receivers such as self-mixing and dc offset. A low-frequency second LO would also mean that the second set of mixers (in the Weaver architecture) can be built using large devices, which would reduce the undesirable effects of flicker noise.

A very well-known LNA topology uses a cascode structure with inductive degeneration. It is possible to modify the transfer function of this LNA by an *LC* tank circuit, as shown in Fig. 4(a) [10]. The *LC* circuit has a low impedance at the frequency of the image signal, i.e., the series resonant frequency of the *LC* circuit is the same as the frequency of the image. The resulting transfer function is depicted in Fig. 4(b). At the frequency of the image signal, the *LC* circuit steals the current away from M_3, thus reducing the gain at that frequency. Although this circuit can help to achieve further filtering of the image signal, the noise figure is degraded due to the finite impedance of the *LC* circuit at the signal frequency.

As shown in Fig. 5(a), the noise performance of the cascode structure is further degraded by the parasitic capacitance at node X. This parasitic capacitance C_x lowers the impedance

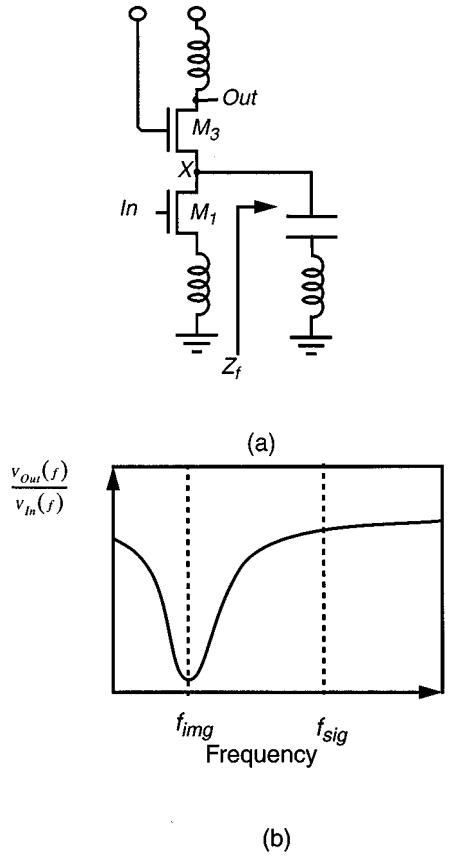

Fig. 4. (a) Image-reject LNA and (b) transfer function of the image-reject LNA.

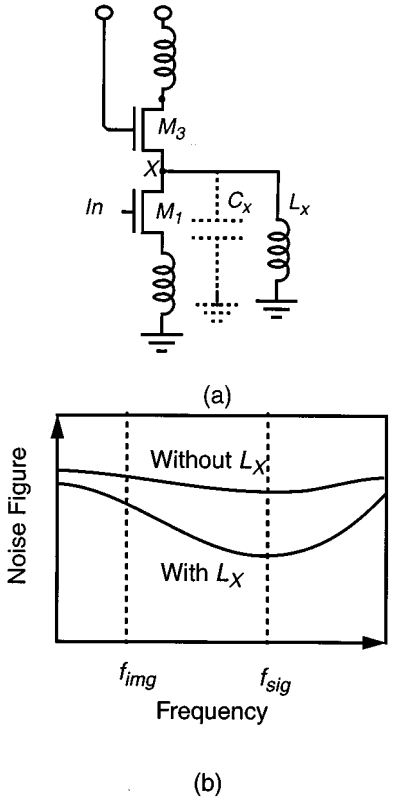

Fig. 5. (a) Improving the noise figure of a standard LNA and (b) noise figure versus frequency.

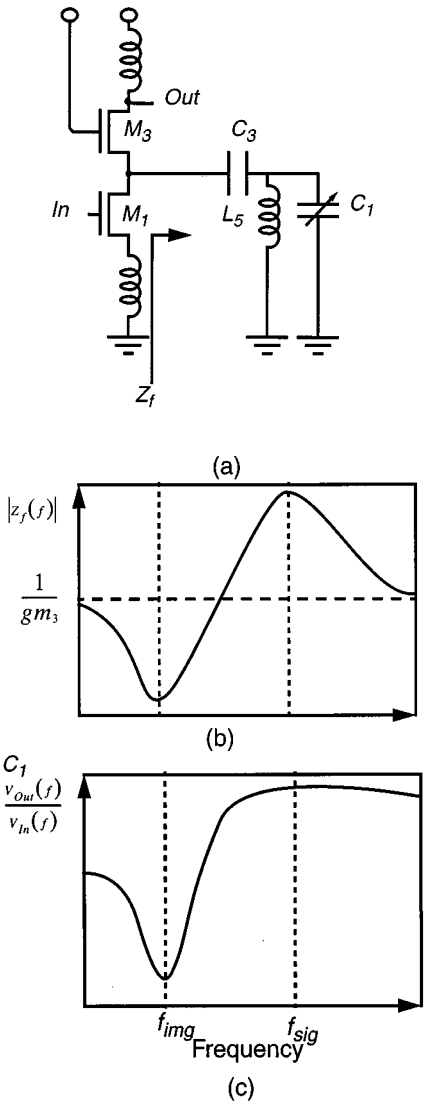

Fig. 6. (a) Circuit diagram of the LNA with a third-order filter, (b) input impedance of the filter versus frequency, and (c) the transfer function of the LNA/filter combination.

at node X and reduces the gain of the cascode structure. The presence of this parasitic capacitance makes the noise contribution of M_3 more pronounced (see the Appendix.) To reduce the noise figure, the effect of this capacitance must be nullified. An inductor placed in parallel with this parasitic capacitance is a remedy to the problem. In Fig. 5(b), noise figure is plotted versus frequency. The noise performance of the LNA is improved with the help of the inductor.

Combining the ideas depicted in Figs. 4(a) and 5(a) would result in the circuit shown in Fig. 6(a). The filter comprises an inductor, a capacitor, and a varactor. The filter has a low impedance at the frequency of the image and a high impedance at the frequency of the signal. The input impedance of the filter Z_f can be written as

$$Z_f(s) = \frac{L_5 \cdot (C_3 + C_1)s^2 + 1}{C_1 \cdot C_3 \cdot L_5 \cdot s^3 + C_3 \cdot s}. \quad (1)$$

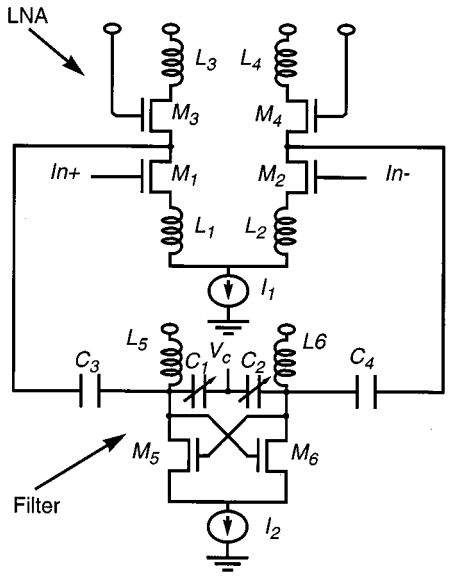

Fig. 7. Simplified circuit diagram of the LNA and filter.

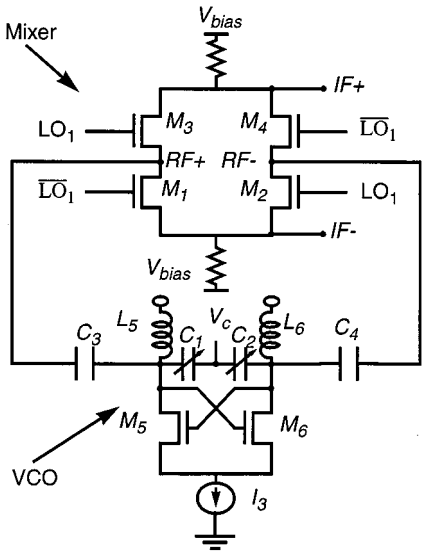

Fig. 8. A simplified circuit diagram of the VCO and PLL mixer.

The filter has imaginary zeros at

$$\omega_z = \pm\frac{1}{\sqrt{L_5 \cdot (C_3 + C_1)}} \tag{2}$$

and imaginary poles at

$$\omega_p = \pm\frac{1}{\sqrt{L_5 \cdot C_1}}. \tag{3}$$

The location of the pole–zero pair on the imaginary axes is controlled by the varactor.

Fig. 6(b) shows the input impedance of the filter $|Zf|$ as a function of the frequency. The resistance looking into the source of the cascode device, gm_3^{-1}, has also been marked on the same graph for comparison. For frequencies close to the location of the zero, the filter has an impedance lower than gm_3^{-1} and steals the ac current away from M_3, thus reducing the LNA gain. At frequencies close to the pole, $|Zf|$ is larger than gm_3^{-1} and the LNA gain is high. The resulting transfer function of the LNA/filter is shown in Fig. 6(c). The transfer function has a narrow valley, so for correct image cancellation, the zero must occur at the correct frequency. On the other hand, the peak is wide-band and the exact location of the pole is less important.

The third-order filter is designed not only to reject the image signal but also to diminish the effect of the parasitic capacitance at node X. Thus, by providing a pole (parallel resonance) as well as a zero (series resonance) the filter achieves image rejection and good noise performance at the same time. Although (1)–(3) need to be modified slightly to include the effect of this parasitic capacitance, the foregoing argument is still valid (see Appendix).

III. Circuit Implementation

A. LNA and Filter

Fig. 7 is a simplified schematic of the LNA and filter. A differential architecture is selected for better rejection of on-chip interference. Also, the differential architecture alleviates the problem of parasitic source degeneration. To achieve the required high linearity, the LNA consists of only one stage, formed by transistors M_1–M_4. Inductive degeneration is employed in the sources of M_1 and M_2 to produce a real term in the LNA's input impedance [11].

Capacitors C_1–C_4 and inductors L_5 and L_6 form a differential version of the filter discussed previously. The voltage V_c controls the location of the pole–zero pair by changing the capacitance of the accumulation mode varactors C_1 and C_2.

The cross-connected differential pair, M_5 and M_6, generates a negative impedance to cancel the losses in the filter, which are mainly due to the finite Q of the inductor. The depth of the notch in Fig. 6(c) depends on this negative impedance. By choosing a correct value for the tail current (I_2 in Fig. 7), one can easily adjust the amount of image rejection without jeopardizing the stability of the filter. The LNA/filter combination becomes unstable when the net negative admittance of the filter (after subtracting the internal losses of the filter itself) becomes comparable to gm_3. Since the LNA core has a much higher bias current than the filter, there is a large margin of safety in this design. According to simulations, in our conservative design, the tail current can be increased by a factor of three before the LNA/filter combination becomes unstable.

The filter also reduces the noise figure of the cascode devices, at the cost of adding some extra noise of its own. However, the bias current of the M_5 and M_6 pair is much lower than that of the cascode devices, M_3 and M_4, so the net effect is an improvement in the noise figure (see Appendix).

B. Image-Reject PLL

Fig. 8 is a simplified circuit diagram of the VCO and mixer used in the PLL loop. The same filter structure is now used as a VCO. The only difference is the increased tail current necessary to sustain oscillation. The mixer consists of four transistors, M_1–M_4. The similarity between the topologies depicted in Figs. 7 and 8 suggests that the oscillation frequency of the VCO is a good measure of the zero location of the filter. A

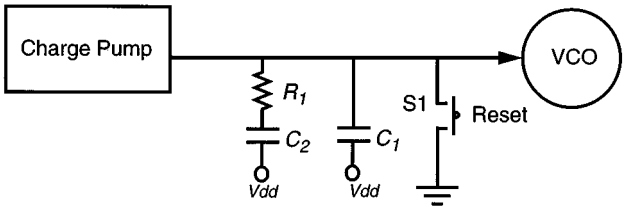

Fig. 9. Loop filter.

PFD, charge pump, and loop filter follow the mixer to complete the loop. Since these three blocks work at the frequency of the second LO, they consume little power (1.1 mW).

The offset PLL topology used for tuning can potentially lock to $\omega_{\mathrm{LO}_1}+\omega_{\mathrm{LO}_2}$ instead of $\omega_{\mathrm{LO}_1}-\omega_{\mathrm{LO}_2}$. Several safety features are imbedded in the design of the PLL to avoid this threat. First, the VCO locking range is limited and $\omega_{\mathrm{LO}_1}+\omega_{\mathrm{LO}_2}$ is outside the locking range of the VCO. In addition, as shown in Fig. 9, a switch is placed at the output of the loop filter to reset the VCO input to zero at the beginning of each channel select cycle. When the switch is released, the VCO input ramps up and the loop can only lock to $\omega_{\mathrm{LO}_1}-\omega_{\mathrm{LO}_2}$. Finally, to avoid overshoot on the control voltage that might otherwise force the PLL to lock to an incorrect frequency, the loop filter is designed such that the PLL is overdamped.

C. Mixers

The output of the LNA is downconverted by the first set of mixers to produce the I and Q components of the IF signal. We chose a passive ring mixer topology for improved linearity. These signal-path mixers are identical to the mixer used in the PLL (Fig. 8). Each mixer consists of four transistors, grouped together into two pairs of transistors. During each half-cycle of the LO signal, the RF port is connected to the IF port with a different polarity, as described in detail in [11].

D. Biasing Circuitry

The biasing of the receiver front end is accomplished on-chip through the use of a rather standard self-biased constant-gm reference [12]. This type of reference generates the right current so that the transconductance gm is proportional to a reference conductance $1/R$. So, the output current of the bias circuit is whatever is necessary for the transconductance to follow $1/R$. Regulating gm reduces the dependence of the LNA gain, the transfer function of the filter, and input matching on supply and temperature variations.

E. Input Matching Circuitry

The differential inputs of the LNA must be coupled to the single-ended output of the antenna. A single-ended to differential coupler (commonly known as a balun) is needed to achieve this task. A simple, yet effective way of designing a good balun at 5-GHz frequency range is to use off-chip microstrip lines. The ring hybrid structure depicted in Fig. 10(a) uses microstrip lines to generate two outputs that are 180° out of phase with respect to each other [13].

The ports A–B, B–C, and C–D are separated by 90°, and ports A and D are three-quarters of the wavelength away from each other. Because of the impedance and phase relationships shown in the structure, power fed to port A splits equally between ports B and D with a 180° phase difference, and port C remains isolated. Note that to maintain matching, the characteristic impedance of the ring is designed to be $\sqrt{2}Z_0$, where Z_0 is the characteristic impedance of each port.

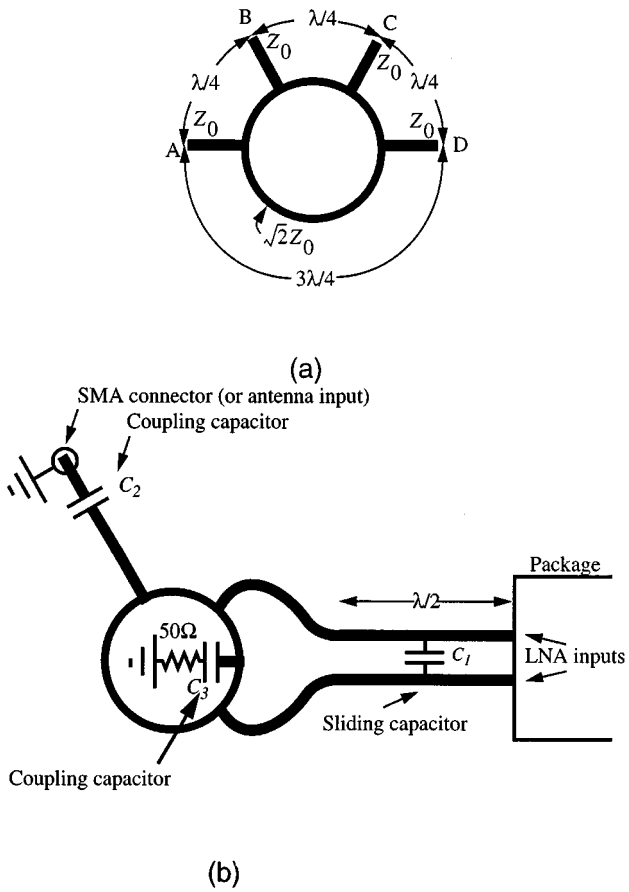

Fig. 10. (a) Ring-hybrid and (b) input matching circuitry.

The off-chip matching circuitry is shown in Fig. 10(b). A sliding capacitor and two parallel transmission-line sections comprise a differential π-match. Matching can simply be done through trial and error. A 50-Ω resistor is used to terminate port C of the hybrid ring balun. The value of the sliding capacitor is determined based on the input impedance of the LNA and parasitic inductance and capacitance of the package and bond wires. In this design, the estimated pin inductance is 3 nH and bond-wire inductance is estimated to be 1 nH/mm.

IV. Measurements

The front-end receiver has been implemented in a 0.24-μm CMOS technology; the die micrograph is shown in Fig. 11. The chip consumes 12.4 mW from a 2-V power supply and occupies 1 mm^2 of die area. It uses eight spiral inductors with patterned ground shields for improved quality factor and reduced crosstalk between spirals [14]. The Q of the inductors are estimated to be about five at the frequency of operation.

The LNA/filter combination has also been laid out as a separate test structure so that it could be characterized independently. As shown in Fig. 12, the differential LNA has a noise figure of

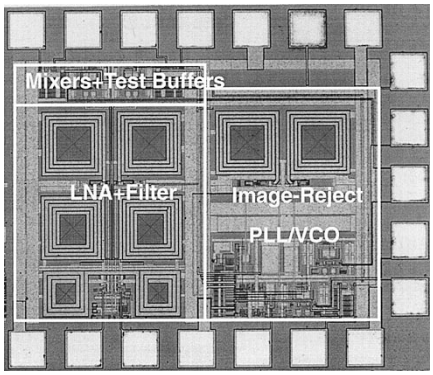

Fig. 11. Die micrograph of the receive path.

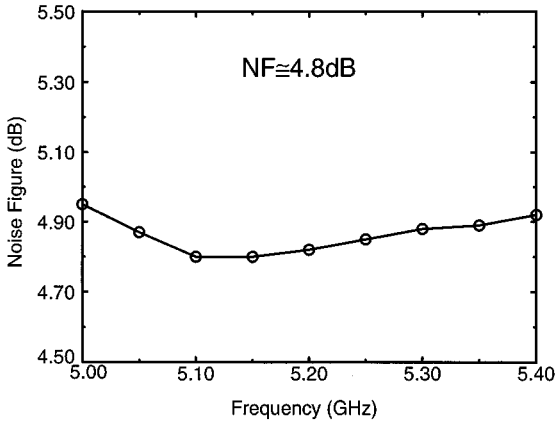

Fig. 12. Measured LNA noise figure.

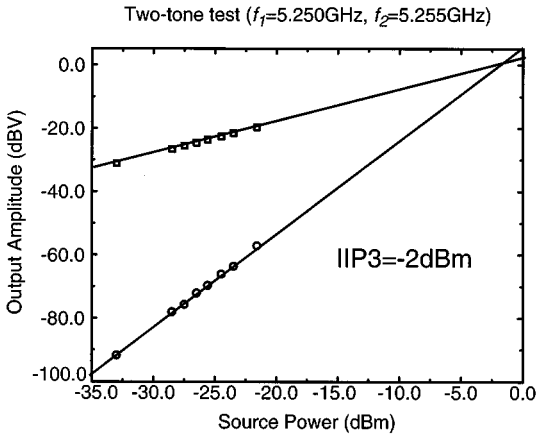

Fig. 13. Two-tone IP3 measurement for the RF front end.

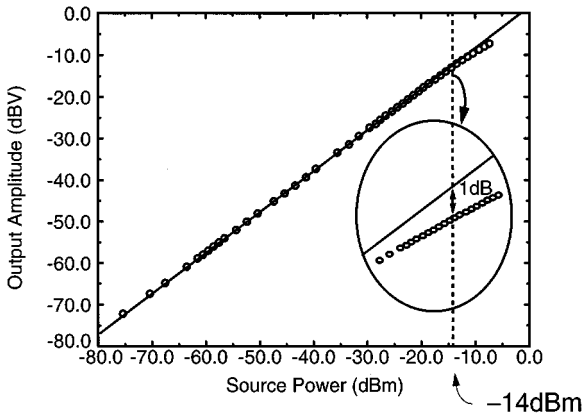

Fig. 14. One-dB compression-point measurement.

4.8 dB and consumes only 7.2 mW of power. For each point in this measurement, the image-reject PLL tunes the filter to the correct frequency.

For measurement purposes, test buffers placed after the two mixers allow characterization of the performance of the signal path. The overall measured noise figure is 5.2 dB. The input capacitance of each buffer is 0.3 pF. The amount of capacitive loading at the output of the mixers when implemented in a full system is lower than this value. Therefore, the test buffers provide more than a practical amount of loading, and the measurement results are realistic. For testing, the LO_1 signal is applied off chip. The amplitude of the LO_1 signal at the LO port of the mixer is 0.9 V-differential (450 mV single-ended). It is noteworthy to mention that passive ring mixers are highly linear but require relatively large LO amplitudes.

The filter consumes 1 mW of power, and the amount of image-rejection boost is 12 dB. The bandwidth of the image-reject notch is 200 MHz. As discussed before, in a more aggressive design, it is possible to increase the amount of rejection even further by increasing the power consumption of the filter. The image-reject PLL consumes 3.2 mW of power, of which 2.1 mW is burned by the VCO. The mismatch between the notch frequency of the filter and the VCO frequency is measured to be 0.9%, which is quite adequate for this application.

Fig. 13 shows the results of a two-tone third-order intercept point (IP3) measurement performed on the signal path. Two in-band signals are applied to the system at 5.250 and 5.255 GHz. The measured input-referred IP3 is -2 dBm. The measured input-referred 1-dB compression point of the receiver is -14 dBm (Fig. 14). The performance of the system is summarized in Table I.

The blocking performance of a receiver is determined by various factors, including its linearity, the phase noise of the VCO, and the spurious frequencies generated by the synthesizer. In this design, a synthesizer spur that falls in the adjacent channel band is the limiting blocking mechanism [8]. The spur is at -54 dBc. An undesired adjacent channel that is 44 dB stronger than the desired signal is tolerated for a signal-to-interference ratio of 10 dB.

V. Conclusions

A low-power and highly linear CMOS front-end receiver for a 5-GHz wireless LAN system has been presented. A third-order filter alters the transfer function of the LNA to reject the image signal and to decrease the noise contribution of the cascode devices in the LNA core. A PLL structure automatically tunes the filter to the correct frequency.

Appendix
Noise Considerations

A simple noise analysis of the circuit shown in Fig. 15(a) quantifies the effects of parasitic capacitance C_x. An equivalent circuit for noise calculation at the resonance frequency ω_0, is

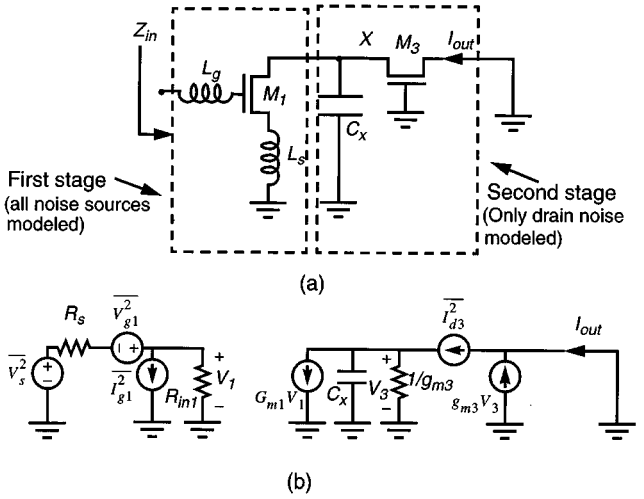

Fig. 15. (a) Standard LNA topology and (b) equivalent circuit for noise calculations.

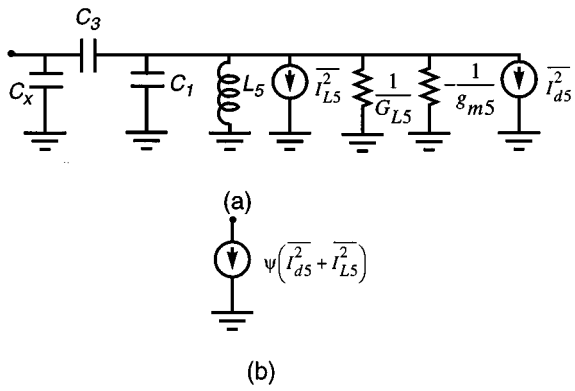

Fig. 16. (a) Filter noise model and (b) simplified filter noise model at the frequency of the pole.

depicted in Fig. 15(b). All parasitic capacitances of node X, as well as junction capacitors and the gate–source capacitance of M_3, are absorbed into C_x.

At the resonant frequency of the input circuit, the impedance is purely real and is calculated to be

$$R_{\text{in1}} = \frac{gm_1}{C_{\text{gs1}}} \cdot Ls. \tag{4}$$

In Fig. 15(b), all the noise sources of the first stage are modeled through equivalent input-referred voltage and current noise sources, but only the drain noise of the second stage is modeled. Including all other noise sources of the second stage only complicates the derivations while adding little accuracy to the derived formulas. The equivalent transconductance of the first stage when the input is matched is

$$G_m \approx \frac{\omega_T}{\omega_0 R_s} \tag{5}$$

where $\omega_T = g_{m1}/C_{\text{gs1}}$, ω_0 is the input resonant frequency and R_s is the source impedance.

The drain noise current of the second stage is

$$\frac{\overline{I_{d3}^2}}{\Delta f} = 4kT\gamma_3 g_{\text{do3}} \tag{6}$$

where g_{do3} is the zero-bias drain conductance of the device and γ_3 is a bias-dependent factor. The noise factor of the first stage F_1 is

$$F_1 = 1 + \frac{1}{4kTR_s}\overline{V_{g1}^2} + \frac{R_s^2}{4kTR_s}\overline{I_{g1}^2}. \tag{7}$$

Calculating the total noise figure of the circuit and simplifying the result using (7), one obtains

$$F_{\text{no-filter}} = F_1 + 4R_s\gamma_3 g_{do3}\left(\frac{\omega_0^2}{\omega_T^2}\right)\left(\frac{C_x^2}{g_{m3}^2}\omega_0^2\right). \tag{8}$$

Equation (8) shows that capacitance C_x has a big impact on the noise figure at high frequencies. The effect of this capacitance can be nullified by an inductor. With the help of a parallel inductor that resonates with C_x at the frequency of interest, the noise factor reduces to that of the first stage. That is, the noise contribution of M_3 is negligible when C_x is effectively removed.

To derive the noise contribution of the filter, (1)–(3) must be modified to include the effect of C_x. A more accurate expression for the input impedance of the filter Z_f can be written as

$$Z_f(s) = \frac{L_5 \cdot (C_3 + C_1) \cdot s^2 + 1}{(C_1C_3 + C_1C_x + C_3C_x) \cdot L_5 \cdot s^3 + (C_3 + C_x) \cdot s} \tag{9}$$

whose imaginary poles are located at

$$\omega_p = \pm\frac{1}{\sqrt{L_5\left(C_1 + \dfrac{C_3C_x}{C_3 + C_x}\right)}}. \tag{10}$$

Fig. 16(a) shows a simplified model for the filter noise. Drain noise of M_5 (Fig. 6) has a form similar to (6) and is expressed as

$$\frac{\overline{I_{d5}^2}}{\Delta f} = 4kT\gamma_5 g_{\text{do5}}. \tag{11}$$

The noise contribution of the inductor is

$$\frac{\overline{I_{L5}^2}}{\Delta f} = 4kTG_{L5} \tag{12}$$

where $G_{L5} = Q_{L5}L_5\omega_0$. Since the Q of the varactor is assumed to be larger than the finite Q of the inductor [16], inductor noise is dominant.

Assuming that the filter is tuned correctly, $\omega_0 = \omega_p$, and using (10), the noise model (Norton equivalent) of the filter is simplified as shown in Fig. 16(b), where

$$\psi = \frac{C_3^2 \cdot \omega_0^2}{\left(\dfrac{C_3^2}{C_x + C_3}\right)^2 \cdot \omega_0^2 + (G_{L5} - g_{m5})^2}. \tag{13}$$

Note that the impedance of the filter at the frequency of the pole is high enough [compared to gm_3^{-1} in Fig. 15(b)] and the equivalent Norton impedance is ignored. The overall noise figure of the LNA/filter combination is

$$F_{\text{tot}} = F_1 + \psi \cdot 4R_s(\gamma_5 g_{\text{do5}} + G_{L5})\left(\frac{\omega_0^2}{\omega_T^2}\right). \tag{14}$$

The measured noise figure of the LNA with the filter is 4.8 dB, whereas the measured noise figure of the LNA without the filter is 5.5 dB. The filter therefore not only performs image rejection but also improves the noise figure by 0.7 dB. To obtain an expression for F_1, please refer to [15].

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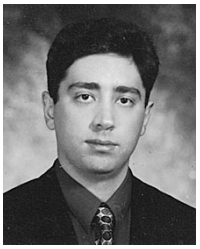

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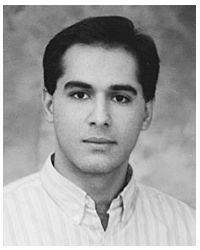

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