A 5-GHz Direct-Conversion CMOS Transceiver

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***Abstract*—A CMOS transceiver fully compliant with IEEE 802.11a in the unlicensed national information infrastructure (UNII) band (5.15–5.35 GHz) achieves a receiver sensitivity of −5 dBm for 64-QAM (quadrature amplitude modulation) with an error vector magnitude (EVM) of −29.3 dB. A single-sideband mixing technique for local-oscillator signal generation avoids frequency pulling. Realized in 0.18-μm CMOS and operating from 1.8-V power supply, the design consumes 171 mW in receive mode and 135 mW in transmit mode while occupying less than 13 mm^2.**

***Index Terms*—CMOS transceiver, IEEE 802.11a, orthogonal frequency division multiplexing (OFDM), wireless local-area network (WLAN).**

I. Introduction

Wireless local-area network (WLAN) is a fast growing market driven by the insatiable demand for high-speed wireless connectivity and increasing availability of cost-effective standards-based interoperable products. WLAN applications include: 1) the extension of the wired Ethernet to wireless mobile devices in the enterprise; 2) the seamless connectivity of networks inside the home for broadband internet sharing; and 3) the increasing deployment of wireless accesses in the public areas such as airports and hotels. Furthermore, the core technology also has applications in the fixed wireless space enabling cost-effective wireless broad-band network between buildings and into the homes. With the Federal Communications Commission (FCC) allocation of 300-MHz bandwidth in the 5-GHz frequency band for the unlicensed national information infrastructure (UNII), high-data-rate (up to 54 Mb/s) WLANs become increasingly popular and important for mobile connectivity. To meet the projected high demand of such WLAN products, the integrated CMOS transceiver is highly desirable for its low cost and high volume manufacturability [1], [2].

The IEEE 802.11a standard [3] incorporates orthogonal frequency division multiplexing (OFDM) modulation, a technique that uses multiple carriers to mitigate the effect of multipath. IEEE 802.11a standard provides for OFDM with 52 subcarriers in a 16.6-MHz bandwidth (channel spacing of 20 MHz); 48 subcarriers are for data, the rest are for pilot signals. Information data rates of 6–54 Mb/s are supported. The 802.11a standard requires a data-rate-dependent minimum receive sensitivity at −65 dBm for 54 Mb/s and −82 dBm for 6 Mb/s. The standard further requires a maximum transmit constellation error at −25 dB for 64-QAM modulated OFDM signal, whereas the output power cannot exceed 16 dBm for channels from 5.15 to 5.25 GHz or 23 dBm for channels from 5.25 to 5.35 GHz.

This paper describes a CMOS direct-conversion transceiver designed for IEEE 802.11a standard for the UNII band from 5.15 to 5.35 GHz. Fabricated in a 0.18-μm CMOS process and operating from a power supply of 1.8 V, the design consumes low power (171 mW in the receive mode, 138 mW in the transmit mode) and occupies a small die area (13 mm^2).

II. Transceiver Architecture

We first made the observation that the superheterodyne architecture requires off-chip surface acoustic wave (SAW) filters and is not a preferred solution. Between direct conversion and low intermediate-frequency (IF) conversion, we realized that direct conversion suffers impairments of flicker noise, dc offset, even-order distortion, local-oscillator (LO) pulling and LO leakage, while low-IF conversion is less susceptible to flicker noise and dc offset. However, low-IF conversion does also suffer impairments of even-order distortion, LO pulling, and LO leakage. Additionally, low-IF conversion requires stringent image rejection as an adjacent channel becomes its image, whereas direct conversion is often referred to as "no image." Furthermore, the signal bandwidth in low-IF conversion is twice that in direct conversion, therefore requires doubling the analog-to-digital converter (ADC) sampling rate, and results in higher power consumption. Finally, the double signal bandwidth in low-IF conversion mandates to double the baseband filter bandwidth, which further increases design complexity and power consumption.

Direct-conversion architecture is therefore chosen, as indicated in Fig. 1. Integrated on a single chip, the transceiver contains a direct-conversion receiver, where the received radio frequency (RF) signal is first amplified by a single-ended low-noise amplifier (LNA), then directly downconverted to baseband signals through a pair of mixers. The baseband section consists of an automatic gain control (AGC) stage and a channel selection low-pass filter (LPF).

The transceiver further contains a direct-conversion transmitter, where the baseband signal from the digital-to-analog converter (DAC), which is on a companion baseband chip, is low-pass filtered and upconverted to RF through a single-sideband doubly balanced mixer. Differential-to-single-ended

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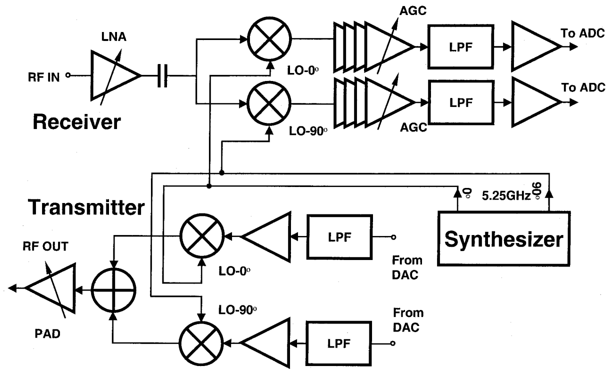

Fig. 1. Transceiver architecture.

(D/S) conversion is performed on chip, so that users do not have to design an off-chip balun. Programmable output power is achieved with the power amplifier driver design.

III. Frequency Planning

Ref. [6] reported an LO generation scheme that consists of voltage-controlled oscillator (VCO) operating at two-thirds of the LO frequency and a divide-by-2 circuit producing quadrature outputs at one-third LO frequency. Two mixers subsequently mixing the VCO signal and the divide-by-2 signal generate both in-phase and quadrature LO signals. As the VCO operates at two-thirds of the LO frequency, this scheme can effectively avoid pulling and reduce LO–RF interaction. However, the generated LO signal has strong sideband at one-third of LO frequency (Fig. 2). In our case, this is roughly 1.8 GHz, a highly populated frequency band where high-power transmitters exist. This technique, therefore, generates an image problem in receive mode and degrades efficiency in transmit mode. This also makes it more challenging to meet the FCC spurious emission requirements.

In this work, we used a quadrature VCO based on crosscoupled *LC* resonators to generate both in-phase and quadrature signals at two-thirds of LO frequency. We further used single-sideband mixers in LO generation, which suppressed the unwanted sideband around 1.8 GHz (Fig. 3). The generated LO signal thus has a cleaner frequency content at the LO frequency, minimizing the adverse effect of the unwanted sideband.

IV. Circuit Design

A. Receiver

In the receiver chain (Fig. 4), a single-ended LNA employs a cascode topology [7] with inductive load (9-nH stacked spiral inductor [8]), achieving a voltage gain of 32 dB. It can be programmed to low-gain mode (12 dB) by lowering the gate bias voltage of the cascode device. Direct downconversion is performed by the voltage-to-current (V/I) converter and mixer stage. A notch filter provides partial channel selection filtering to relax the linearity requirement of the baseband stages. The baseband section consists of an AGC stage and a channel selection LPF, which is designed to have a seventh-order Chebyshev response with a nominal cutoff frequency of 8.7 MHz and a stop-band attenuation of 60 dB.

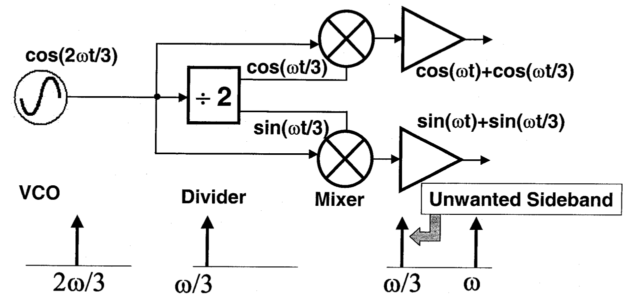

Fig. 2. Example of frequency planning [6].

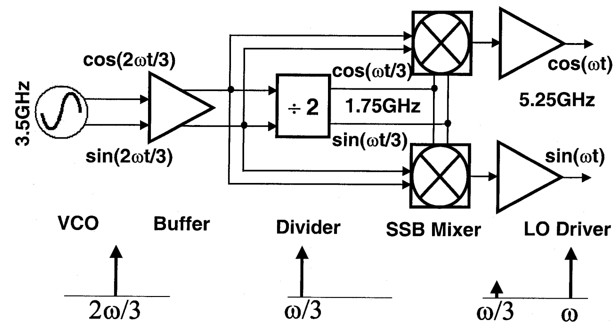

Fig. 3. Frequency planning proposed in this work.

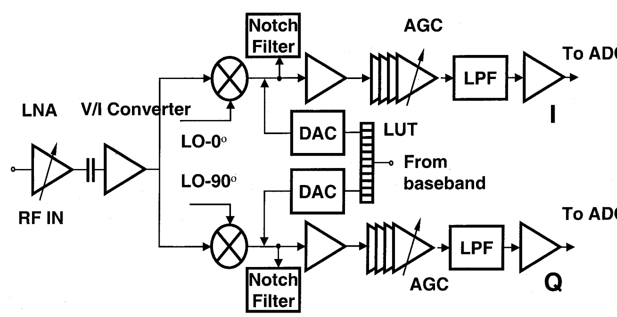

Fig. 4. Receiver architecture.

As direct conversion is more susceptible to second-order nonlinearity [4], [5], [9], ac coupling is used throughout the RF front-end and the baseband section blocks are fully differential, so as to achieve a high second-order intercept point (IP2). Note that dc coupling is employed in the entire baseband section starting from the mixer outputs. This avoids having to trade off between a degradation of signal-to-noise ratio (SNR) with a high cutoff frequency (especially when a frequency offset exits between the receiver and the transmitter) and a slow transient related to a low cutoff frequency if ac coupling were to be used.

DC offset compensation is achieved with two 7-bit DACs. Since the offset changes with the LNA gain setting, a lookup table (LUT) is incorporated in the transceiver chip and precalibrated compensation values can be selected based on gain control. An algorithm has been implemented in the baseband chip to automatically calibrate the LUT whenever the receiver (RX) is in the idle mode and no signal is detected, which is adequate since WLAN applications are mostly stationary or in slow motion. In addition, 10-bit 40-MHz ADCs are used for the receive channels to accommodate the residual dc offset, which is subsequently removed in the digital domain.

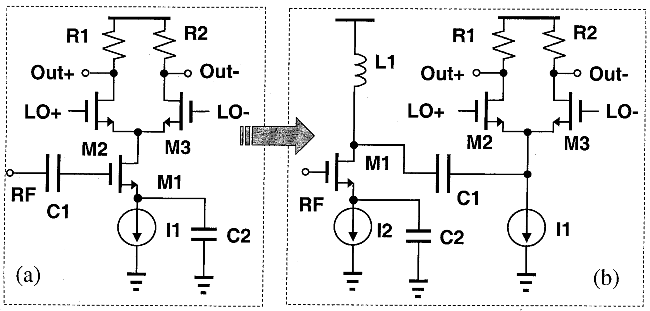

Fig. 5. Mixer design.

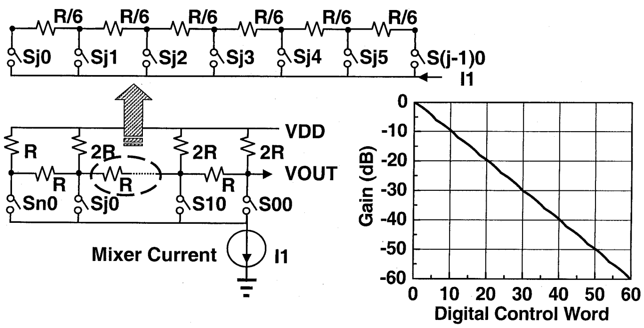

Fig. 6. Digital gain control: R-2R ladder.

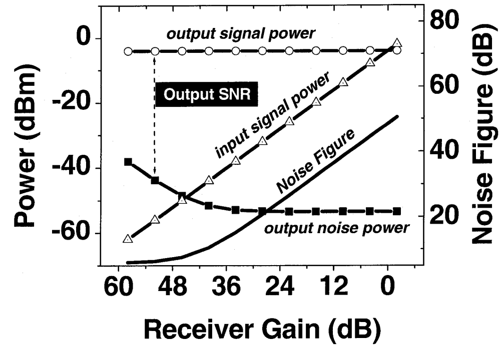

Fig. 7. For an input signal ramping in power, the RX gain is adjusted to maintain a constant output signal power level. Although the RX noise figure increases in low-gain settings, the output SNR remains higher than 34 dB in the entire dynamic range.

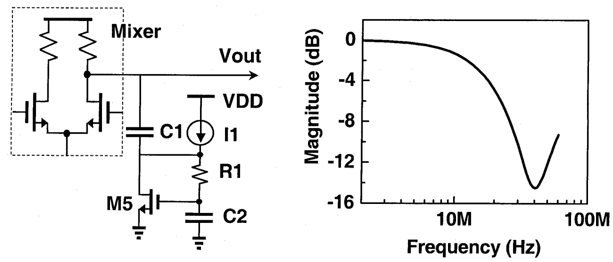

Fig. 8. Notch filter: Active-*LC* trap.

1) Mixer: The mixer is the most critical stage in the receiver chain in combating the flicker noise. In a conventional single balanced mixer [Fig. 5(a)], one faces a difficult tradeoff in choosing the proper biasing of I1. The switching quad M2, M3 exhibits lower flicker noise if I1 can be reduced, while the V/I converter M1 requires a high biasing current to achieve a decent conversion gain and good linearity.

In this work, a two-stage mixer is used [Fig. 5(b)] where the V/I converter and the switching quad biasing currents can be independently optimized [10]. Simulation shows that the two-stage mixer achieves 10 dB higher IIP3 and 5 dB lower noise figure while maintaining the same conversion gain. This performance improvement readily justifies the extra biasing current (2 mA) for the V/I stage.

Note also that the V/I output is ac coupled to the switching quad, which further improves the IP2 of the mixer stage.

2) R-2R Ladder Gain Control: The mixer load resistor is designed as a ten-section R-2R ladder (Fig. 6). By switching the mixer output current to various nodes in the R-2R network, the output voltage signal V_{OUT} varies as the power of 2, realizing 6 dB/step linear-in-dB gain control. Each R in the network can be further split into six equal parts and achieve finer gain variation at roughly 1 dB/step, nonlinear-in-dB but monotonic, as indicated in the transfer curve in Fig. 6. The R-2R ladder guarantees monotonic gain control. It is highly linear, settles fast, and maintains constant output impedance.

By maintaining constant output impedance, the noise contribution by the resistor network at the output of the RX is constant regardless of the gain setting. This ensures that the RX noise figure does not increase by more than the decibel number that the RX gain is reduced by, and therefore facilitates the implementation of an AGC algorithm that guarantees a received SNR no less than 34 dB at any low-gain settings, allowing error-free decoding for the 64-QAM signal with sufficient margin for signal fading and/or other impairments (Fig. 7).

3) Active LC-Trap: The RX chain further contains a notch filter (Fig. 8) to provide partial channel selection.

With proper biasing I1, M5 together with R1 and C2 presents inductive impedance in series with C1, and thus generates a 14-dB notch at the alternate adjacent channel of 40 MHz when coupled to the output of the mixer. Combined with the natural low-pass filtering at the mixer output (−3-dB cutoff frequency at $\sim$ 20 MHz), the notch filter rejects any interferers at 40 MHz or above by more than 14 dB, and significantly relaxes the linearity requirement of the baseband stages. Measurement shows that it improves the RX out-of-channel IIP3 by 7 dB. The notch filter takes minimal silicon area and contributes negligible flicker noise to the signal path due to the large impedance of C1 at low frequency. The thermal noise of M5 is also negligible as the flicker noise of the mixer switching quad dominates.

B. Transmitter

In the transmitter chain (Fig. 1), the LPF is designed to have a fourth-order Butterworth response with a nominal corner frequency at 12 MHz. After reconstruction filtering, the modulated signal is upconverted by a single-sideband doubly balanced mixer. The differential signal is subsequently converted to single-ended and further amplified by a power amplifier driver (PAD). An off-chip power amplifier is to be used for the overall system power saving.

In a direct-conversion transmitter, the LO leakage resides at the center of the RF signal frequency band. It is not possible to remove it with an RF filter. Although LO leakage can be due to various imbalances and mismatches both in the RF domain

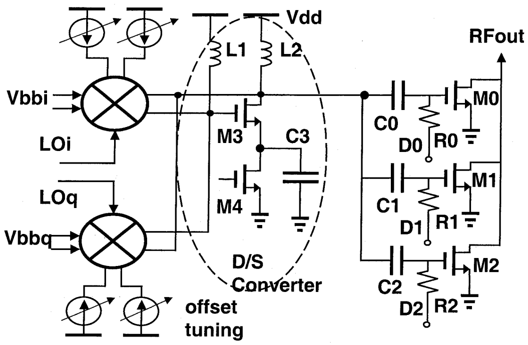

Fig. 9. Transmitter RF front-end.

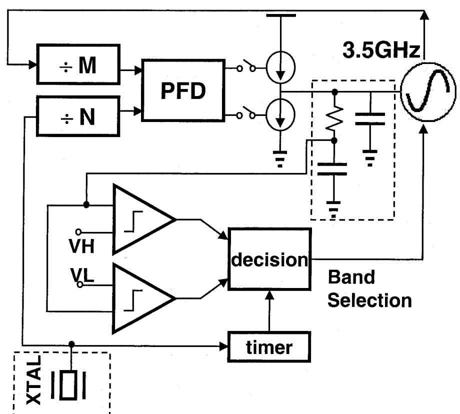

Fig. 10. Frequency synthesizer.

and baseband, it can be compensated by applying a baseband dc offset regardless of its origin. DC offset tuning is introduced to the mixers to suppress LO leakage (Fig. 9) and the calibration can be done as a production trimming. An LO rejection of more than 38 dBc is achieved without affecting the linearity or dynamic range of the TX, which is more than 20 dB better than the 802.11a standard requirement.

The D/S converter [11] consists of a capacitively degenerated common source amplifier M3, whose gate senses the positive node of the differential signal in the voltage domain and combines with the negative node in the current domain at the drain. The D/S converter shares the load inductors of the upconversion mixers, and consequently, saves area and power consumption. The PAD is designed as binary weighted parallel fingers of M0, M1, and M2, so as to achieve programmable output power.

C. Frequency Synthesizer

The frequency synthesizer (Fig. 10) is designed as an integer-N phase-locked loop (PLL). The frequency divider is implemented using a dual-modulus 8/9 prescaler and a 13-bit pulse swallow counter. The frequency synthesizer further contains a phase-frequency detector (PFD) and a high-performance charge pump. With a power supply voltage of 1.8 V, the VCO gain tends to be quite high in order to cover the required frequency range. A high VCO gain results in high sensitivity to the noise of VCO tuning voltage, which increases the spur level and degrades phase noise [12]. In this work, the required frequency range is divided into nine bands, each about 60-MHz wide with 30-MHz overlap between adjacent bands. An automatic band

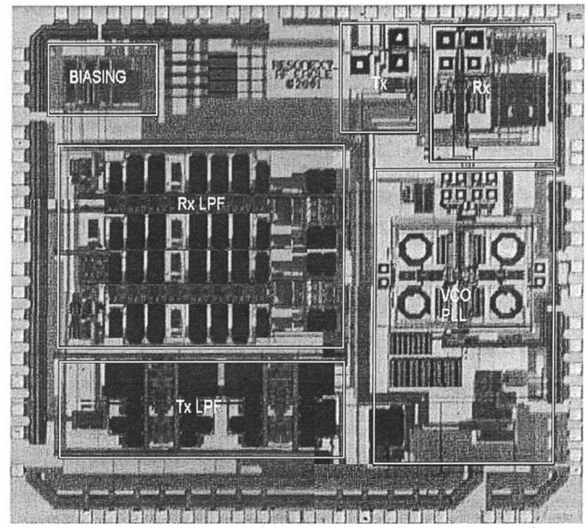

Fig. 11. Chip micrograph.

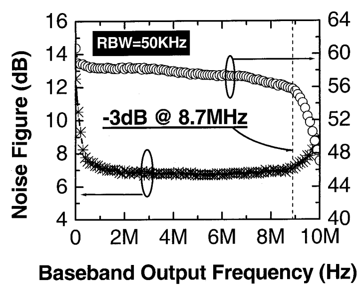

Fig. 12. Receiver gain and noise figure.

selection scheme is implemented by connecting unit capacitors to the VCO core while monitoring the varactor tuning voltage. It therefore achieves sufficient frequency tuning range while maintaining a moderate VCO gain. Within each band, continuous frequency tuning is achieved by using accumulation-mode nMOS varactors.

With a reference clock at 40 MHz, an off-chip loop filter with a bandwidth of roughly 200 kHz is found to be optimal for phase noise performance.

V. Measurement

The transceiver chip is fabricated in CMOS process with a feature size of 0.18 μm, a single poly layer, six layers of metal, and options of metal–insulator–metal (MIM) capacitors and high sheet rho poly resistors. The chip micrograph is shown in Fig. 11. The total die area is less than 13 mm^2. It is packaged in a 64-pin microlead frame with a backside central ground plate.

The RX gain and noise figure have been measured as a function of baseband output frequency with a resolution bandwidth of 50 kHz (Fig. 12). The RX provides 58-dB voltage gain, which is sufficient for the minimum sensitivity level at -82 dBm required by the 802.11a standard. Take a 10-bit ADC, for example, assuming an ADC full scale at 800 mV (1 dBV) when a 1.8-V power supply is used; the quantization noise level is at -59 dBV. A received signal at -82 dBm at the antenna port will be amplified to -34 dB Vrms at the ADC input, which is 25 dB higher than the quantization noise level, with sufficient margin

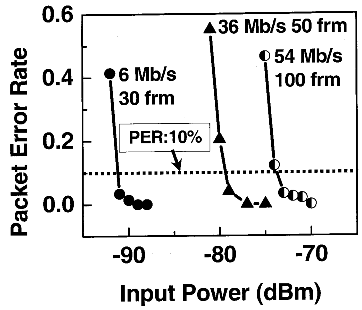

Fig. 13. Receiver sensitivity.

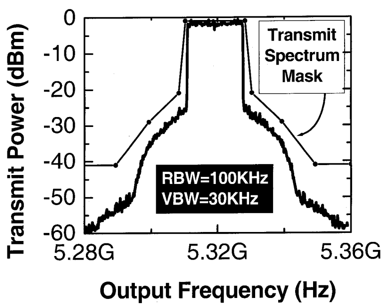

Fig. 14. TX transmit spectrum.

for ADC implementation imperfection (e.g., losing least significant bit) as well as RX gain variations due to process, temperature, and voltage supply (PTV).

A spot noise figure of 6.8 dB is measured at 5-MHz baseband signal frequency. The flicker noise effect manifests itself at and below 1 MHz. According to the 802.11a standard, the first subcarrier of the OFDM signal starts at 150 kHz, where the noise figure is about 8 dB, which is still 2 dB better than the 802.11a standard [3] noise figure assumption of 10 dB. The transfer curve also shows an LPF corner frequency at 8.7 MHz.

The received packet error rate (PER) of the RX (with T/R switch and RF filter) is measured with physical layer convergence procedure service data unit (PSDU) of 1000 bytes as indicated in the 802.11a standard. The number of frames that can be used is limited by the measurement system memory and are shown in Fig. 13. The sensitivity level is defined by the 802.11a standard as the minimum input power when the PER reaches 10%. We therefore have a sensitivity of −91 dBm at 6 Mb/s and −74 dBm at 54 Mb/s, both 9 dB better than 802.11a requirement.

In Fig. 14, the transmitted spectrum of a 64-QAM OFDM signal is plotted against the spectrum mask defined by the 802.11a standard. With a total output power of 16.2 dBm, the output spectrum is well below the spectrum mask, indicating a good linearity margin. Note that the transceiver chip delivers roughly −5 dBm of total power in this case, and the rest of the RF gain is made up by an external PA. Fig. 15 shows the transmit constellation of the same 64-QAM OFDM signal. The error vector magnitude (EVM) is found to be less than −29 dB, which is well below the standard requirement of −25 dB, indicating sufficient linearity and phase noise performance.

The open-loop VCO phase noise has been characterized at the divided-by-2 output. Centered on 1.75 GHz, the single side-band phase noise is roughly −120 dBc/Hz at an offset frequency of 1 MHz. The closed-loop phase noise is measured at the TX output with the center frequency at 5.25 GHz. Integrated from 10 kHz to 10 MHz, the total phase error is less than 1.5° (Fig. 16).

Table I is a summary of the transceiver performance.

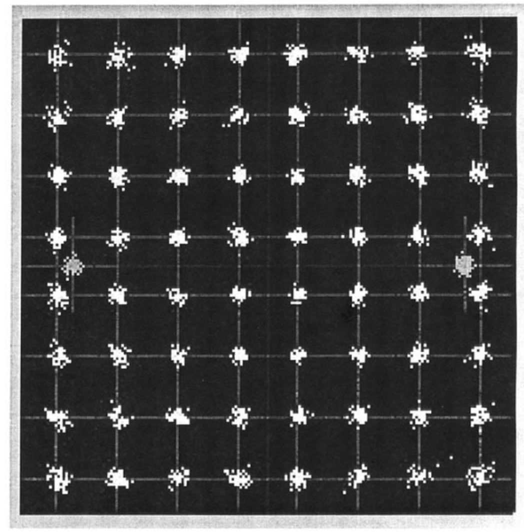

Fig. 15. Transmit constellation.

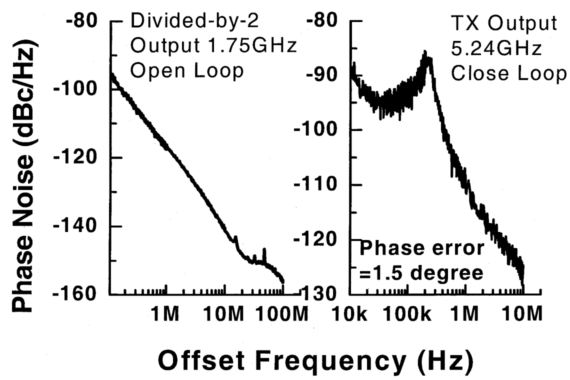

Fig. 16. LO phase noise.

TABLE I
TRANSCEIVER PERFORMANCE SUMMARY

Parameters	Conditions	Results	Units
Power Consumption (VCC=1.8V)	Receive mode	171	mW
	Transmit mode (P_{linear}= -5 dBm)	135	mW
Rx Voltage Gain		58	dB
Rx IIP3	In channel	-25	dBm
	Out of Channel	-18	dBm
Noise Figure	5 MHz down converted signal	6.8	dB
Tx Output -1dB GCP		5	dBm
Tx OIP3		15	dBm
Tx LO Rejection	With offset control tuning	38	dBc
Tx Sideband Rejection		50	dBc
LO Phase Noise	Integrated (Δf = 10 kHz to 10 MHz from 5.24 GHz)	1.5	°
LO Reference Spur	@ 13.33 MHz	-66	dBc

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In 1998, he joined DigitalDNA Labs, Motorola, and became a Staff Research Scientist/Project Leader. He led the efforts in 80-nm CMOS technology development. In 2001, he joined Resonext Communications, where he worked in the field of mixed-signal VLSI design for WLAN (802.11a/b/g) chipset. He has been with RF Micro Devices after the acquisition of Resonext in 2002. He has authored or coauthored 42 publications in many journals and conferences. He holds four patents in semiconductor technology and has three patents pending. His current research interests are in the areas of wireless communications, networking, and semiconductor technology.

Siegfried Hart (S'95–M'97) was born in Rosenheim, Germany, in 1967. He received the B.S. degree in electrical engineering from the Fachhochschule München, Munich, Germany, in 1995, and the M.S. degree in electrical engineering from Wayne State University, Detroit, MI, in 1997.

From 1997 to 2000, he was with the Datacom Business Unit of Infineon Technologies, Munich, where he was a Project Lead for a family of wireline transceivers and introduced Infineon's first E3/T3 transceiver product to the marketplace. From 2000 to 2001, he was with Infineon Technologies, Santa Cruz, CA, where he was involved in the design of high-speed CMOS read/write channel ICs for next-generation disk drives. In 2001, he joined Resonext Communications (now RF Micro Devices) to work on CMOS direct-conversion radio transceivers for 802.11a/b/g wireless LAN. He holds several international patents and has coauthored papers in the field of ultralow-noise circuits for charge sensing and CMOS-integrated RF transceivers. His current research interests are CMOS-integrated WLAN transceivers as well as analog-to-digital and digital-to-analog converter design for communication systems.

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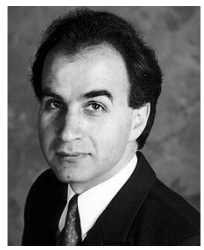
Taoufik Bourdi (M'98) is working toward the Ph.D. degree in mixed-signal ICs at Westminster University, London, U.K.

He is currently a Member of Technical Staff with RF Micro Devices, Inc., San Jose, CA. His current work is in the area of mixed-signal/RFIC CMOS design for wireless transmission systems. This includes the design and implementation of delta-sigma fractional-N frequency synthesizers and oversampled DAC/ADC architectures. He was with Resonext Communications before its acquisition by RF Micro Devices. Previously, he was with Nokia U.K., Ltd., where he was a Senior Design Engineer; his work involved the development of new RF technology architectures including fast frequency hopping synthesizers for the GSM/DCS and PCS base station transceivers. His main interests are RFIC and mixed-signal IC circuits, systems, and architectures for wireless transmission systems.

Andrew (KhongMeng) Tham (M'97) received the App. Sci. Electronics degree from University Science Malaysia, Malaysia, in 1978, and the M.S.E.E. degree from Lehigh University, Bethlehem, PA, in 1990.

From 1978 to 1985, he was with Intel Corporation in various functions as Equipment, Test, and Product Engineer. He was with Bell Laboratories, AT&T, Reading and Allentown, PA, from 1985 to 1995, designing mixed-signal CMOS T1/E1 transceiver devices. Since 1995, he has been several wireless communication companies, including Qualcomm, Prominent, and Resonext Communications, involved in the design and management of cellular, Bluetooth and WLAN integrated circuits. He is currently with RF Micro Devices, San Jose, CA.



Behzad Razavi (S'87–M'90–SM'00–F'03) received the B.Sc. degree in electrical engineering from Sharif University of Technology, Tehran, Iran, in 1985 and the M.Sc. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 1988 and 1992, respectively.

He was an Adjunct Professor at Princeton University, Princeton, NJ, from 1992 to 1994, and at Stanford University in 1995. He was with AT&T Bell Laboratories and Hewlett-Packard Laboratories until 1996. Since September 1996, he has been an Associate Professor and subsequently Professor of electrical engineering at the University of California, Los Angeles. He is the author of *Principles of Data Conversion System Design* (New York: IEEE Press, 1995), *RF Microelectronics* (Englewood Cliffs, NJ: Prentice-Hall, 1998), *Design of Analog Integrated Circuits* (New York: McGraw-Hill, 2001), *Design of Integrated Circuits for Optical Communications* (New York: McGraw-Hill, 2002), and the editor of *Monolithic Phase-Locked Loops and Clock Recovery Circuits* (New York: IEEE Press, 1996). His current research includes wireless transceivers, frequency synthesizers, phase-locking and clock recovery for high-speed data communications, and data converters.

Dr. Razavi received the Beatrice Winner Award for Editorial Excellence at the 1994 ISSCC, the Best Paper Award at the 1994 European Solid-State Circuits Conference, the Best Panel Award at the 1995 and 1997 ISSCC, the TRW Innovative Teaching Award in 1997, and the Best Paper Award at the IEEE Custom Integrated Circuits Conference in 1998. He was the corecipient of the Jack Kilby Outstanding Student Paper Award at the 2002 ISSCC. He served on the Technical Program Committee of the International Solid-State Circuits Conference (ISSCC) from 1993 to 2002. He has also served as Guest Editor and Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS, and the *International Journal of High Speed Electronics*. He is recognized as one of the top ten authors in the 50-year history of ISSCC. He is also an IEEE Distinguished Lecturer.