

# A 5-GHz Fully Integrated Full PMOS Low-Phase-Noise LC VCO

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**Abstract**—A 5-GHz fully integrated, full PMOS, low-phase-noise and low-power differential voltage-controlled oscillator (VCO) is presented. This circuit is implemented in a 0.35- $\mu\text{m}$  four-metal BiCMOS SiGe process. At 2.7-V power supply voltage and a total power dissipation of only 13.5 mW, the proposed VCO features a worst case phase noise of  $-97$  dBc/Hz and  $-117$  dBc/Hz at 100 kHz and 1 MHz frequency offset, respectively. The oscillator is tuned from 5.13 to 5.68 GHz with a tuning voltage varying from 0 to 2.7 V.

**Index Terms**—Cyclostationary noise, design method, phase noise, PMOS, symmetric center-tapped inductor, varactors, voltage-controlled oscillator (VCO).

## I. INTRODUCTION

INCREASING pressure for lower power, higher integration, and lower cost in the mobile communication market will, in the near future, drive industry to “on-chip” solutions. This will be made possible by the continuous scaling down of CMOS processes which allows the use of MOSFETs for low-noise applications up to microwave frequencies. Indeed, the substrate resistivity of such technologies is now close to what is obtainable with a BiCMOS SiGe technology. Also, the  $f_T$  of the MOS transistors increases with decreasing geometry.

In this context, this work presents the design of an original 5-GHz, full PMOS, low-phase-noise and low-power differential voltage-controlled oscillator (VCO) using a 0.35- $\mu\text{m}$  BiCMOS SiGe process of Jazz Semiconductor. The feasibility of such a high-performance high-frequency VCO with only pMOS transistors, with  $f_T$  (16 GHz) much lower than that possible with advanced CMOS processes, is demonstrated.

This paper is organized as follows. Section II treats the circuit design with two subsections concerning the design method used to minimize the phase noise and the VCO core design. Section III presents the implementation and measurement results, followed by the conclusion in Section IV.

## II. CIRCUIT DESIGN

### A. Phase Noise Minimization

From the well-known Leeson model [1], it can be concluded that the loaded quality factor  $Q$  of the tank needs to be maximized

Manuscript received February 22, 2005; revised June 14, 2005.

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Digital Object Identifier 10.1109/JSSC.2005.854601

in order to reduce phase noise. Unfortunately, the integration of a high- $Q$  LC tank is not easy because of the medium resistivity of Silicon substrate ( $\approx 10 \Omega\cdot\text{cm}$ ). In the same way, this model recommends to maximize the dissipated power in the resistive part of the resonator, which is related to the added power of the oscillator amplifier [2]. In other words, the voltage swing across the resonator needs to be maximized, without entering the triode region of the MOS transistor. However, in most cases, the dominant noise contributor in oscillators or VCOs is the collector shot noise for bipolar transistors and channel noise for CMOS transistors [3], [4]. These cyclostationary noise sources have been related to waveform signals. Indeed, according to the linear time-varying phase noise theory of Hajimiri [5], the total single sideband phase noise spectral density in dBc/Hz due to one current noise source on one node of the circuit at an offset frequency  $\Delta\omega$  is given by

$$L(\Delta\omega) = 10 \cdot \log \left( \frac{(\overline{i_n^2}/\Delta f) \cdot \Gamma_{\text{rms}}^2}{2 \cdot q_{\text{max}}^2 \cdot \Delta\omega^2} \right) \quad (1)$$

where  $\overline{i_n^2}/\Delta f$  is the power spectral density of the current noise source in question,  $\Gamma_{\text{rms}}^2$  is the rms value of the impulse sensitivity function (ISF) associated with the noise source considered previously, and  $q_{\text{max}}$  is the maximum charge swing across the current noise source. Considering that a white cyclostationary noise current can be written as the product of a white stationary process and a deterministic periodic function  $\alpha(x)$  describing the noise amplitude modulation and strongly correlated with currents waveforms of the oscillator, the cyclostationary noise can be treated as a stationary noise by introducing the effective ISF given by

$$\Gamma_{\text{eff}}(x) = \Gamma(x)\alpha(x). \quad (2)$$

Thus, the phase noise due to the cyclostationary current noise source is expressed by (1) replacing  $\Gamma_{\text{rms}}^2$  by  $\Gamma_{\text{eff,rms}}^2$ . Consequently,  $\Gamma_{\text{eff,rms}}$  needs to be minimized in order to reduce phase noise significantly. In other words, the transistor would remain off almost all of the time, waking up periodically to deliver an impulse of current at the signal peak of the oscillator, where the ISF ( $\Gamma(x)$ ) has its minimum value [6]. This induces a class-C operation of the active element within the VCO. Thus, the design method used to minimize the phase noise of the VCO consists essentially in optimizing the circuit for a class-C operation of the active part with a maximum voltage swing across the resonator.

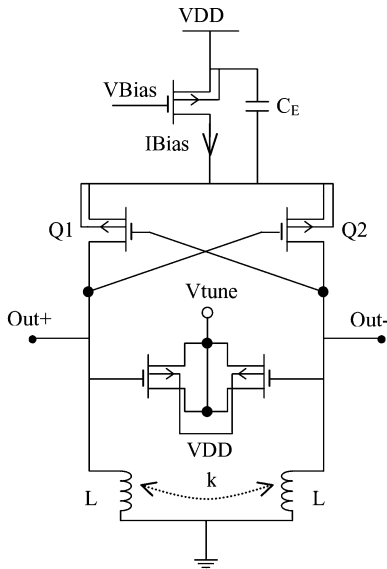


Fig. 1. VCO schematic.

### B. VCO Core Design

Fig. 1 shows the VCO schematic using a cross-coupled pMOS differential topology which is the complementary structure to the well-known “nMOS only” architecture. A tail capacitor  $C_E$  is used to attenuate both the high-frequency noise components of the tail current and the voltage variations on the tail node. This latter effect results in more symmetric waveforms and smaller harmonic distortion in VCO outputs. Thus, the most significant remaining noise component of the tail current noise source is the upconversion of the flicker noise [7]. In this condition, the use of a pMOS tail-current source is justified since the pMOS transistors have lower  $1/f$  noise than the nMOS [8], [9]. In addition, one must increase the width and the length of the pMOS tail transistor to further reduce the flicker noise which lowers significantly the close-in phase noise of the VCO [8]. Furthermore, this capacitor provides an alternative path for the tail current and, consequently, if the capacitor is large enough, the transistors of the differential pair might carry very little current for a fraction of the cycle [7]. Thus, the duty cycle of the drain current waveform is significantly reduced. This effect is very important since it reduces the drain current noise injection during the zero-crossing of the tank differential voltage (i.e., when the ISF is maximum). Consequently, this behavior is consistent with an improvement of the phase noise performances of the VCO as explained in the previous subsection.

The use of a symmetric center-tapped inductor as opposed to two “uncoupled” inductors exploits the benefits of the coupling factor  $k$  to increase the inductance value and can lead to a saving in chip area. Furthermore, it is now well known that a higher peak quality factor can be achieved by exciting an inductor differentially rather than single-endedly [10].

This inductor was fabricated with the last metal level, which presents a low resistivity ( $10 \text{ m}\Omega/\text{sq.}$ ). The layout of the center-tapped inductor is shown in Fig. 2 and Fig. 3 shows its broadband three-port equivalent circuit model. As shown in

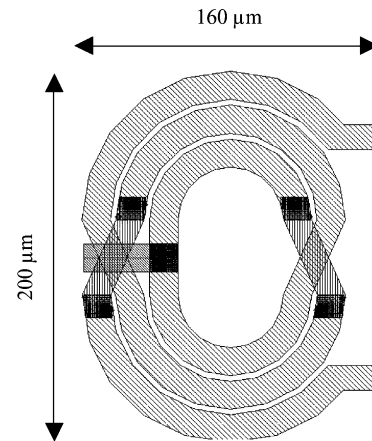


Fig. 2. Layout of the center-tapped inductor.

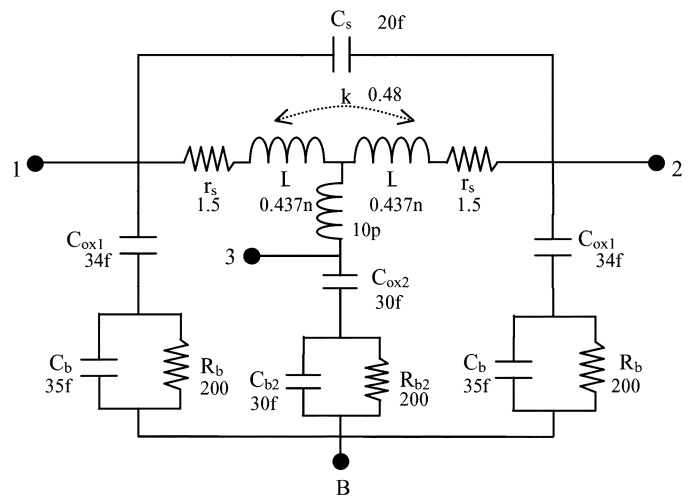


Fig. 3. Lumped circuit model of the inductor.

this figure, the global inductance value is about  $1.3 \text{ nH}$ . Both the single-ended quality factor

$$Q = -\frac{\text{Im}(Y_{11})}{\text{Re}(Y_{11})} \quad (3)$$

and differential quality factor

$$Q_{\text{diff}} = \frac{\text{Im}(Z_{11} + Z_{22} - Z_{12} - Z_{21})}{\text{Re}(Z_{11} + Z_{22} - Z_{12} - Z_{21})} \quad (4)$$

are evaluated and plotted in Fig. 4. As shown in this figure, the associated differential  $Q$  factor of the symmetric center-tapped inductor is estimated to be in the range of 12 to 13 at 5 GHz. Furthermore, let us note that an improvement of the maximum  $Q$  factor of about 30% for the inductor driven differentially over that of the same inductor driven single-endedly is observed.

PMOS varactors are used in inversion mode because of the wide capacitor variation that can be obtained with a low variation of source to gate bias voltage [11]. Consequently, the use of MOS varactors is consistent with the new CMOS technologies because of the low supply voltage required.

The tail-current value ( $I_{\text{Bias}}$ ) is maximized while maintaining a *current-limited* mode of operation since, in this mode, the voltage swing across the resonator is proportional to the

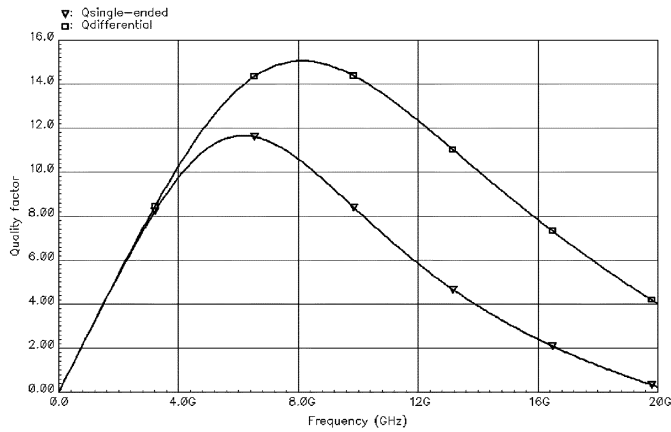


Fig. 4. Simulated  $Q$  factor of the inductor driven single-endedly versus differentially.

tail-current and the tank equivalent resistance [4], [7]. Transistors Q1 and Q2 are properly sized to obtain a large enough transconductance value to ensure proper startup of the VCO but sufficiently small to reduce thermal noise.

### III. IMPLEMENTATION AND MEASUREMENT RESULTS

A  $0.35\text{-}\mu\text{m}$  BiCMOS SiGe process, which provides four metal layers with a  $3\text{-}\mu\text{m}$ -thick top metal, is used to implement the oscillator. Fig. 5 shows the microphotograph of the fabricated VCO whose size is only  $300 \times 650 \mu\text{m}^2$ . During the layout, we have focus on the symmetry of the balanced circuit. For frequency measurements, an Agilent E4407B spectrum analyzer is used. The tuning characteristic of the VCO for different bias currents is shown in Fig. 6. As expected in simulations, the VCO is tuned from roughly 5.13 to 5.68 GHz with a tuning voltage varying from 0 to 2.7 V. As the slope of the characteristic is relatively linear between 0.5 and 1.5 V, the VCO is suited for frequency synthesizer realization (PLL). Unfortunately, the steep slope of the tuning characteristic leads to the undesirable effect of higher VCO gain even if this can be compensated by connecting in parallel one or more pMOS varactors biased at different voltages to linearize the  $C(V)$  characteristic of the resulting varactor [12]. Furthermore, due to the complementary nature of this VCO, the frequency decreases with an increase of the tuning voltage. Thus, for use in a conventional PLL architecture, the input of the charge pump must be inverted. Fig. 7 shows the tuning characteristic of the VCO for different supply voltages. As shown in this figure, for a tuning voltage of 1 V, the maximum variation of the oscillation frequency is only 34 MHz for a supply voltage varying from 2.5 to 3.3 V. Furthermore, temperature measurements between  $-40^\circ\text{C}$  and  $80^\circ\text{C}$  have shown a variation of the oscillation frequency of only 5% in the worst case confirming the excellent robustness of this circuit.

Phase noise was measured using the delay line method and a battery is used as supply voltage to avoid external parasitic signals. Fig. 8 shows the plot of the measured phase noise at 100 kHz frequency offset versus the tuning voltage and Fig. 9 shows the plot of the phase noise versus offset frequency for a tuning voltage of 0.5 V.

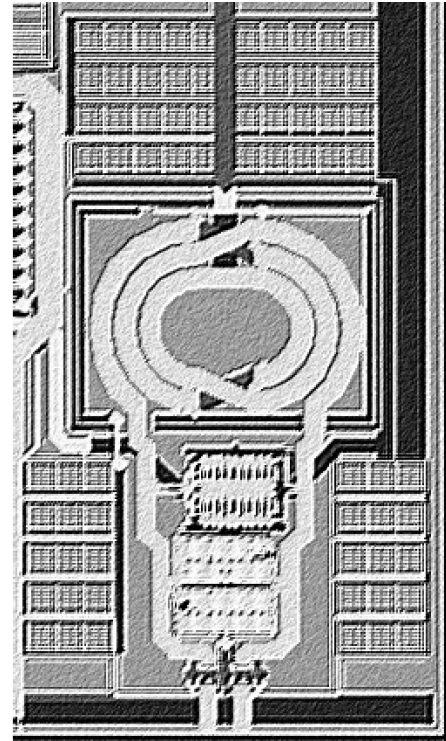


Fig. 5. 5-GHz VCO microphotograph.

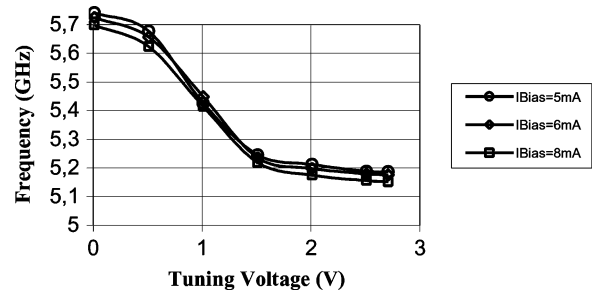


Fig. 6. Tuning characteristic of the VCO for different bias currents.

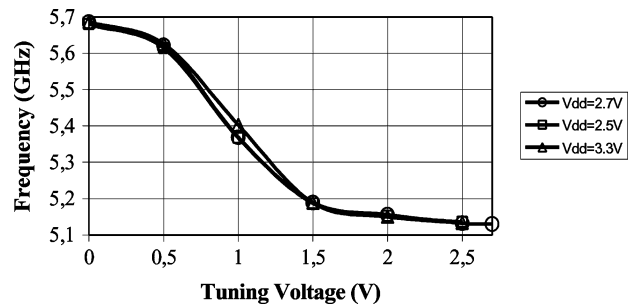


Fig. 7. Tuning characteristic for different supply voltages.

As shown in those two figures, the VCO features a worst case phase noise of  $-97$  dBc/Hz and  $-117$  dBc/Hz at 100 kHz and 1 MHz frequency offset, respectively. A figure of merit (FOM) has been defined in [13] to compare VCOs performances

$$\text{FOM} = L(\Delta\omega) [\text{dBc/Hz}] + 10 \cdot \log(P_{\text{DC}} [\text{mW}]) - 20 \cdot \log\left(\frac{\omega_0}{\Delta\omega}\right) \quad (5)$$

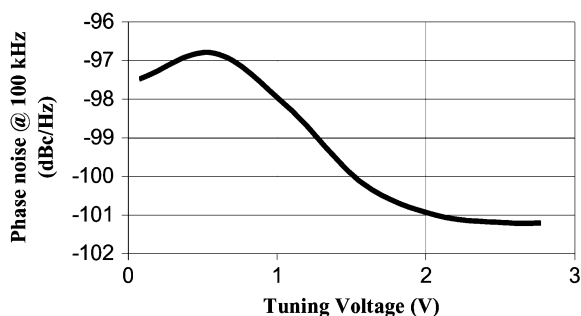


Fig. 8. Measured phase noise at 100 kHz versus tuning voltage.

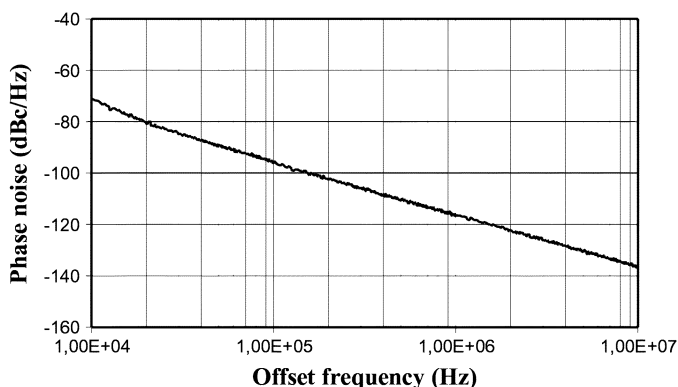


Fig. 9. Measured phase noise of the VCO for a tuning voltage of 0.5 V.

TABLE I  
VCO PERFORMANCES COMPARISON

| VCO         | Tech.                     | Frequency [GHz] | Power [mW] | PN [dBc/Hz]    | FOM [dBc/Hz] |
|-------------|---------------------------|-----------------|------------|----------------|--------------|
| [14]        | 0.18 $\mu\text{m}$ CMOS   | 5.8             | 8.1        | -110 @ 1 MHz   | -176         |
| [9]         | 0.24 $\mu\text{m}$ CMOS   | 5.8             | 5          | -112 @ 1 MHz   | -180         |
| [15]        | BiCMOS 0.35 $\mu\text{m}$ | 1.91            | 10         | -121 @ 600 kHz | -176.6       |
| (this work) | BiCMOS SiGe 0.35          | 5.6             | 13.5       | -117 @ 1 MHz   | -180         |

where  $L(\Delta\omega)$  is the total single sideband phase noise spectral density at an offset frequency  $\Delta\omega$ ,  $P_{\text{DC}}$  is total VCO power consumption, and  $\omega_0$  is the pulsation of oscillation. This results in a FOM of  $-180$  for this design.

In Table I, some recently published VCOs are listed. As shown in this table, our results compare favorably to other recently published fully integrated VCO performances. The measured performances of this 5-GHz, fully integrated, full pMOS VCO are summarized in Table II.

#### IV. CONCLUSION

The feasibility of a high-performance, high-frequency, fully integrated VCO with only pMOS transistor with poor  $f_T$  (16 GHz) is demonstrated in this paper. The fabricated VCO is tuned from 5.13 to 5.68 GHz with a tuning voltage varying from 0 to 2.7 V. The phase noise of the oscillator was optimized by taking into account for cyclostationary noise phenomena. Measured worst case phase noise is  $-97$  dBc/Hz

TABLE II  
5-GHz VCO MEASURED PERFORMANCES SUMMARY

|   |         |
|---|---------|
| Supply Voltage (V)                        | 2.7     |
| Power Consumption (mW)                    | 13.5    |
| Area ( $\mu\text{m}^2$ )                  | 300*650 |
| Tuning Range (MHz)                        | 550     |
| Tuning Voltage (V)                        | 0-2.7   |
| $F_0$ (GHz)                               | 5.4     |
| Phase Noise @ 100 kHz (dBc/Hz) at 5.6 GHz | -97     |
| Phase Noise @ 1 MHz (dBc/Hz) at 5.6 GHz   | -117    |

and  $-117$  dBc/Hz at 100 kHz and 1 MHz frequency offset, respectively, under 2.7-V power supply voltage with only 5-mA current consumption.

#### ACKNOWLEDGMENT

The authors wish to acknowledge P. Colestock from Jazz Semiconductor and O. Llopis and G. Cibiel from the LAAS-CNRS for phase noise measurements.

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