# A 5-GHz Radio Front-End With Automatically *Q*-Tuned Notch Filter and VCO

John W. M. Rogers, Member, IEEE, and Calvin Plett, Member, IEEE

Abstract—A low-voltage receiver front-end for 5-GHz radio applications is presented. The receiver consists of a low-noise amplifier (LNA) with notch filter, a voltage-controlled oscillator (VCO), and a mixer. The LNA/notch filter has an automatic Q-tuning circuit integrated with it to provide good image rejection. On-chip transformers are used extensively in the receiver to improve performance and facilitate low-voltage operation. The receiver has a gain of 19.8 dB, noise figure of 4.5 dB, a third-order input intercept point (IIP3) of -11.5 dBm, and an image rejection of 59 dB, and the VCO had a phase noise of -116 dBc/Hz at 1-MHz offset.

*Index Terms—LC* filters, phase noise, *Q*-tuning, radio-frequency integrated circuit (RFIC), SiGe, voltage-controlled oscillator (VCO), wireless communications.

## I. INTRODUCTION

**R** ECENTLY, there has been much interest in monolithically integrated receivers for wireless local-area networks, such as 802.11a WLAN. Two of the most challenging components are the voltage-controlled oscillator (VCO) and image filter. Creating a band stop filter on chip is complicated by the need to *Q*-tune it for best image rejection. In addition, low supply voltage makes VCO design more difficult due to limited headroom. In this paper, we present a prototype design for a lowvoltage low-power receiver with on-chip VCO and notch filter. Performance at low supply voltage is enhanced through extensive use of on-chip transformers.

The receiver consists of a low-noise amplifier (LNA) with coupled resonator for image rejection, a low-voltage mixer, an on-chip local oscillator, and a Q-tuning circuit for the filter, as shown in Fig. 1. Together, they form a superheterodyne receiver front-end. In this paper, the local oscillator (LO) is high-side injected, which places the image frequency above the LO frequency. The design for each circuit will be discussed next. The design of the LNA and notch filter is discussed in Section II, followed by discussion of the VCO in Section III. The mixer is discussed in Section IV and the transformer in Section V. Experimental results are presented in Section VI, followed by conclusions in Section VII. The complete receiver circuit schematic is given in Fig. 2 and will be used to discuss each block.

#### II. LNA AND NOTCH FILTER DESIGN

There has been much interest in integrated high-frequency filters recently [1]–[13]. Some previous receiver designs used a

The authors are with the Department of Electronics, Carleton University, Ottawa, ON K1S 5B6, Canada.

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Fig. 1. Block diagram of the superheterodyne front-end.

separate LNA followed by an image-reject notch filter, or modified the LNA itself by placing a series resonant circuit at the cascode transistor's emitter [10]–[13]. In contrast, our approach modifies a conventional cascode LNA by adding a capacitor  $C_{\text{var}}$  in parallel with the inductor  $L_{s1}$ , as shown in Fig. 3 [14]. This *LC* resonator is centered at the notch frequency and, therefore, presents a high impedance to the emitter of the driving transistor coupled through the transformer. A high impedance here means that the driver will have a very low gain (ideally, a zero gain) at the image frequency. Thus, the LNA will reflect the image. Below the resonance frequency, the emitter of  $Q_1$  will see an impedance close to that of  $L_{p1}$ . Thus, in the passband, the LNA will still look like an LNA with inductive degeneration.

Active circuitry is added to cancel losses in the *LC* resonator. A simple way to implement this is to add feedback in the form of a  $-G_m$  cell (the notch filter), as shown in Fig. 2(b). The filter notch frequency is tunable by the use of varactors  $C_{\text{var}}$ . Due to process variations, the current  $I_{\text{sharp}}$  will need to be tuned as well, to ensure perfect cancellation of the resonator losses.

## A. Image-Rejection Formulas

In the passband,  $C_1$  and  $L_{p2}$  of Fig. 3 resonate and the impedance of the collector tank is  $R_1$ , while  $C_{var}$  and  $L_{s1}$ are below their resonance frequency and the impedance seen at the emitter of  $Q_1$  is roughly that of  $L_{p1}$ . In the stopband, the collector tank is above resonance, so its impedance is roughly that of  $C_1$ , while the emitter tank is at resonance and its impedance is  $R_{Tot}$  where  $R_{Tot}$  is the combination of  $R_{e1}$ (the tank loss referred to the primary of the transformer) of the transformer) and  $-R_{loss}$  (also referred to the primary of the transformer). Thus, the gain in the LNA passband  $G_{PB}$  and the



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Fig. 2. Schematic of the entire receiver front-end. (a) LNA. (b) Notch filter. (c) Master Q-tuning circuit. (d) VCO. (e) Mixer.



Fig. 3. LNA with image rejection shown conceptually.

gain in the stopband  $G_{\rm SB}$  are given by

$$G_{\rm PB} \approx \frac{Z_L}{Z_e(\omega_{\rm PB})} = \frac{R_1}{\omega_{\rm PB}L_{p1}}$$
(1)  
$$G_{\rm SB} \approx \frac{Z_L}{Z_{eL}} = \frac{1}{C_{eL}}.$$
(2)

$$J_{\rm SB} \approx \frac{2}{Z_e(\omega_{\rm SB})} = \frac{1}{\omega_{\rm SB}C_1R_{\rm Tot}}.$$

 $R_{\text{loss}}$  is generated by the notch filter  $-G_m$  cell, as shown in Fig. 2(b), and has a value of  $-2/g_m$  where  $g_m$  is the transconductance of  $Q_5$  and  $Q_6$  and, therefore,  $R_{\text{Tot}}$  can be approximated as

$$R_{\rm Tot} = \frac{R_{e1}R_{\rm loss}}{R_{e1} + R_{\rm loss}} = \frac{-2N_L R_{e1}}{g_m R_{e1} - 2N_L}$$
(3)

where  $N_L$  is the inductance ratio of the transformer in the emitter. Thus, the image rejection can be approximated as

$$IR = 20 \log \left(\frac{G_{PB}}{G_{SB}}\right)$$
$$= 20 \log \left[\frac{R_1 \omega_{SB} C_1}{\omega_{PB} L_{p1}} \left(\frac{-2N_L R_{e1}}{g_m R_{e1} - 2N_L}\right)\right].$$
(4)

This formula shows that the image rejection can be made infinite with proper adjustment of  $g_m$ . However, even with perfect tuning, there will always be some finite amount of signal leakage through  $C_{\mu}$  of  $Q_1$ . In this case, the minimum image rejection can be shown to be

$$\mathrm{IR}_{\mathrm{min}} = 20 \log \left( \frac{R_1}{\omega_{\mathrm{PB}} L_{p1}} \sqrt{\left(\frac{\omega_{\mathrm{SB}} C_1}{g_m}\right)^2 + \left(\frac{C_1}{C_{\mu}}\right)^2} \right).$$
(5)

## B. Filter Stability

The fundamental problem of filter stability is nontrivial: how to stabilize an *LC* resonator specifically designed to have infinite Q, since an *LC* oscillator design begins with a resonator with infinite Q [15]. The mechanism for damping the oscillation must come from either the source or load impedance. In previous work [10]–[13], the cascode transistor provided damping for the resonator. In this circuit, the source impedance must damp the filter.

For perfect notching, negative resistance  $R_{\text{loss}}$  of Fig. 3 must equal tank losses referred to the secondary of the transformer  $R_{e2}$  so the optimal current [shown in Fig. 2(b)] must be

$$I_{\text{sharp-opt}} = \frac{2V_T}{R_{e2}}.$$
(6)

To start an oscillation requires the negative resistance to be equal to the parallel combination of both the tank losses and the loading due to the emitter of  $Q_1 r_{e1}$ . Therefore, for oscillations to start requires a current of

$$I_{\text{sharp\_osc}} = \frac{2V_T N_L \left(R_{e2} + \frac{r_{e1}}{N_L}\right)}{R_{e2} r_{e1}}.$$
 (7)

The ratio of these two currents is then given by

$$\frac{I_{\text{sharp-osc}}}{I_{\text{sharp-opt}}} = 1 + \frac{N_L R_{e2}}{r_{e1}}.$$
(8)

Thus, if the source resistance is smaller than the tank resistance, then the tank can be safely tuned to provide infinite Q and still have ample damping. However, if the tank resistance is smaller than the source resistance, then even a small error in tuning the tank to infinite Q could result in oscillation.

# C. Linearity of the Filter

The filter resonator is part of the signal path, so if a very large signal is present on the resonator, performance can be degraded. Large signals will change the effective  $g_m$  of the filter transistors  $Q_5$  and  $Q_6$ , and therefore, the negative resistance is changed and image rejection suffers.

If a transistor without degeneration is driven with a voltage source  $v_{in}$ , then we can find the effective  $g_m$  as

$$g_{m} = \frac{di_{c}}{dv_{\text{in}}}$$

$$= I_{C} \left[ \frac{1}{V_{T}} + \frac{v_{\text{in}}}{V_{T}^{2}} + \frac{1}{2} \frac{v_{\text{in}}^{2}}{V_{T}^{3}} + \cdots \right]$$

$$= g_{\text{mss}} \left[ 1 + \frac{v_{\text{in}}}{V_{T}} + \frac{1}{2} \frac{v_{\text{in}}^{2}}{V_{T}^{2}} + \cdots \right].$$
(9)

For small  $v_{in}$ , this takes on the small-signal value  $g_{mss}$  of  $I_c/V_T$ ; however, as the signal grows this value changes. Thus, with a  $-G_m$  resonator, the negative resistance is

$$\frac{R_{\text{neg}}}{R_{\text{negss}}} = \frac{-2/g_m}{-2/g_{\text{mss}}} = \left[1 + \frac{v_{\text{in}}}{V_T} + \frac{1}{2}\frac{v_{\text{in}}^2}{V_T^2} + \cdots\right]^{-1}$$
(10)

where  $R_{negss}$  is the small-signal negative resistance. Since the voltage across the resonator is twice that across any transistor, at a resonator voltage of about  $2V_T$ , its effectiveness will degrade. At the image frequency, this corresponds to a maximum input level of about 100 mV. Because the transformer has a 2:1 turns ratio, the voltage across the resonator is halved. Note that linearity can be improved by adding degeneration resistors to  $Q_5$  and  $Q_6$ .

## D. Noise Added Due to the Filter

Sources of noise in an LNA are base shot noise, collector shot noise, and base resistance. If we assume that noise comes from the driver transistor, then the noise figure (NF) of an LNA with a notching circuit would be approximated as shown in (11) at the bottom of the page, where  $Z_{eq}$  is the impedance seen at the base of  $Q_1$  and  $I_{C1}$  is the collector current of  $Q_1$ . In addition, in the filter, active circuitry in the emitter will add extra noise. If we assume that the noise produced by the resonator is dominated by collector shot noise in the case of the  $-G_m$  resonator, then the output noise current is given by

$$\overline{I_{\text{out}_{notch}}}^2 \approx \left(\sqrt{2q\frac{I_{\text{sharp}}}{2}}\right)^2 + \left(\sqrt{2q\frac{I_{\text{sharp}}}{2}}\right)^2$$
$$= 2qI_{\text{sharp}}.$$
(12)

This noise current is passed through the transformer, injected into the emitter of  $Q_1$ , then passed into the collector of  $Q_2$ . Therefore, the NF at the output with the notching circuitry is as shown in (13) at the bottom of the next page. This is the same as for an LNA except with an additional term due to  $I_{\text{sharp}}$ . Thus, the LNA built with the filter can never be as quiet as a true LNA. Here, the transformer also helps performance by transforming the noise current produced by the notch filter circuitry to a lower value.

Note that in the case of a Q-enhanced bandpass filter, since the gain is very high, this noise current could produce a large output voltage. This same noise current in the case of notch filters will create a large noise voltage on the notch resonator, due to its high Q. However, the output voltage will be much lower due to the presence of a lower impedance.

## E. Automatic Q-Tuning for the Notch Filter

Image-reject notch filters are little more than curiosities unless they can be tuned automatically on chip. The current through the resonator must be set precisely so that the losses

$$NF_{LNA} \approx \frac{\frac{2qI_{C1}}{\beta_o} Z_{eq}^2 \cdot \left(\frac{R_1}{Z_{L_e}}\right)^2 + 2qI_{C1}R_L^2 + 4kTr_b \cdot \left(\frac{R_1}{Z_{L_e}}\right)^2 + 4kTR_S \cdot \left(\frac{R_1}{Z_{L_e}}\right)^2}{4kTR_S \cdot \left(\frac{R_1}{Z_{L_e}}\right)^2}$$
(11)

are perfectly cancelled to get a deep notch. In previous experiments, the notch was tuned manually by adjusting the current flowing through the resonator.

Fig. 2(c) shows a master VCO used to perform Q tuning. An automatic amplitude control (AAC) feedback circuit is used to adjust the current in the VCO so that it just barely oscillates. This is the point at which the losses are exactly cancelled. For a filter built with a similar resonator, the same bias applied to it will also exactly balance the losses and the notch will be at its deepest. The AAC loop is similar to that described in [16]. However, in this case the loop sets the VCO amplitude to zero rather than at a level optimal for phase-noise performance. The loop consists of a VCO core, voltage sensing transistors  $Q_3$  and  $Q_4$ , and a capacitor  $C_{\text{FB}}$ .  $C_{\text{FB}}$  sets the dominant pole in the control loop providing stability. The bias of  $Q_3$  and  $Q_4$  represents the only major difference between the loop used here and the one presented in [16]. In this case, they are biased to act as class-B amplifiers that turn on for half the cycle and steal current from the bias circuit. This scales back the current so that oscillations cannot grow significantly beyond zero amplitude. As well, it should be noted that the VCO includes a very small additional fixed capacitor in its resonator so that the VCO does not oscillate at exactly the image frequency. Thus, it is not injecting signal at the very frequency we are trying to remove.

## III. VCO DESIGN

The basic VCO design is a cross-coupled  $-G_m$  topology, as shown in Fig. 2(d). The main difference between this design and traditional designs is that the feedback is provided by a transformer rather than by directly coupling the bases to the collectors or by using capacitors in the feedback path [17]. Decoupling the base from the collector allows the voltage swing to grow larger than 0.8-V peak without forward biasing the collector-base junctions of  $Q_{13}$  and  $Q_{14}$ . Since the transformer is a 2:1 structure, this helps to reduce the swing on the bases of the transistors. Thus, the signal can grow to a larger level than in the case of capacitive decoupling. The transformer has the added advantage that the bias may be provided at the center tap, avoiding the need for RF blocking resistors. The removal of these resistors along with the addition of a capacitor on the bias line keeps the noise injected into the oscillator to a minimum.

The current through the oscillator is limited with the use of a resistor  $R_{E1}$  rather than a current source because the resistor needs much less headroom to accommodate it. As well, the resistor can be less noisy than a standard current source and uses less chip area than a tail filter [18].

To keep the amplitude of the oscillation constant, clamping diodes were placed across the tank, preventing the amplitude from growing beyond about 1.8-V peak [19]. This also keeps noise from causing amplitude fluctuations in the oscillator. These fluctuations would otherwise be modulated by the VCO and upconverted around the carrier, and therefore, converted into phase noise. Note that automatic amplitude control could be used with this VCO and has been demonstrated in [16]; however, this was not included here. Buffers were included in the circuit so that the VCO would have a low output impedance to drive other circuits or test equipment without loading the tank and decreasing its Q.

Previously, linear analysis of oscillators has shown that phase noise (PN), described by Leeson's formula [20], can be expressed as

$$PN \approx \left(\frac{A\omega_o}{(2Q\Delta\omega)}\right)^2 \left(\frac{FkT}{2P_S}\right) \tag{14}$$

where  $\omega_o$  is the frequency of oscillation, Q is the quality factor of the resonator,  $\Delta \omega$  is the offset frequency, A describes the nonlinear effects and is nominally equal to  $\sqrt{2}$  [20], [21], F is the excess noise factor [22], and  $P_s$  is the power at the oscillation frequency. In order to be complete, we must have a way to compute the value of F for the oscillator.

If the transistor and bias were assumed to be noiseless, then the only noise present will be due to the resonator losses and it will have a noise power of kT. The switching transistors and the bias will add noise to this minimum. Considering the bias noise in the case of the  $-G_m$  oscillator, during transitions the transistors  $Q_{13}$  and  $Q_{14}$  act like amplifiers. Thus, collector shot noise  $i_{cn}$  from  $Q_{13}$  and  $Q_{14}$  dominates the noise during this time. When these transistors are completely switched on or off, noise will mainly come from the tail resistor  $R_{E1}$  as well as a reduced amount of noise from the transistors. If  $\rho$  is the fraction of a cycle that the transistors are completely switched and  $i_{nt}$  is the noise current injected into the oscillator from the tail resistor during this time, then the ratio of the total input noise relative to the noise in the case of noiseless transistors and bias is

$$F \approx 1 + \frac{\left(i_{\rm nt}^2 + i_{\rm cnl}^2\right)R_T}{kT}\rho + \frac{i_{\rm cn}^2R_T(1-\rho)}{kT} \qquad (15)$$

where  $R_T$  is the equivalent parallel resistance of the tank,  $i_{cnl}$  is the collector shot noise while the transistors are fully switched on, and  $i_{cn}$  is the collector shot noise during the zero crossings. Note that as the Q of the tank increases,  $R_T$  increases and noise has more gain to the output, therefore increasing F. Also note that to be more accurate this analysis should include a noise sensitivity function such as the one used by [23], but this is omitted here for simplicity and due to the fact that over an oscillation cycle F was found to be almost constant. This is illustrated with a simple ac noise simulation used to illustrate the major sources of noise over the course of a complete oscillation cycle, as shown in Fig. 4. In the plot, the noise produced by the tank loss and the noise produced by other major noise sources is shown. Note that only the transistor noise sources for  $Q_{13}$  have

$$NF_{LNA \text{ with Notch}} \approx \frac{2qI_{\text{sharp}} \cdot \left(\frac{R_1}{N_L}\right)^2 + \frac{2qI_{C1}}{\beta_o} Z_{\text{eq}}^2 \cdot \left(\frac{R_1}{Z_{L_e}}\right)^2 + 2qI_{C1}R_L^2 + 4kTr_b \cdot \left(\frac{R_1}{Z_{L_e}}\right)^2 + 4kTR_S \cdot \left(\frac{R_1}{Z_{L_e}}\right)^2}{4kTR_S \cdot \left(\frac{R_1}{Z_{L_e}}\right)^2}$$
(13)



Fig. 4. Simulation showing noise over a cycle.

been plotted, and the noise due to  $Q_{14}$  would be similar to the ones for  $Q_{13}$ . From inspection of the graph, it can be seen that the noise figure in this case should be approximately 3 dB, as the tank losses and other noise sources are almost equal. Using (14) results in a phase noise prediction of -117 dBc/Hz at 1-MHz offset for the VCO used in this paper.

Note that as well as Leeson's style noise, the VCO must also be optimized to ensure that low-frequency noise is not dominant in the design. In this case, the transformer primary shorts out low-frequency noise on the tank and the clamping diodes prevent amplitude fluctuations. Otherwise, both amplitude fluctuations and low-frequency noise would be upconverted by the varactors [24].

#### IV. MIXER DESIGN

The LNA is coupled into the mixer with the use of another transformer [25]. The 2:1 turns ratio in this case is used to increase the current flowing into the quad transistors, thus, increasing the receiver gain. Bias current is provided through the transformer center tap. A voltage is developed across the collector resistors and output followers (not shown) are used to drive the measurement equipment. Capacitors  $C_L$  are included here to remove high-frequency feedthrough of the RF or LO signals.

## V. TRANSFORMER DESIGN

On-chip transformers in silicon are as yet not very common. They can, however, be extremely useful for low-voltage operation. Transformers are more complicated than inductors and, therefore, harder to model in many cases. A circular symmetric transformer with a turns ratio of 2:1 is shown in Fig. 5(a). This structure is optimal for differential applications because both primary and secondary have a point of symmetry where a bias can be applied without affecting RF performance. Note also that a circular structure will provide the lowest loss, design rules permitting [19]. The actual dimensions of the structure can be optimized much the same as in the case of an inductor with the help of a simulator such as ASITIC [26].

Traditionally, when transformers are measured and characterized,  $S_{21}$  for the device is reported [27]. While correct, this



Fig. 5. Illustration of the use of transformers in RFICs. (a) Drawing of a circular 2:1 transformer. (b) Simplified narrow-band model. (c) Broad-band model.

leaves the circuit designer with little directly applicable information. It would be more useful instead to extract an inductance and Q for both windings and the coupling (k factor) for the structure.

If the Z parameters are extracted from the measured S parameters, one can find the equivalent primary inductance  $L_p$  and equivalent primary loss  $R_p$  using the narrow-band model for the transformer shown in Fig. 5(b) and knowing that

$$Z_{11} = R_p + j\omega L_p. \tag{16}$$

Similarly

$$Z_{22} = R_s + j\omega L_s. \tag{17}$$

Thus, the inductance of the primary and secondary and the primary and secondary single-ended Q can be determined and are shown in the following equations:

$$L_s = \frac{\operatorname{Im}(Z_{22})}{i\omega} \tag{18}$$

$$L_p = \frac{\mathrm{Im}(Z_{11})}{i\omega} \tag{19}$$

$$Q_s = \frac{\text{Im}(Z_{22})}{\text{Re}(Z_{22})}$$
(20)

$$Q_p = \frac{\mathrm{Im}(Z_{11})}{\mathrm{Re}(Z_{11})}.$$
 (21)

The mutual inductance can also be extracted, as follows:

$$M = \frac{Z_{12}}{j\omega} = \frac{Z_{21}}{j\omega}.$$
 (22)

Additionally, the measured data can be used to fit a broad-band model such as the one shown in Fig. 5(c). It is modeled as two inductors, but with the addition of coupling coefficient k between them, and interwinding capacitance  $C_{\rm IW}$  from input to output. Also, the inductors are broken in two so that the center tap for biasing both the primary and secondary can be included. Normally, test structures are measured as two-port structures with the other two ports grounded. Thus, the primary and secondary would each have one terminal grounded, and if the device is



Fig. 6. Photomicrograph of the 5-GHz receiver.

assumed to be symmetric, then this is sufficient to extract the transformer model.

## VI. RESULTS

The entire receiver was fabricated in a 75-GHz SiGe bipolar process that featured a 3- $\mu$ m-thick top-level aluminum metal approximately 5  $\mu$ m from the Si substrate. The chip measured  $1.2 \text{ mm} \times 1.8 \text{ mm}$ . A die photo is shown in Fig. 6. The chip drew 21.6 mA from a 1.8-V supply excluding IF buffers. The RF passband was centered at 5.1 GHz with a gain of 19.8 dB. Thus, with a minimum attenuation of 39 dB in the stopband, this provides the receiver with a minimum image rejection of 59 dB. The noise figure of the receiver was 4.5 dB. This was slightly worsened due to the presence of the notch circuitry in the LNA, mainly due to collector shot noise of  $Q_5$  and  $Q_6$ . Simulations showed that the notch circuitry added about 1 dB to the system noise figure. The linearity was also measured and the receiver had a third-order input intercept point (IIP3) of -11.5dBm and a 1-dB compression point of -21.1 dBm, which is reasonable for applications such as WLAN. Port-to-port isolation was good and is summarized in Table I with other receiver parameters. Note that due to the transformer terminals being inadvertently swapped in the simulation, the notch frequency was higher than intended (nominally, the LO was intended to operate at 6 GHz, and image was to be at 7 GHz) so the notch frequency tuning range does not line up with the image frequency even at the highest frequency the VCO can operate, which was only 5.6 GHz due to parasitic loading.

The transformer used in the receiver was characterized as a test structure in order to create a model to use in the receiver design. The k factor for the transformer was 0.54 at 5 GHz. Fig. 7 shows the inductance and Q for the primary and secondary windings. As can be seen from the plot, the Q of the primary is about 10 at the frequency of interest, and the Q of the secondary are about 1.7 and 0.7 nH, respectively, at 5.5 GHz. Thus, the structure geometry has been optimized so that its Q is highest in the 5-GHz frequency band of interest.

The VCO by itself drew 2.78 mA from a nominal power supply of 1.8 V. The circuit had a 600-MHz tuning range or

TABLE I SUMMARY OF RECEIVER PERFORMANCE

| Parameter             | Performance              |  |
|-----------------------|--------------------------|--|
| Supply Voltage        | 1.8V                     |  |
| Current               | 21.6mA                   |  |
| Power Consumption     | 38.9mW                   |  |
| Image Rejection       | > 59dB                   |  |
| Conversion Gain       | 19.8dB                   |  |
| 1dB Compression Point | -21.1dBm                 |  |
| IIP3                  | -11.5dBm                 |  |
| RF Frequency          | 5.1GHz                   |  |
| VCO Tuning Range      | 5.1-5.6GHz               |  |
| Notch Tuning Range    | 8.2-8.6GHz               |  |
| LO-RF Isolation       | >60dB                    |  |
| LO-IF Isolation       | > 50dB                   |  |
| RF-IF Isolation       | > 50dB                   |  |
| VCO Phase Noise       | -116dBc/Hz @ 1MHz offset |  |
| Noise Figure          | 4.5dB                    |  |



Fig. 7. Inductance and Q for the coils of the transformer.

about 12%. Measured phase noise was -116 dBc/Hz at 1-MHz offset. A plot of the phase noise is shown in Fig. 8. This is extremely close to the predicted value. The VCO is also compared with designs presented in the literature, and Table II shows that the figure of merit (FOM) of this design is good compared with other published results.

The filter was also tested by itself, without the rest of the receiver. The circuit showed very good attenuation in the stopband between 39 and 47 dB. In this case, unlike previous circuits, no manual adjustment of the current was required to maintain the image rejection across the band. A plot of the filter response is shown in Fig. 9. The notch was tunable between 8.2 and 8.6 GHz. A plot showing the voltage that can be tolerated by the filter before it starts to lose image rejection is shown in Fig. 10. From this figure it can be seen that, for a voltage larger

| Reference | Supply   | Frequency | Current | Tuning Range  | Phase Noise (offset)  | FOM   |
|-----------|----------|-----------|---------|---------------|-----------------------|-------|
| [17]      | 2.7V     | 2GHz      | 12mA    | 150MHz (7.5%) | -102dBc/Hz (100kHz)   | 172.9 |
| [19]      | 2.6-2.8V | 4.4GHz    | 4mA     | 260MHz (6%)   | -100.2dBc/Hz (100kHz) | 170.9 |
| [16]      | 3.3V     | 2.4GHz    | 4mA     | 600MHz (25%)  | -99 dBc/Hz (100kHz)   | 175.4 |
| [28]      | 3.3V     | 2GHz      | 5.5mA   | 120MHz (6%)   | -106dBc/Hz (100kHz)   | 179.4 |
| [29]      | 5V       | 20GHz     | 10mA    | 3GHz (15%)    | -101dBc/Hz (1MHz)     | 170   |
| [30]      | 2V       | 2.5GHz    | 7mA     | 500MHz (20%)  | -104 dBc/Hz (100kHz)  | 180.4 |
| [31]      | 1.8V     | 6GHz      | 1.8mA   | 300MHz (5%)   | -106dBc/Hz (1MHz)     | 176   |
| This Work | 1.8V     | 5.5GHz    | 2.8mA   | 500MHz (9%)   | -116dBc/Hz (1MHz)     | 184   |

TABLE II COMPARISON OF VCO PERFORMANCE



Fig. 8. VCO phase noise at 1-MHz offset. Note the plot is done at a resolution bandwidth of 30 kHz.



Fig. 9. Plot of the filter response.

than about 95 mV, image rejection degrades. This voltage appears directly on  $L_{p1}$  in Fig. 2(b) and is then transformed down to about 42.5 mV on  $L_{s1}$ . Therefore, each transistor  $Q_5$  and  $Q_6$  of Fig. 2(b) sees about 21 mV<sub>rms</sub> or about 30 mV<sub>peak</sub>. This agrees with the earlier discussion of linearity.

## VII. CONCLUSION

The design of a 5-GHz radio receiver front-end using a 1.8-V supply in a 75-GHz SiGe technology has been presented with



Fig. 10. Plot of the image rejection versus input signal voltage.

4.5-dB noise figure and an IIP3 of -11.5 dBm. The receiver featured a notch filter with automatic Q tuning, integrated with the LNA to provide image rejection greater than 59 dB across its frequency band of operation. Noise, linearity, and stability of the filter have been considered. Design considerations achieving a VCO with a phase noise of -116 dBc/Hz at 1-MHz offset were also discussed in detail. Circular transformers were used, which offered advantages for the notch filter performance and allowed for better low-voltage operation of the VCO and mixer.

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#### REFERENCES

- R. Schaumann, M. S. Ghausi, and K. R. Laker, *Desgin of Analog Filters: Passive, Active RC, and Switched Capacitor.* Englewood Cliffs, NJ: Prentice-Hall, 1990.
- [2] A. B. Williams and F. J. Taylor, *Electronic Filter Design Handbook: LC, Active, and Digital Filters*. Boston, MA: McGraw-Hill, 1988.
- [3] T. Yoshimasu, K. Sakuno, N. Matsumoto, E. Suematsu, T. Tsukao, and T. Tomita, "A low-current Ku-band monolithic image rejection downconverter," *IEEE J. Solid-State Circuits*, vol. 27, pp. 1448–1451, Oct. 1992.
- [4] D. Li and Y. Tsividis, "Design techniques for automatically tuned integrated gigahertz-range active *LC* filters," *IEEE J. Solid-State Circuits*, vol. 37, pp. 967–977, Aug. 2002.
- [5] C. Guo, C. Lo, Y. Choi, I. Hsu, T. Kan, D. Leung, A. Chan, and H. C. Luong, "A fully integrated 900-MHz CMOS wireless receiver with on-chip RF and IF filters and 79-dB image rejection," *IEEE J. Solid-State Circuits*, vol. 37, pp. 1084–1089, Aug. 2002.

- [6] T. Soorapanth and S. S. Wong, "A 0- dB IL 2140±30 MHz bandpass filter utilizing *Q*-enhanced spiral inductors in standard CMOS," *IEEE J. Solid-State Circuits*, vol. 37, pp. 579–586, May 2002.
- [7] S. Pipilos, Y. Tsividis, and J. Fenk, "1.8-GHz tunable filter in Si technology," in *Proc. IEEE Custom Integrated Circuits Conf.*, May 1996, pp. 189–191.
- [8] S. Pavan and Y. Tsividis, *High Frequency Continuous Time Filters in Digital CMOS Processes*. Norwell, MA: Kluwer, 2000.
- [9] S. D. Willingham and K. Martin, *Integrated Video-Frequency Contin*uous-Time Filters. Norwell, MA: Kluwer, 1995.
- [10] J. Macedo and M. A. Copeland, "A 1.9-GHz silicon receiver with monolithic image filtering," *IEEE J. Solid-State Circuits*, vol. 33, pp. 378–386, Mar. 1998.
- [11] M. A. Copeland, S. P. Voinigescu, D. Marchesan, P. Popescu, and M. C. Maliepaard, "5-GHz SiGe HBT monolithic radio transceiver with tunable filtering," *IEEE Trans. Microwave Theory Tech.*, vol. 48, pp. 170–181, Feb. 2000.
- [12] J. W. M. Rogers, J. Macedo, and C. Plett, "A completely integrated 1.9-GHz receiver front-end with monolithic image-reject filter and VCO," *IEEE Trans. Microwave Theory Tech.*, vol. 50, pp. 210–215, Jan. 2002.
- [13] H. Samavati, H. R. Rategh, and T. H. Lee, "A 5-GHz CMOS wireless LAN receiver front end," *IEEE J. Solid-State Circuits*, vol. 35, pp. 765–772, May 2000.
- [14] J. W. M. Rogers and C. Plett, "A completely integrated 1.8-V 5-GHz tunable image-reject notch filter," in *Proc. Radio Frequency Integrated Circuits Symp.*, May 2001, pp. 75–78.
- [15] B. Razavi, *RF Microelectronics*. Englewood Cliffs, NJ: Prentice-Hall, 1998.
- [16] J. W. M. Rogers, D. Rahn, and C. Plett, "A study of digital and analog automatic-amplitude control circuitry for voltage-controlled oscillators," *IEEE J. Solid-State Circuits*, vol. 38, pp. 352–356, Feb. 2003.
- [17] M. Zannoth, B. Kolb, J. Fenk, and R. Weigel, "A fully integrated VCO at 2 GHz," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1982–1991, Dec. 1998.
- [18] E. Hegazi, H. Sjoland, and A. Abidi, "A filtering technique to lower *LC* oscillator phase noise," *IEEE J. Solid-State Circuits*, vol. 36, pp. 1921–1930, Dec. 2001.
- [19] A. M. Niknejad, J. L. Tham, and R. G. Meyer, "Fully integrated low phase noise bipolar differential VCOs at 2.9 and 4.4 GHz," in *Proc. 25th Eur. Solid-State Circuits Conf.*, 1999, pp. 198–201.
- [20] B. Razavi, "A study of phase noise in CMOS oscillators," *IEEE J. Solid-State Circuits*, vol. 31, pp. 331–343, Mar. 1996.
- [21] J. W. M. Rogers and C. Plett, *Radio Frequency Integrated Circuit Design*. Norwood, MA: Artech House, 2003.
- [22] J. Rael and A. Abidi, "Physical processes of phase noise in differential *LC* oscillators," in *Proc. IEEE Custom Integrated Circuits Conf.*, June 2000, pp. 569–572.
- [23] T. H. Lee, The Design of CMOS Radio Frequency Integrated Circuits. Cambridge, U.K.: Cambridge Univ. Press, 1998.
- [24] J. W. M. Rogers, J. A. Macedo, and C. Plett, "The effect of varactor nonlinearity on the phase noise of completely integrated VCOs," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1360–1367, Sept. 2000.
- [25] J. R. Long, "A low-voltage 5.1–5.8 GHz image-reject downconverter RFIC," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1320–1328, Sept. 2000.
- [26] A. M. Niknejad and R. G. Meyer, "Analysis, design, and optimization of spiral inductors and transformers for Si RF IC's," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1470–1481, Oct. 1998.
- [27] J. Long, "Monlithic transformers for silicon RF IC design," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1368–13, Sept. 2000.
- [28] J. W. M. Rogers, V. Levenets, C. A. Pawlowicz, N. G. Tarr, T. J. Smy, and C. Plett, "Post-processed Cu inductors with application to a completely integrated 2-GHz VCO," *IEEE Trans. Electron Devices*, vol. 48, pp. 1284–1287, June 2001.
- [29] S. P. Voinigescu, D. Marchesan, and M. A. Copeland, "A family of monolithic inductor-varactor SiGe-HBT VCO's for 20 GHz to 30 GHz LMDS and fiber-optic receiver applications," in *Proc. Radio Frequency Integrated Circuits Symp.*, June 2000, pp. 173–176.

- [30] A. Zanchi, C. Samori, S. Levantino, and A. Lacaita, "A 2 V 2.5 GHz 104 dBc/Hz at 100 kHz fully integrated VCO with wide-band low-noise automatic amplitude control loop," *IEEE J. Solid-State Circuits*, vol. 36, pp. 611–619, Apr. 2001.
- [31] H. Shin, Z. Xu, and M. Chang, "A 1.8-V 6/9-GHz switchable dual-band quadrature LC VCO in SiGe BiCMOS technology," in Proc. Radio Frequency Integrated Circuits Symp., June 2002, pp. 71–74.



John W. M. Rogers (M'95) was born in Cobourg, ON, Canada in 1974. He received the B.Eng. degree in 1997, the M.Eng. degree in 1999, and the Ph.D. degree in 2002, all in electrical engineering, from Carleton University, Ottawa, ON, Canada.

During his Master's degree research, he was a resident researcher at Nortel Network Advanced Technology Access and Applications Group, where he did exploratory work on VCOs and developed a copper interconnect technology for building high-quality passives for RF applications. From

2000 to 2002, he was with SiGe Semiconductor Ltd. while working towards his Ph.D. degree on low-voltage radio-frequency integrated circuits for wireless applications. Concurrent with his Ph.D. research, he worked as part of a design team that developed a cable modem IC for the DOCSIS standard. He is currently an Assistant Professor with Carleton University and collaborating with Cognio Canada Ltd., Ottawa. He is a coauthor of *Radio Frequency Integrated Circuit Design* (Norwood, MA: Artech House, 2003). He holds one U.S. patent with four pending. His research interests are in the areas of radio-frequency integrated circuit design for wireless and broad-band applications.

Dr. Rogers was a recipient of an IEEE Solid-State Circuits Predoctoral Fellowship and received the BCTM Best Student Paper Award in 1999. He is a member of the Professional Engineers of Ontario.



**Calvin Plett** (M'91) received the B.A.Sc. degree in electrical engineering from the University of Waterloo, Waterloo, ON, Canada, in 1982 and the M.Eng. and Ph.D. degrees from Carleton University, Ottawa, ON, Canada, in 1986 and 1991, respectively.

Prior to 1982, he worked for a number of companies, including nearly four years with Atomic Energy of Canada. From 1982 to 1984, he worked with Bell-Northern Research doing analog circuit design. In 1989, he joined the Department of Electronics, Carleton University, where he is now an Associate

Professor. For some years, he did consulting work for Nortel Networks in radio-frequency integrated circuit design. Recently, he has been involved in collaborative research which involved numerous graduate and undergraduate students and various companies including Nortel Networks, SiGe Semiconductor, Philsar, Conexant, Skyworks, and IBM. He has authored or coauthored more than 40 technical papers which have appeared in international journals and conferences. He is a coauthor of the book *Radio Frequency Integrated Circuit Design* (Norwood, MA: Artech House, 2003). His research interests include the design of analog and radio-frequency integrated circuits, including filter design, and communications applications.

Dr. Plett is a member of AES and PEO. He has been the faculty advisor to the student branch of the IEEE at Carleton University for about ten years. He was a coauthor of papers that won the Best Student Paper Awards at the 1999 Bipolar/BiCMOS Circuits and Technology Meeting and at the 2002 Radio Frequency Integrated Circuits Symposium.