A 50.1-Gb/s 60-GHz CMOS Transceiver for IEEE 802.11ay With Calibration of LO Feedthrough and I/Q Imbalance

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***Abstract*— This paper presents a 60-GHz CMOS transceiver targeting the IEEE 802.11ay standard. A calibration block for local oscillator feedthrough (LOFT) and I/Q imbalance featuring high accuracy and low power consumption is integrated with the transceiver. With the help of the proposed calibration, this paper is capable of boosting the data rate with higher order modulation scheme and wider channel-bonding bandwidth, which are demanded by IEEE 802.11ay. At the same time, it maintains the compatibility with the existing IEEE 802.11ad standard. This paper reports a two-channel-bonding data rate of 24.64 Gb/s in 128 quadrature amplitude modulation (QAM). The corresponding TX-to-RX error vector magnitude (EVM) is −26.1 dB. Furthermore, a four-channel-bonding data rate of 42.24 Gb/s in 64 QAM is realized with a single-element transceiver. The measured maximum data rate is 50.1 Gb/s in 64 QAM, which is the highest data rate achieved in the 60-GHz band. The power consumption is only 169 mW in the transmitting mode and 139 mW in the receiving mode.**

***Index Terms*— 128 quadrature amplitude modulation (QAM), 60 GHz, calibration, CMOS, four-channel bonding, I/Q imbalance, local oscillator feedthrough (LOFT), transceiver.**

I. Introduction

THE utilization of the millimeter-wave spectrum significantly boosts the achievable data rate. With the 2.16-GHz channels in the 60-GHz band defined in IEEE 802.11ad/WiGig, up to 7-Gb/s wireless data communication has already been realized. However, the rapid growth of data traffic in human society demands a much higher wireless communication speed in the not far future. To satisfy the future data transmission capacity, IEEE 802.11ay is the standard to additionally extend the data rate to over 28 Gb/s. Fig. 1 shows the channels defined in IEEE 802.11ay. A channel-bonding technique is applied to broaden the available signal bandwidth. A data rate of 42.24 Gb/s can be realized considering a 64 quadrature amplitude modulation (QAM) four-channel bonding. Besides the channel-bonding technique, a higher order modulation scheme like 128 QAM is always desirable to further increase the spectrum efficiency.

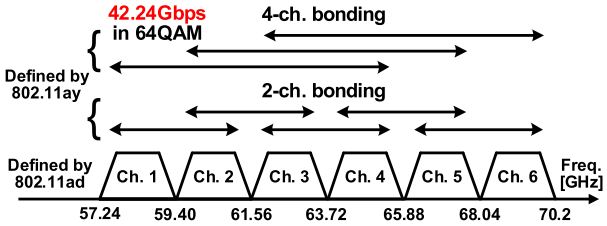

Fig. 1. Channels defined by IEEE 802.11ad/WiGig and IEEE 802.11ay.

Efforts have been concentrated on realizing 60-GHz CMOS transceivers with extremely high data rate during the past few years [1]–[15]. Recent research includes a transceiver implementation utilizing a dual-polarized multiple-in and multiple-out (DP-MIMO) technique [3]. The 27.8 Gb/s in 16 QAM is achieved by doubling the data rate in a single-polarization stream. Also, A frequency-interleaved (FI) transceiver is reported in [6]. The primary purpose is to relieve the error vector magnitude (EVM) requirement for a single-element transceiver. A four-channel-bonding data rate of 42.24 Gb/s is realized with two transceiver elements. However, both two works mentioned above suffer from large power consumption due to an additional front-end element. Furthermore, two other 7.04-GS/s analog-to-digital converters (ADCs) will be required at the baseband, which makes

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		IEEE 802.11ad	IEEE 802.11ay	
Standard	Channel Bandwidth	2.16GHz	1-ch.: 2.16GHz 2-bonded ch.: 4.32GHz 4-bonded ch.: 8.64GHz	
	Modulation (SC)	16QAM (MCS20)	64QAM* (MCS17)	128QAM*
	TX EVM (SC)	-19.0dB	-24.0dB*	-*
Design Target	TX-to-RX EVM (SC)**	-16.5dB	-22.5dB	-25.5dB
	LOFT Supp.	-26.5dB	-32.5dB	-35.5dB
	IMRR	-26.5dB F_{BB}< 0.88GHz	-32.5dB F_{BB}<0.88GHz(1-ch.) F_{BB}<1.76GHz(2-ch.) F_{BB}<3.52GHz(4-ch.)	-35.5dB F_{BB}<0.88GHz(1-ch.) F_{BB}<1.76GHz(2-ch.) F_{BB}<3.52GHz(4-ch.)
	I/Q Mag. Mismatch	< 0.8dB	< 0.4dB	< 0.3dB
	I/Q Phase Mismatch	< 5°	< 3°	< 2°
	Phase Noise (OFDM)	16QAM: -90dBc/Hz @1MHz	64QAM: -96 dBc/Hz@1MHz 128QAM: -99 dBc/Hz@1MHz	

* Modulation schemes and required EVMs for IEEE 802.11ay are still under discussion
** TX-to-RX EVM is defined with BER of 10^{-3} and is equal to –SNR (MER).

Fig. 2. Summary of requirement and design target for IEEE 802.11ad/ay.

the architectures even more power hungry. Although realizing the four-channel bonding with a single-element transceiver requires a 14.08-GS/s time-interleaved ADC, a power consumption of 69.5 mW for a 20-GS/s 6-bit ADC is still reasonable considering the whole system power budget [16].

Due to the system simplicity, direct-conversion architecture is attractive for achieving compact and low-power 60-GHz transceivers [1], [4], [6], [14], [17]–[20]. However, such a kind of transceiver suffers terribly from the local oscillator feedthrough (LOFT) and I/Q imbalance. Thus, to improve the yields, an on-chip calibration block for LOFT suppression and image rejection ratio (IMRR) is usually essential [1], [21]. Saito *et al.* [1] introduces a transceiver chipset developed for IEEE 802.11ad with a built-in self-calibration circuit. The LOFT suppression and IMRR in [1] are calibrated by reusing the 5-bit 3.52-GS/s baseband ADCs, whereas applying the same calibration method to an IEEE 802.11ay transceiver will result in severe inaccuracy and even higher power consumption. Therefore, calibration circuits designed for IEEE 802.11ay demands an accuracy improvement along with a small enough power and area overhead.

This paper introduces a 60-GHz CMOS transceiver designed for IEEE 802.11ad/ay. The maximum single-carrier (SC) mode data rate of 50.1 Gb/s is realized with 8.35-GSymbol/s symbol rate in 64 QAM. The data rate is boosted from the dimensions of higher order modulation schemes and broader signal bandwidth. A compact calibration block featuring high accuracy and low power consumption for LOFT and I/Q imbalance is presented. Thanks to the suppressed impairments by the proposed calibration, the transceiver realizes a data rate of 24.64 Gb/s in 128 QAM with a TX-to-RX EVM of −26.1 dB even though 128 QAM is not planned in IEEE 802.11ad. A four-channel-bonding raw data rate of 42.24 Gb/s is also achieved by the calibrated transceiver.

The rest of this paper is structured as follows. Section II will explain the requirements from IEEE 802.11ay on some critical transceiver design parameters. The calibration architecture considerations will also be included in Section II. Section III will introduce the specific circuit schematics of the transceiver. Section IV will present the measurement results

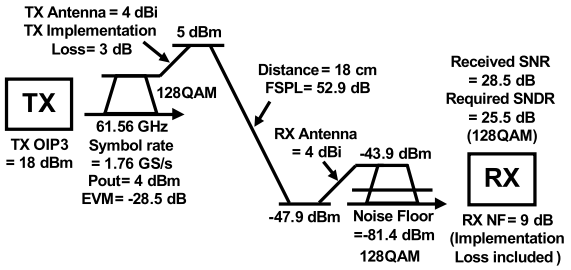


Fig. 3. Link budget for a data transmission in 128 QAM.

of the transceiver after the proposed automatic calibration scheme. Finally, a conclusion will be drawn in Section V.

II. Requirements and Architecture Considerations

Compared with the existing IEEE 802.11ad standard, the outcoming IEEE 802.11ay standard demands a much more stringent EVM requirement. As it is known to us, the EVM of a transceiver $\mathrm{EVM_{TRX}}$ can be evaluated with the following equation [22]:

$$\mathrm{EVM_{TRX}} \approx \sqrt{\frac{1}{\mathrm{SNDR}^2} + \varphi^2{}_{\mathrm{rms}} + \mathrm{EVM}^2_{\mathrm{LOFT}} + \mathrm{EVM}^2_{\mathrm{Image}} + \mathrm{EVM}^2_{\mathrm{Flat}}} \quad (1)$$

where SNDR represents the signal-to-noise-and-distortion ratio and $\varphi^2{}_{\mathrm{rms}}$ stands for the integrated double-sideband (DSB) phase noise of the carrier. $\mathrm{EVM_{LOFT}}$, $\mathrm{EVM_{Image}}$, and $\mathrm{EVM_{Flat}}$ denote the EVMs caused by the LOFT, the I/Q imbalance, and the in-band gain response variation. Fig. 2 summarizes the requirement from IEEE 802.11ad/ay and the design target in this paper. The detailed design considerations will be explained in the remaining part of this section.

Facing the increased signal bandwidth in IEEE 802.11ay, the input noise level for an IEEE 802.11ay application can be 6 dB higher than an IEEE 802.11ad one. Thus, the SNDR optimization of a transceiver becomes essential within a limited power budget. In addition, the increased bandwidth also puts more pressures on the gain flatness of an SC transceiver. A 2.8-dB gain variation within the 8.64-GHz bandwidth can lead to a −16.5-dB $\mathrm{EVM_{Flat}}$ [22], which severely limits the overall EVM. Although the utilization of an equalizer at the receiver side can minimize the gain variation, a flat frequency response is still desirable for a wideband transceiver.

Besides the channel-bonding technique, higher order modulation schemes such as 64 QAM or 128 QAM are also considered to increase the data rate in IEEE 802.11ay. A link budget example is shown in Fig. 3. The data communication in 128 QAM with a one-channel bandwidth can be supported in a maximum communication distance of 18 cm. The increased modulation order in IEEE 802.11ay will demand a lower phase noise of the RF phase-locked loop (PLL). Usually, the usage of the baseband carrier tracking circuit can suppress the influence of phase noise. For an IEEE 802.11ay transceiver in the orthogonal frequency division multiplexing (OFDM) mode the phase noises of −96 and −99 dBc/Hz at 1-MHz

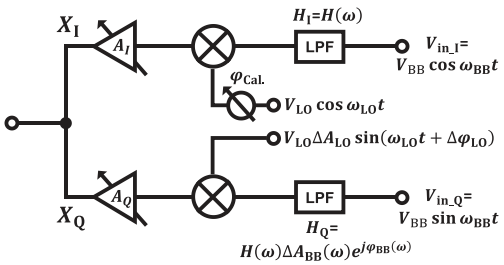


Fig. 4. I/Q imbalance and RF domain compensation for the direct-conversion transceiver.

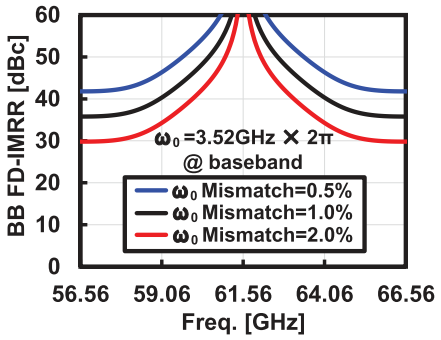


Fig. 5. Simulated FD-IMRR with different I/Q cutoff frequency mismatch.

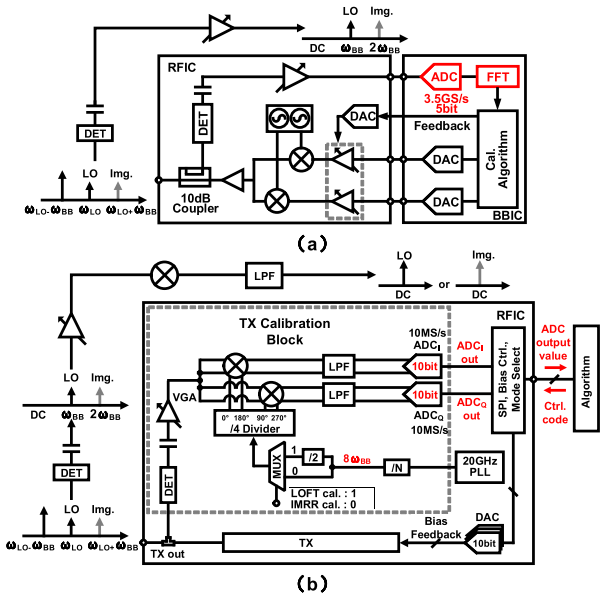


Fig. 6. Block diagrams of (a) traditional calibration method for LOFT and image calibration and (b) proposed calibration method.

offset, with a 400-kHz carrier tracking bandwidth, will be required for 64 QAM and 128 QAM, respectively [23]. On the other hand, the phase noise requirement for the SC mode can be relaxed due to the wider carrier tracking bandwidth.

The IEEE 802.11ay standard also demands a much more rigorous level for the in-band LOFT suppression and IMRR. Both the LOFT suppression and IMRR should be higher than 32.5 dB for 64 QAM and 35.5 dB for 128 QAM within the signal bandwidth. The I/Q magnitude mismatches of less than 0.4 and 0.3 dB along with the I/Q phase mismatches of less than 3° and 2° are required for 64 QAM and 128 QAM, respectively. Circuits supporting such high-resolution magnitude and phase tuning will be required to compensate the I/Q imbalance. Usually, the I/Q imbalance of a receiver can be compensated by the digital signal processing (DSP) circuit [24], [25], while for the transmitter, a stand-alone block for detection and calibration is required. For saving power, an RF domain calibration is usually adopted to calibrate the I/Q imbalance [4]. Fig. 4 shows the I/Q imbalance in a transceiver and the corresponding RF domain compensation. From Fig. 4, the IMRR can be calculated by comparing the magnitudes of the $(\omega_{LO}-\omega_{BB})$ and $(\omega_{LO}+\omega_{BB})$ components

$$|\text{IMRR}| = \left|\frac{A_I^2+\Delta A^2 A_Q^2+2\Delta A A_I A_Q\cos(\Delta\varphi-\Delta\varphi_{cal})}{A_I^2+\Delta A^2 A_Q^2-2\Delta A A_I A_Q\cos(\Delta\varphi-\Delta\varphi_{cal})}\right|. \quad (2)$$

In (2), $\Delta A(\omega)=\Delta A_{LO}\Delta A_{BB}(\omega)$ is the I/Q magnitude mismatch from the baseband and the local oscillator (LO), while $\Delta\varphi(\omega)=\Delta\varphi_{LO}+\Delta\varphi_{BB}(\omega)$ is the I/Q phase mismatch. A_I, A_Q, and $\Delta\varphi_{cal}$ represent the magnitude and phase calibration parameters from the calibration circuit. By selecting A_I, A_Q, and φ_{cal} properly, the I/Q imbalance can be compensated at an RF frequency of $(\omega_{LO}-\omega_{BB})$. However, the calibrated IMRR will degrade rapidly when approaching the passband edge of the baseband low-pass filter (LPF). The main reason for the degradation is because of the frequency-dependent (FD) I/Q imbalance caused by the mismatch between an I-path LPF and a Q-path LPF [26]. Fig. 5 demonstrates the simulated FD-IMRR with a mismatched cutoff frequency ω_0 between the I- and Q-path LPFs. Regarding the degraded IMRR from the baseband, even more margins should be included in an RF domain calibration circuit. A larger than 50-dBc detection accuracy will be required for achieving 64 QAM and 128 QAM, which corresponding to a more than 50-dBc detection path sensitivity and a more than 9-bit detection ADC. Fig. 5 also shows that the calibration frequency for an RF domain compensation should be selected near the carrier frequency because of the low enough influence from the baseband FD I/Q imbalance there. Usually, the cutoff frequency ω_0 mismatch will depend on the layout. Regarding a severe ω_0 mismatch, the overall EVM will be influenced by the image signal. I/Q compensation techniques [27] at the baseband should be considered.

Fig. 6(a) shows the traditional calibration method for LOFT and I/Q imbalance calibrations [1]. In [1], the LOFT and image signal after detection are directly processed by the ADC and the fast Fourier transformer (FFT) circuit. A 5-bit baseband ADC for the I/Q demodulation is reused due to power saving. Although the traditional method includes an FD-IMRR calibration, poor resolution of the ADC still leads to a severe calibration inaccuracy. Accuracy improvement in the traditional approach can be realized with a higher resolution detection ADC. However, the cost is the increased power consumption and on-chip area. Fig. 6(b) shows the proposed calibration method. In this paper, a small portion of the TX

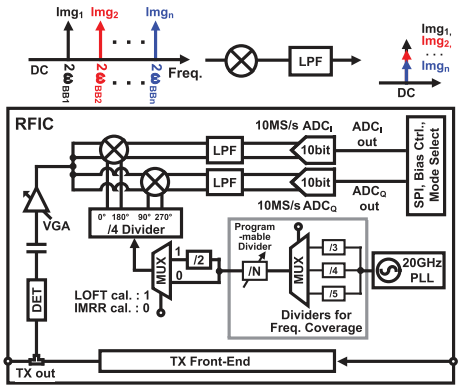


Fig. 7. Extension of the proposed calibration method for the FD-IMRR detection.

output will be coupled to the input of the detector. If a baseband test-tone signal with a frequency of ω_{BB} is assumed, LOFT and image signal frequencies will be detected at ω_{BB} and $2\omega_{BB}$. Different from the traditional method, the detected LOFT and image signal will be downconverted to dc by an area-efficient quad-phase mixer. Thus, two 10-bit, 10-MS/s successive approximation (SAR) ADCs can be utilized for a quick and accurate calibration. Compared with the 67-mW ADC and the power-hungry FFT logic circuit utilized in the traditional method [1], the calibration block in this paper only consumes 3.1 mW and 0.2-mm^2 area. Power-efficient and high-accuracy calibration is realized with a compact chip size.

Moreover, the proposed calibration method can also be applied for the FD-IMRR calibration. The block diagram of the FD-IMRR calibration is shown in Fig. 7. With a series of frequency dividers for covering the required calibration LO frequencies, the proposed circuit can support the baseband frequency sweep. FD-IMRR due to the baseband cutoff frequency mismatch can be compensated by the capacitance tuning [1]. In this condition, a wide operating bandwidth will be required for the detector. Regarding the potentially degraded frequency response of the detector, the noise figure (NF) of the calibration path can be improved by applying a preamplifier before the detector.

III. Circuit Implementation

Fig. 8 shows the topology of the proposed direct-conversion 60-GHz transceiver. The transmitter in this paper consists of a five-stage power amplifier (PA), I/Q RF variable gain amplifiers (VGAs), and I/Q double-balanced passive mixers. The receiver consists of a five-stage low noise amplifier (LNA), I/Q RF VGAs, I/Q double-balanced active mixers, and I/Q baseband amplifiers. The transceiver design in this paper mainly focuses on channel 1–channel 4 defined in IEEE802.11ay. The LO generation in this paper is realized by a quadrature injection-locked oscillator (QILO) with injection from a 20-GHz sub-sampling PLL [23]. The LO chain is capable of generating every required carrier frequencies including the channel bonding. To minimize the LOFT and I/Q imbalance of the transmitter, a calibration block mentioned in Section II is integrated with the transceiver.

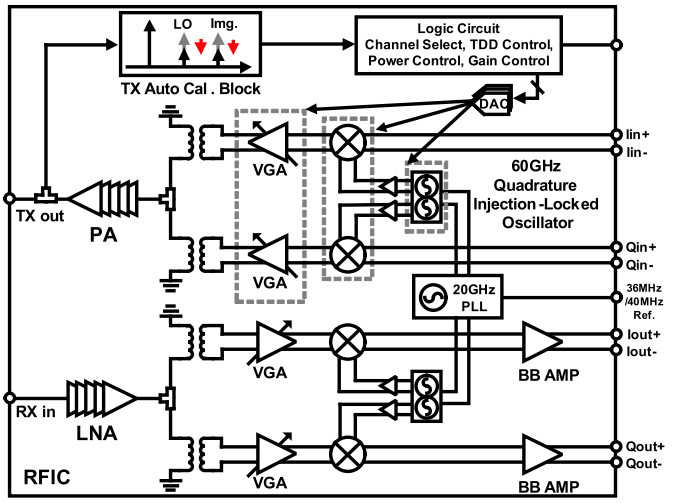


Fig. 8. Block diagram of the proposed 60-GHz transceiver.

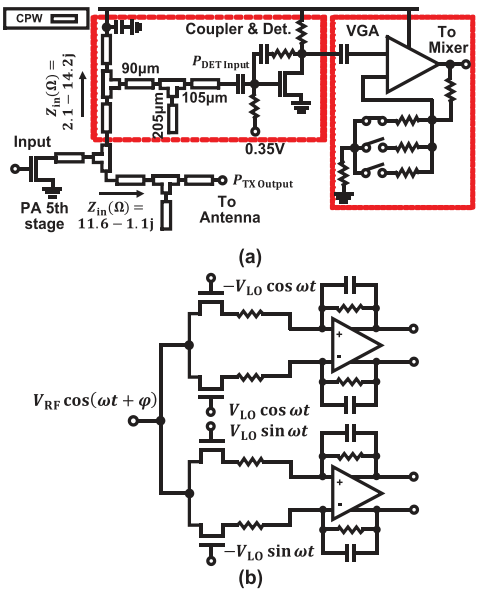


Fig. 9. Circuit schematic of (a) coupler, detector, and VGA, and (b) quad-phase mixer and LPF.

A. Calibration Block

Fig. 9(a) shows the circuit schematics for the coupler, detector, and VGA in the calibration path. Conventional couplers for detection usually utilize the quarter-wavelength coupled-line architecture [1], [28]. However, such couplers suffer from high insertion loss at RF path, which will significantly degrade the linearity performance of the TX. In addition, large on-chip area will be consumed by the quarter-wavelength lines. In this paper, an area-efficient coupler based on the coplanar waveguide (CPW) is adopted. Instead of the lossy quarter-wavelength lines, the coupling in this paper is realized by the shunt CPW stub matching. The power is splitted at the branch point. After the following matching networks for the antenna side and the coupler side, the power of $P_{TX_{Output}}$ and $P_{DET_{Input}}$ will be delivered to the detector and the output of the TX, respectively. The simulated coupling ratio and the insertion loss for PA are shown in Fig. 10. Within a frequency

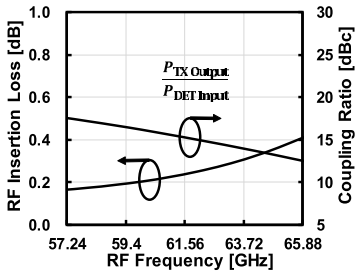


Fig. 10. Simulated coupling ratio and RF path insertion loss of the proposed coupler.

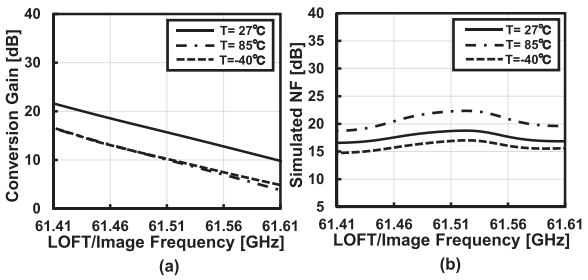


Fig. 11. Simulated (a) conversion gain and (b) NF of the proposed calibration block against the input impairment frequency of the TX.

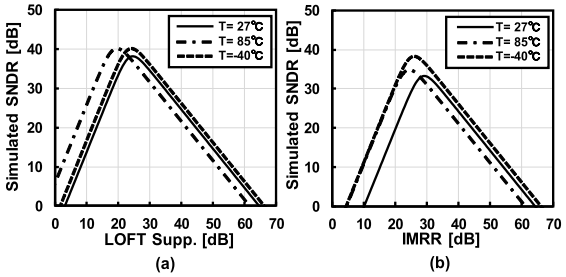


Fig. 12. Simulated SNDR of the calibration path against. (a) LOFT suppression. (b) IMRR.

range of 57.24–65.88 GHz, the insertion loss for TX is always less than 0.42 dB with a coupling ratio of larger than 17.5 dBc. The required area for this coupler is only 0.025 mm^2.

The detector circuit used in this paper is based on a diode-connected transistor. A 0.35-V bias is chosen to achieve the highest second-order output. The VGA circuit is realized with a non-inverting amplifier. A dc block is inserted between the detector and VGA to filter out the dc component generated by self-mixing. The signal output from the VGA will be sent to a mixer for downconversion.

Fig. 9(b) shows the circuit schematic of the downconversion mixer together with the first-order LPF. The 3-dB bandwidth of the LPF is designed to be 316 kHz, which only allows the dc component transferred to ADC. Due to the random phase of the input signal, utilizing a single-phase LO for the downconversion will lead to a time-variant dc level. As a result, a quad-phase downconversion is adopted in this paper to minimize the SNR degradation in the calibration path. If a mixer input signal of $V_{\mathrm{RF}}\cos(\omega t+\varphi)$ and a quad-phase LO are assumed, the detected signal strength can be derived from the I/Q output voltages

$$\begin{aligned}\text{Signal Strength} &= \sqrt{V_{\mathrm{out\_I}}^2+V_{\mathrm{out\_Q}}^2}\\ &= 2V_{\mathrm{LO}}V_{\mathrm{RF}}\sqrt{\sin\varphi^2+\cos\varphi^2}=2V_{\mathrm{LO}}V_{\mathrm{RF}}. \quad (3)\end{aligned}$$

It can be found from (3) that the signal strength is no longer a function of the input phase. Quick and accurate detection can be realized.

Besides the constant magnitude detection, the calibration path still needs to achieve the required 50-dBc detection sensitivity. In this paper, the calibration LOs (ω_{BB} or $2\omega_{\mathrm{BB}}$) are generated from the 20-GHz PLL. The PLL output in this paper is divided by ratios of 192 for the LOFT calibration and 96 for the IMRR calibration. As a result, when the transmitter is operating at channel 2.5 (LO frequency: 61.56 GHz and PLL output frequency: 20.52 GHz), the required baseband test-tone frequency will be 107 MHz. Fig. 11 shows the simulated conversion gain and NF of the calibration path against the input LOFT or image frequency. The TX RF output frequency is kept with 61.667 GHz considering the 107-MHz baseband test tone, while the TX output power is kept with 0 dBm. With three different temperature conditions (27 °C, 85 °C, and −40 °C), the 61.56-GHz LOFT and the 61.453-GHz image result in a conversion gain variation of less than 5.5 dB and a NF variation of less than 4.1 dB.

Fig. 12 shows the simulated SNDR against the LOFT suppression and IMRR over different temperature conditions. The TX output power is still kept with 0 dBm. Usually an uncalibrated LOFT suppression or IMRR can reach 20 dB [1]. A 10-dB design margin is considered for the uncalibrated impairments. To improve the SNDR for a small LOFT suppression or IMRR, the gain of the calibration path can be further decreased. For a large LOFT suppression or IMRR, the SNDR of the calibration path is limited by the noise floor. Regarding the required 50-dBc calibration sensitivity, more than 10-dB margin can be maintained as shown in Fig. 12.

The dc offset of the calibration block will also degrade the calibration accuracy. Because the calibration system itself can be treated as a receiver, the dc offset at the calibration mixer output will directly offset the downconverted dc component. It is well known that the dc offset for a receiver can be expressed as the following equation [29]:

$$V_{\mathrm{offset\_total}} = V_{\mathrm{self\_mixing}} + V_{\mathrm{nonlinear}} + V_{\mathrm{dynamic}} \quad (4)$$

where $V_{\mathrm{self\_mixing}}$ represents the dc offset caused by the calibration LO self-mixing which is static and independent of the input. $V_{\mathrm{nonlinear}}$ stands for the input-dependent dc component caused by the second-order nonlinearity of the calibration circuit. V_{dynamic} denotes the dynamic dc offset. Because of the huge frequency difference between the calibration LO and the 60-GHz RF signal, the dynamic dc offset caused by reradiation can be ignored. Regarding $V_{\mathrm{self\_mixing}}$, the dc offset from self-mixing can be removed by testing the ADC outputs $V'_{\mathrm{out\_I}}$ and $V'_{\mathrm{out\_Q}}$ without any RF input. The signal strength can be rewritten as

$$\begin{aligned}&\text{Signal Strength'}\\ &= \sqrt{\left(V_{\mathrm{out\_I}}-V'_{\mathrm{out\_I}}\right)^2+\left(V_{\mathrm{out\_Q}}-V'_{\mathrm{out\_Q}}\right)^2}. \quad (5)\end{aligned}$$

The accuracy of Signal Strength' will rely on the effective number of bits (ENOB) of ADC. With enough design margin (10 bit in this paper), $V_{\text{self\_mixing}}$ will not limit the final calibration accuracy. Furthermore, it is known that $V_{\text{nonlinear}}$ can be minimized by optimizing IP2 [30]. The simulated IIP2 for the calibration path in a Monte Carlo simulation falls inside a range of 19.8–20.9 dBm regarding the nonlinearity and random mismatch. When the TX is operating at channel 2.5 (LOFT frequency is 61.56GHz), a large LOFT of −25 dBm at the TX output will result in a −40-dBm input power for the calibration block. The corresponding dc component $V_{\text{nonlinear}}$ is estimated to be 0.23 mV. While for a small LOFT, the induced dc offset is negligible, which will not limit the calibration accuracy.

In addition, the I/Q imbalance of the calibration circuit will cause the potential degradation in the calibration accuracy. Moreover, the phase of the input signal φ_{in} will again influence the detected signal strength. Both 1-dB magnitude mismatch and 10° phase mismatch will cause a larger than 10% peak-to-peak ripple in the detected signal. The magnitude and phase imbalance of the calibration circuits can be suppressed by a frequency-divider-based LO generation and symmetric layout. The ripple can further be mitigated by an averaging function, so the calibration accuracy is not much degraded by the I/Q imbalance.

During the calibration period, the second harmonic of the detected LOFT generated by the calibration VGA will also fall into the same frequency with the detected image signal ($2\omega_{\text{BB}}$). As a result, the LOFT will be calibrated first to prohibit the IMRR calibration accuracy from the degradation. At the same time, the calibrated LOFT will also be slightly influenced by the IMRR calibration due to the changed bias condition. Thus, an additional LOFT calibration is added at the end of the calibration procedure.

B. Transmitter

To meet the stringent transmitter EVM requirement from IEEE 802.11ay, an improved linearity needs to be achieved within a flat frequency response. A mixer-first topology is adopted in the transmitter with the purpose of wideband matching and low power consumption [4]. Fig. 13(a) shows the circuit schematic of the double-balanced upconversion mixer. The LOFT cancellation in this paper is realized by tuning the current sources at the baseband side [31]. Including the design margin, a 10-bit digital-to-analog converter (DAC) is adopted for achieving a tuning resolution of less than 0.1 mV, which corresponds to a higher than 50-dB LOFT suppression.

As mentioned in Section II, the I/Q imbalance in this paper is compensated with a power-efficient RF domain calibration. Fig. 13(b) shows the capacitive-cross-coupling RF VGA. The I/Q magnitude mismatch is compensated by tuning the gate bias. Regarding the phase mismatch calibration, Fig. 14 shows the circuit schematic of QILO. A 3-bit switching capacitor and a 10-bit-DAC-controlled varactor are designed to cover a frequency range from 57 to 66 GHz. To fulfill the required resolution for the I/Q phase calibration mentioned in Section II, a sub-degree I/Q phase tuning is realized by tuning the free-run

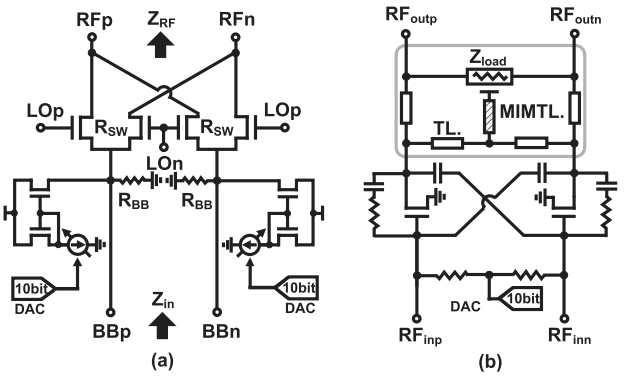


Fig. 13. Circuit schematic of (a) 60-GHz upconversion mixer and (b) 60-GHz VGA.

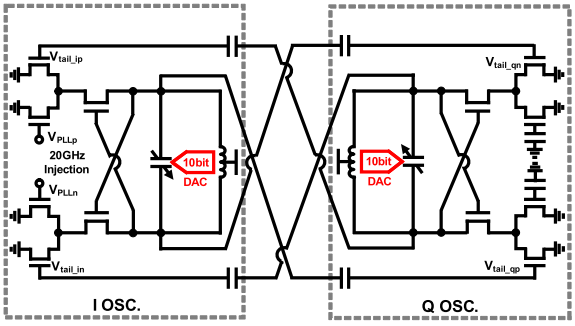


Fig. 14. Circuit schematic of QILO.

frequency of the I oscillator [23]. During the calibration period, the magnitude mismatch will be compensated first and afterward the phase mismatch will be calibrated by the RF gain-invariant phase tuning. The analysis mentioned in Section II assumed a perfect RF domain calibration. However, the mismatch between the I/Q calibration circuits will also induce additional RF domain IMRR degradation. The degradation from the QILO will be limited and frequency independent due to its position at the LO path. While, I/Q VGA will be the main contributor to the IMRR degradation due to its wide operational bandwidth. To analyze the influence from RF VGA, the L-type matching network at the RF VGA output is modeled as a parallel RLC resonant circuit. When the feedback resistor is large enough, the I/Q imbalance due to the VGA can be presented with the following equations:

$$\Delta A = \frac{\text{MAG}_{\text{I}}}{\text{MAG}_{\text{Q}}} = \frac{\left|\frac{g_m(L/C)}{R+j(\omega L-1/\omega C)}\right|_{\text{I}}}{\left|\frac{g_m(L/C)}{R+j(\omega L-1/\omega C)}\right|_{\text{Q}}} = \sqrt{\frac{g_{\text{m\_I}}^2\left(1+Q^2\left(\frac{\omega}{\omega_{0\text{Q}}}-\frac{\omega_{0\text{Q}}}{\omega}\right)^2\right)}{g_{\text{m\_Q}}^2\left(1+Q^2\left(\frac{\omega}{\omega_{0\text{I}}}-\frac{\omega_{0\text{I}}}{\omega}\right)^2\right)}} \tag{6}$$

$$\Delta\varphi = \arctan\left(Q\left(\frac{\omega_{0\text{I}}}{\omega}-\frac{\omega}{\omega_{0\text{I}}}\right)\right) - \arctan\left(Q\left(\frac{\omega_{0\text{Q}}}{\omega}-\frac{\omega}{\omega_{0\text{Q}}}\right)\right) \tag{7}$$

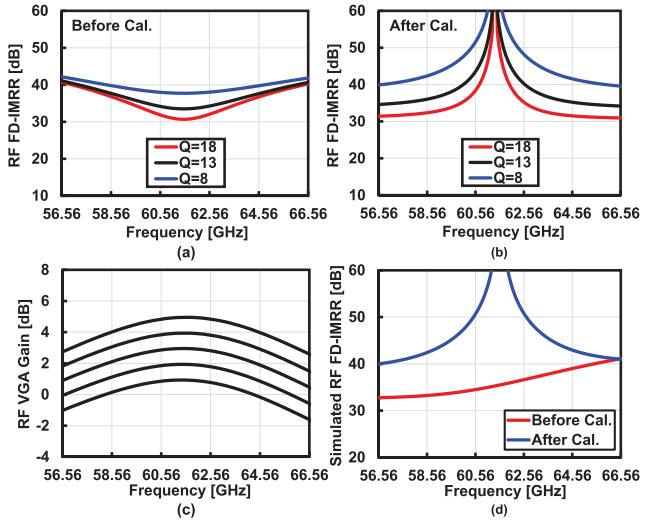


Fig. 15. IMRR due to the RF domain FD I/Q mismatch. (a) Before the proposed calibration. (b) After the proposed calibration. The simulated (c) RF VGA gain and (d) RF FD-IMRR before and after the proposed calibrations.

where ΔA and $\Delta\varphi$ are the I/Q magnitude and phase mismatch, while Q and ω_0 stand for the quality factor and the resonant frequency of the matching network. Equations (6) and (7) find the IMRR degradation due to the transistor g_m mismatch does not rely on the frequency and can be easily removed. However, the resonant frequency difference caused by the mismatched transistor size, and I/Q matching networks will cause an FD-IMRR after the calibration. Fig. 15(a) and (b) shows the influence of the RF FD-IMRR degradation due to the resonant frequency mismatch at channel 2.5. Severe FD-IMRR degradation against the increasing bandwidth after the calibration can be observed with an 100-MHz ω_0 mismatch (1.6%). Fig. 15 also shows that RF FD-IMRR will be improved with a lower quality factor due to the suppressed in-band gain and phase mismatch. To minimize the degradation from the calibration circuit, the RF VGA in this paper is designed based on the CPW. The 50-ohm CPW is utilized to realize a matching network with a reduced quality factor Q. In addition, a symmetric layout of the CPW matching network is also strong against the passive components' mismatch between the I and Q paths. Fig. 15(c) shows the simulated gain of the RF VGA with a 1-dB tuning step. A bandwidth of larger than 10 GHz is covered in this paper. Furthermore, RF-VGA is controlled by a 10-bit DAC. A less than 0.1-dB tuning step is achieved, which meets the resolution requirement from the I/Q magnitude imbalance calibration. The simulated IMRR before and after the proposed calibrations is shown in Fig. 15(d). A transistor size mismatch of 5% is included in this simulation. After the calibration, larger than 40-dB IMRR can be maintained within the whole 60-GHz band. Although the decreased Q results in a 5-dB maximum gain, the wide band matching still contributes to a flatter frequency response. The simulated transmitter-mode 3-dB bandwidth is from 54.8 to 66.7 GHz.

Fig. 16 shows the CPW-based five-stage common-source PA. A cross-sectional view for the proposed CPW is shown

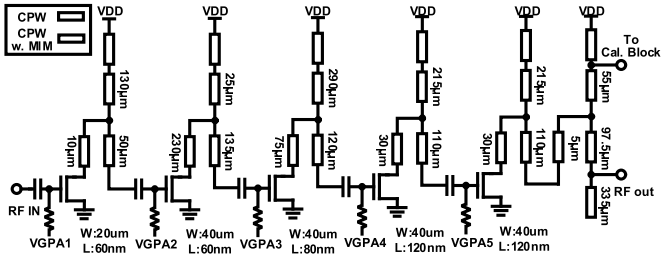


Fig. 16. Circuit schematic of the 60-GHz five-stage PA.

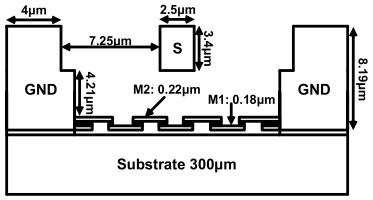


Fig. 17. Cross-sectional view of the CPW line.

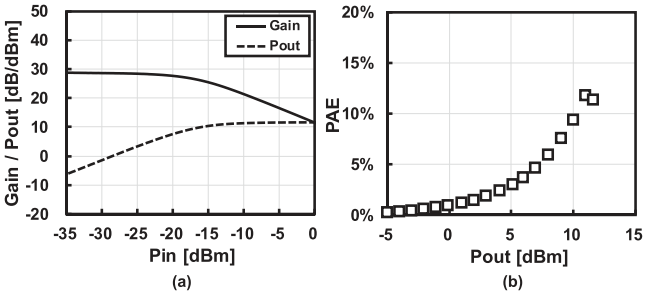


Fig. 18. (a) Measured output power and gain and (b) corresponding PAE of the five-stage PA.

in Fig. 17. The top metal layer is selected for the signal line while the two interdigitated metal layers at the bottom are employed for shielding. Specific sizes of the CPW are optimized for lower attenuation constant, which ensures an efficient and reliable matching performance. The VDD feed line for the PA is realized by CPW with shunt MIM capacitor to ground. The feed line topology is carefully modeled with low impedance but high isolation to RF signal. Fig. 18 shows the measured results for PA at 61.56 GHz. The measured output P_{1dB} is 6.9 dBm, and the saturated output power is 11.6 dBm. The corresponding power-added efficiency (PAE) at the P_{1dB} is 4.6%.

C. Receiver

As mentioned in Section II, receivers targeting at the IEEE 802.11ay standard demand a careful design. The usage of the flipped-voltage-follower (FVF) [32]-based amplifier at the baseband can achieve an improved linearity performance within a wide bandwidth [22]. Fig. 19 shows the single-stage I/Q baseband amplifier employed in this paper. The frequency response is optimized, and the power consumption is 12 mW. The simulated receiver-mode 3-dB RF bandwidth is from 55.9 to 67.6 GHz.

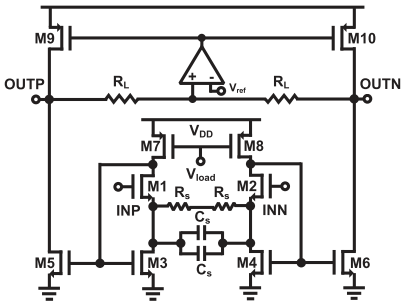


Fig. 19. Circuit schematic of the baseband amplifier.

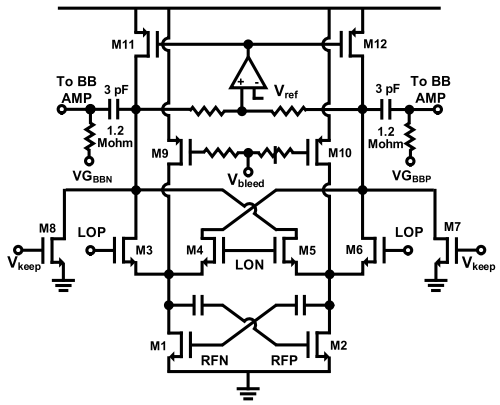


Fig. 20. Circuit schematic of the fast-startup downconversion mixer.

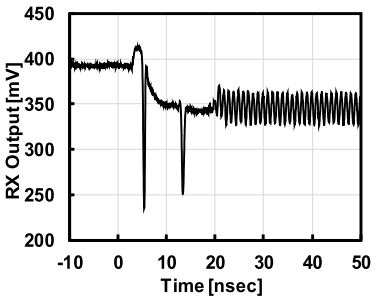


Fig. 21. Measured output of the receiver.

To improve the SNDR of the receiver, a linearity-enhanced double-balanced active mixer based on the current-bleeding technique [33] is adopted in this paper (Fig. 20). A reasonable power budget for the LO path can be realized with the current-mode switching. As shown in Fig. 20, a 3-pF capacitor and a 1.2-Mohm bias resistor are applied to maintain an ac coupling at the mixer output. However, an unreasonable settling time of larger than 3.5 μs will be required due to the charging time of the capacitor [22]. To support the low-latency requirement from IEEE 802.11ay, two dummy transistors M7 and M8 are connected to the mixer output and kept on while the receiver is OFF. The small-size dummy transistors together with the common-mode feedback circuit will keep the output voltage unchanged with a power consumption of only 0.5 mW. Furthermore, the baseband amplifier is shut down with a VDD switch instead of any gate-bias tuning. Fig. 21 shows the measured receiver output with a single-tone input (500 MHz at baseband). The receiver is switched ON at 0 ns. The measured startup time for the receiver is less than 20 ns.

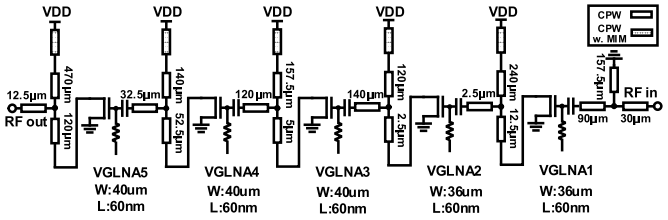


Fig. 22. Circuit schematic of the 60-GHz five-stage LNA.

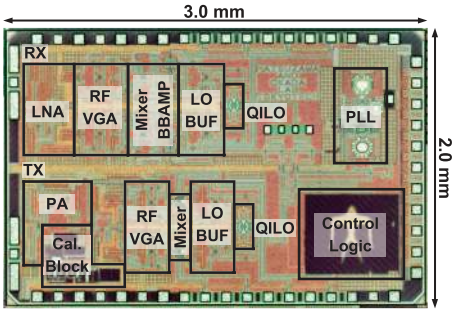


Fig. 23. Die photograph of the 60-GHz transceiver with the calibration block.

TABLE I
CORE AREA OF BLOCKS

	Core Area [mm^2]
TX	1.07
RX	1.09
PLL	0.21
Cal. Block	0.19
Logic	0.36

Regarding the increased input noise floor due to the bandwidth, a five-stage CPW-based LNA is employed in this paper to suppress the noise. The circuit schematic is shown in Fig. 22. The input shunt-stab matching is shorted to ground for the purpose of electrostatic discharge (ESD) protection. Two I/Q coupled-line baluns optimized by the electromagnetic (EM) simulation are inserted to transform the single-ended signal into differential.

IV. MEASUREMENT RESULTS

The 60-GHz transceiver with the calibration block is fabricated in a standard 65-nm CMOS technology. Fig. 23 shows the die micrograph. The chip size is 3 mm $\times$ 2 mm with a core area of 2.81 mm^2. Core area for each block is summarized in Table I. The proposed on-chip calibration block occupies an area of less than 0.2 mm^2, which is area efficient. Fig. 24 shows the 60-GHz RF PCB for measurement. The chip is silver epoxy glued in the center of the PCB and connected to the 50-ohm transmission line with bonding wires. A bonding wire inductance of 0.5-nH is considered in the simulation.

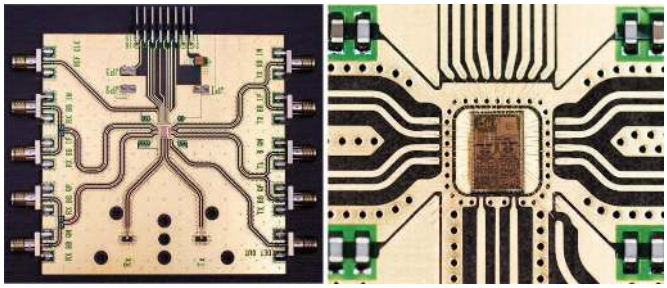


Fig. 24. RF PCB for measurement.

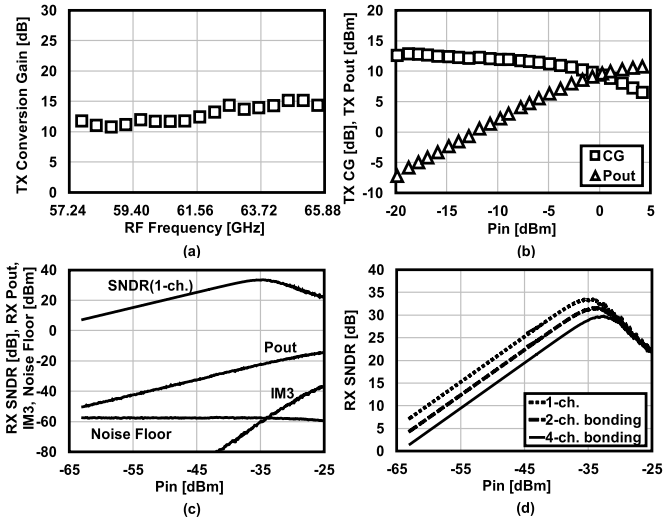


Fig. 25. Measured characteristics of TX: (a) TX conversion gain over frequency and (b) output power and conversion gain against input power. Measured characteristics of RX: (c) RX SNDR, *P*out, IM3, and noise floor for one-channel bandwidth and (d) RX SNDR for two-channel-bonding bandwidth and four-channel-bonding bandwidth.

The dc supply and the control signals for the on-chip logic are sent from the pin connectors. The insertion loss of the PCB is measured by comparing the saturated output power of a PCB in transmitter mode and a stand-alone PA. A PCB loss of 9.8 dB is observed at 61.56 GHz.

Fig. 25(a) shows the conversion gain of the TX excluding the PCB loss. The conversion gain is around 12.5 dB. To support the IEEE 802.11ay standard, TX is required to cover the four channels defined in the 60-GHz band. The measured gain has a 4.5-dB variation over the entire 8.64-GHz bandwidth with a carrier frequency of 61.56 GHz (channel 2.5). Fig. 25(b) shows the measured TX output power against the input power. The measured TX saturated output power is 10.8 dBm excluding the PCB loss. The measured output P_{1dB} for TX is 6.5 dBm. Fig. 25(c) shows the measured output power, third-order intermodulation power (IM3), and output noise floor for RX. The LO frequency is 61.56 GHz while the input frequency is 61.66 GHz. The SNDR of the RX is calculated regarding the measured IM3 and noise floor with different bandwidth conditions [Fig. 25(d)]. The calculated peak SNDRs are 33.5, 31.6, and 29.8 dB for one-channel, two-bonded channel, and four-bonded channel, respectively.

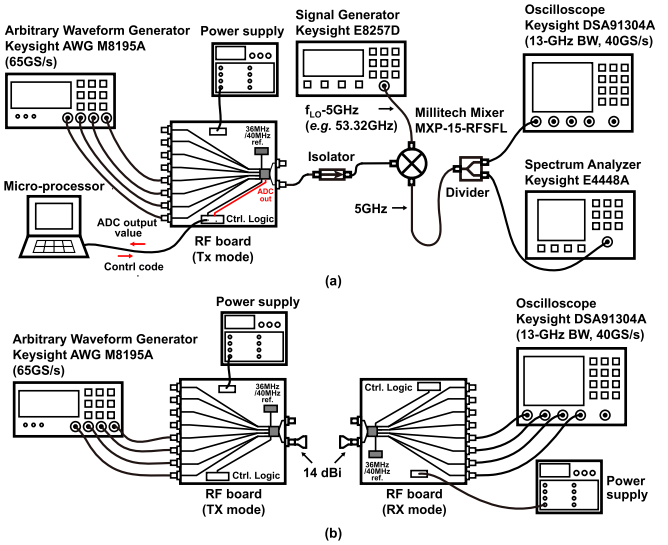


Fig. 26. Equipmental setup for (a) TX calibration and TX EVM measurement and (b) TX-to-RX EVM measurement.

The measured phase noise at channel 2 is −93 dBc/Hz with a 1-MHz offset [23].

Fig. 26(a) shows the equipment setup for the TX EVM measurement. One PCB in the transmitter mode with a 36-MHz onboard reference is used in this measurement. Fig. 26(b) shows the measurement setup for TX-to-RX EVM. Two PCBs with two 14-dBi horn antennas are used in this measurement. One operates in the transmitter mode and the other operates in the receiver mode. During the measurement, the TX and RX are tested in the SC mode. For both TX and TX-to-RX measurement, the baseband signal is generated by an arbitrary waveform generator (Keysight AWG M8195A). Modulated baseband signals with the symbol rate of 1.76 GSymbol/s for a one-channel bandwidth, 3.52 GSymbol/s for a two-bonded channel, and 7.04 GSymbol/s for a four-bonded channel are generated. The corresponding roll-off factor is 0.25. The TX output spectrum is observed with a downconversion mixer and a spectrum analyzer (Keysight E4448A). An oscilloscope (DSA91394A) with an adaptive equalizer is used for the EVM measurement.

The TX calibration performance is also evaluated with the setup shown in Fig. 26(a). A single-tone baseband signal of 107 MHz is generated from the AWG for the calibration. The LO frequency is 61.56 GHz. In this condition, frequencies of the corresponding RF signal, LOFT, and image signal are 61.453, 61.56, and 61.667 GHz, respectively. During the calibration period, the output codes of the calibration ADCs will be sent to a microprocessor, and a gradient descent algorithm is applied to search for the best bias value. Finally, the feedback control code will be sent back to the chip for calibration. Fig. 27 shows the measured Signal Strength″ calculated from the output codes of I/Q ADCs. ADC_{I} and ADC_{Q}, and ADC_{I0} and ADC_{Q0} in the equation stand for the output codes with and without RF input for the calibration block, respectively. The TX output power is fixed with −5 dBm in this measurement. As shown in Fig. 27,

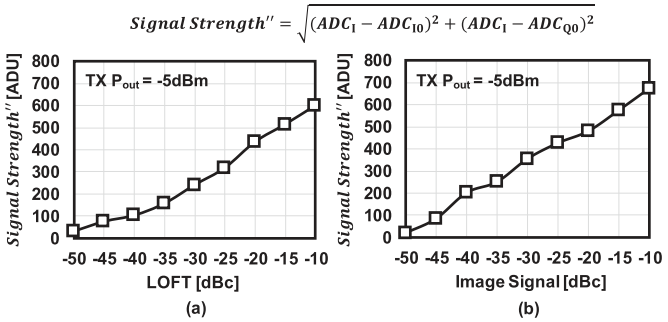


Fig. 27. (a) Measured detected signal strength against the LOFT. (b) Measured detected signal strength against the image signal.

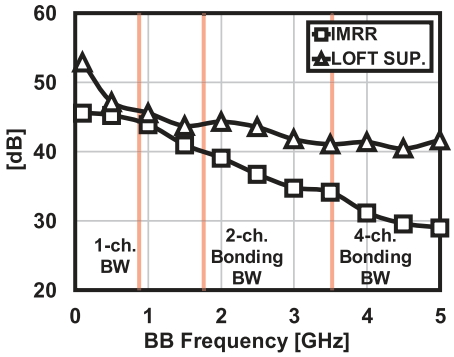


Fig. 28. Measured LOFT suppression and IMRR over the baseband frequency.

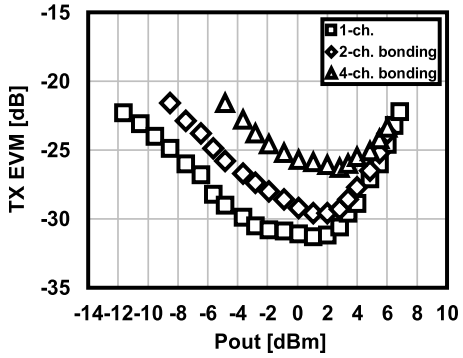


Fig. 29. Measured TX EVM with one-channel bandwidth, two-channel-bonding bandwidth, and four-channel-bonding bandwidth in the 60-GHz band.

The LOFT and the image signal level less than −50 dBc can still be detected by the proposed circuit. The calibrated LOFT suppression and IMRR over the channel-bonding conditions are measured and shown in Fig. 28. The LOFT suppression is always higher than 40 dB within the four-bonded channel. The IMRR of TX is better than 44.5, 40.0, and 34.2 dB for one channel, two-bonded channel, and four-bonded channel, respectively. The influence of FD-IMRR after an RF domain calibration can be obviously observed from this result. One important reason for the observed FD-IMRR is because of the FD mismatch caused by the RF PCB and the baseband cables. Fig. 29 demonstrates the TX 64-QAM EVM after the calibration against the average output power. In the left region of the traces, EVMs are dominated by the output noise floor, while in the right region, the EVMs are limited by IM3. Thanks to the high-accuracy calibration, the minimum EVMs of TX in 64 QAM are 31.3, 29.8, and 26.3 dB for one channel, two-bonded channel, and four-bonded channel, respectively. The peak EVM for the four-channel-bonding condition is degraded in Fig. 29, which is due to the increased bandwidth. By optimizing the transmitter path NF, the peak EVM can be improved.

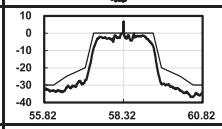
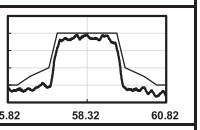
	Before cal.	After cal.
Carrier freq.	58.32GHz	58.32GHz
BW.	1.76GHz	1.76GHz
Modulation	128QAM	128QAM
Data rate	-	12.32Gb/s
Constellation		
Spectrum		
TX EVM	-19.5dB	-28.7dB
TX-to-RX EVM	-	-27.2dB

Fig. 30. Measured TX and TRX performances at channel 1 before and after the calibrations in the SC mode.

A similar calibration is performed at channel 1 (carrier frequency: 58.32 GHz). Fig. 30 shows the comparison of the spectrum and constellation in 128 QAM before and after the calibrations. Large LOFT at 58.32 GHz can be observed from the spectrum before calibration, which cannot satisfy the spectrum emission mask requirement. After the calibration, LOFT and image signal are suppressed. A TX EVM improvement of 9.2 dB is achieved. The RX IMRR calibration in this paper is performed by adjusting the RX I/Q VGA and QILO. The corresponding TX-to-RX EVM after the calibration within a 2.16-GHz (one-channel) bandwidth is −26.0 dB in 128 QAM, which satisfies the requirement for a BER of less than 10^{-3}. A data rate of 12.32 Gb/s in 128 QAM is realized by the transceiver.

The IEEE 802.11ay standard demands the coexistence with the existing IEEE 802.11ad standard. As a result, channels defined in IEEE 802.11ad (channel 1–channel 4) are supposed to be supported by the proposed transceiver. Fig. 31 summarizes the measured spectrum, constellation, TX EVM, and TX-to-RX EVM in 64 QAM for each channel. The EVMs are measured in the SC mode. The measured peak TX EVMs in 64 QAM are better than −28.4 dB. Furthermore, the TX output spectra satisfy the required spectrum emission mask. The measured peak TX-to-RX EVMs in 64 QAM are −28.2, −27.0, −25.2, and −27.1 dB for channel 1, channel 2, channel 3, and channel 4, respectively. The maximum communication distance is defined by the required TX-to-RX SNRs for a BER of 10^{-3}, which are −9.8 dB for QPSK, −16.5 dB for 16 QAM, −22.5 dB for 64 QAM, and −25.5 dB for 128 QAM. Data link of 10.56 Gb/s in 64 QAM is

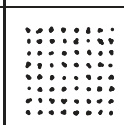
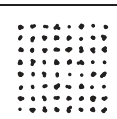
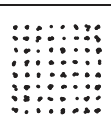
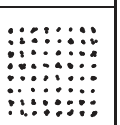
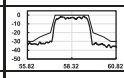
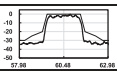
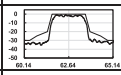
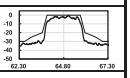
Channel/ Carrier freq.	ch.1 58.32GHz	ch.2 60.48GHz	ch.3 62.64GHz	ch.4 64.80GHz
Modulation	64QAM			
Data rate	10.56Gb/s	10.56Gb/s	10.56Gb/s	10.56Gb/s
Constellation				
Spectrum				
TX EVM	-30.3dB	-30.0dB	-29.3dB	-28.4dB
TX-to-RX EVM	-28.2dB	-27.0dB	-25.2dB	-27.1dB
Distance	0.15m	0.15m	0.14m	0.14m

Fig. 31. Measured performance in 64 QAM within the channels defined in IEEE 802.11ad.

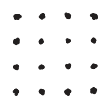
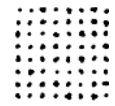
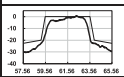
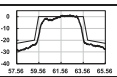
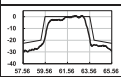
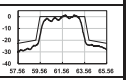
Carrier freq. BW.	61.56GHz 2-ch. bonding	61.56GHz 2-ch. bonding	61.56GHz 2-ch. bonding	61.56GHz 2-ch. bonding
Modulation	QPSK	16QAM	64QAM	128QAM
Data rate	7.04Gb/s	14.08Gb/s	21.12Gb/s	24.64Gb/s
Constellation				
Spectrum				
TX EVM	-29.7dB	-29.5dB	-29.8dB	-27.1dB
TX-to-RX EVM	-26.6dB	-27.3dB	-27.5dB	-26.1dB
Distance	1.06m	0.40m	0.10m	0.03m

Fig. 32. Summarization of two-channel-bonding performance at channel 2.5 defined in IEEE 802.11ay.

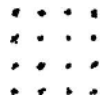
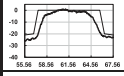
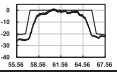
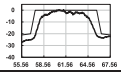
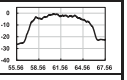
Carrier freq. BW.	61.56GHz 4-ch. bonding	61.56GHz 4-ch. bonding	61.56GHz 4-ch. bonding	61.56GHz 10.44GHz
Modulation	QPSK	16QAM	64QAM	64QAM
Data rate	14.08Gb/s	28.16Gb/s	42.24Gb/s	50.10Gb/s
Constellation				
Spectrum				
TX EVM	-26.3dB	-26.3dB	-26.3dB	-24.0dB
TX-to-RX EVM	-24.5dB	-24.6dB	-24.3dB	-23.2dB
Distance	0.54m	0.24m	0.04m	0.04m

Fig. 33. Summarization of four-channel-bonding performance at channel 2.5 defined in IEEE 802.11ay.

maintained from channel 1 to channel 4 with further than 0.14-m communication distance. A 2.5-m communication distance is achieved at channel 1 in QPSK.

TABLE II
POWER CONSUMPTION OF BLOCKS

	Sub Blocks	Power Consumption [mW]
TX	PA	105.7
	I/Q RF VGA	12.1
	I/Q Mixer	2.0
	I/Q LO Buffer	16.6
	QILO	14.6
Cal. Block		3.1
RX	LNA	60.2
	I/Q RF VGA	20.5
	I/Q Mixer	6.4
	I/Q BB Amp	12.3
	I/Q LO Buffer	13.8
	QILO	10.3
PLL		15.0

Figs. 32 and 33 demonstrate the summarized channel-bonding performance at channel 2.5. Within a two-channel-bonding bandwidth, the TX after the calibration achieves TX EVMs of -29.7, -29.5, -29.8, and -27.1 dB in QPSK, 16 QAM, 64 QAM, and 128 QAM, respectively. The maximum data rate realized with a two-bonded channel is 24.64 Gb/s in 128 QAM. The corresponding TX-to-RX EVM is -26.1 dB. The measured maximum distances with a two-bonded channel are 1.06 m for QPSK, 0.40 m for 16 QAM, 0.10 m for 64 QAM, and 0.03 m for 128 QAM. Regarding a four-channel-bonding condition, the transceiver in this paper supports data links of 14.08 Gb/s in QPSK, 28.16 Gb/s in 16 QAM, and 42.24 Gb/s in 64 QAM. The corresponding TX-to-RX EVMs are -24.5 dB in QPSK, -24.6 dB in 16 QAM, and -24.3 dB in 64 QAM. For both two-channel-bonding and four-channel-bonding conditions, the output spectra satisfy the spectrum emission masks from IEEE 802.11ay. The non-flatness of the spectrum is mainly from the five-stage PA and the measurement equipment. The measured maximum data rate is 50.1 Gb/s in 64 QAM with an RF bandwidth of 10.44 GHz. The corresponding TX EVM and TX-to-RX EVM are -24.0 and -23.2 dB, respectively. A communication distance of 0.04 m is achieved in this condition.

Table II shows the power consumption breakdown of the transceiver. The analog and digital supply voltages are 1 V in this paper. The proposed calibration block consumes 3.1 mW during the calibration period. The power consumption of the transceiver in the TX mode is 169 mW including the PLL and the calibration block. The measured RX mode power consumption is 139 mW with PLL.

Table III shows the comparison of this work with the state-of-the-art 60-GHz CMOS transceiver front ends. This paper presents the first 60-GHz transceiver achieving four-channel bonding in 64 QAM with a single-element transceiver. An equivalent data rate of 42.24 Gb/s is realized with a low power consumption. Furthermore, this paper is the first-reported transceiver achieving 128 QAM in the 60-GHz band. Data rate of 24.64 Gb/s in 128 QAM is available with two-channel bonding.

TABLE III
PERFORMANCE COMPARISON OF 60-GHZ TRANSCEIVERS

	Data rate/ Modulation	TX-to-RX EVM	Pout/ant. path	Integration	Power Consumption
Panasonic [1]	2.5Gb/s QPSK	-22.0dB (1 ch.) (TX only)	2.0dBm at TX EVM=-22.0dB	90nm, direct conversion, TX, RX, LO, antenna, analog BB, dig. BB.	TX: 347mW RX: 274mW
Broadcom [2]	4.6Gb/s 16QAM	-19.5dB (1 ch.)	-4.0dBm* at TX EVM=-21.0dB	40nm, 16-array heterodyne, TX, RX, LO, analog BB, dig. BB.	TX: 1190mW RX: 960mW 16x16 array
Broadcom [3]	4.6Gb/s 16QAM	-20.5dB (1 ch.)	-2.0dBm at TX-to-RX EVM =-22.0dB	28nm/40nm, 144-array, heterodyne, TX, RX, LO, analog BB, dig. BB	TX: 8400mW RX: 6600mW 144-element
Tokyo Tech [4]	28.16Gb/s 16QAM 4-ch. bonding	-26.3dB (1 ch.)	8.5dBm at TX EVM=-21.0dB	65nm, direct conversion, TX, RX, LO.	TX: 251mW RX: 220mW
Intel [5]	27.8Gb/s 16QAM	-18.0dB	N.A.	28nm, digital polar TX, direct conversion RX, TX, RX, LO, w/o PLL.	TX: 210mW RX: 110mW
Tokyo Tech [6]	21.12Gb/s +21.12Gb/s 2ch. bonding x 2	-24.0dB (LB) -23.0dB (HB)	7.0dBm at TX EVM=-22.0dB	65nm, direct conversion, 2TX, 2RX, 2LO.	TX: 544mW RX: 432mW
IMEC [17]	7Gb/s 16QAM	-20.4dB (1 ch.)	6dBm* at TX EVM=-23dB	28nm, 4-element, direct conversion, TX, RX, LO.	TX: 670mW RX: 431mW 4-element
This Work	12.32Gb/s 128QAM 1 ch.	-27.2dB (1 ch.)	7.3dBm at TX EVM=-22.0dB	65nm, direct conversion, TX, RX, LO.	TX: 169mW RX: 139mW
	24.64Gb/s 128QAM 2-ch. bonding	-26.1dB (2-ch. bonding)			
	42.24Gb/s 64QAM 4-ch. bonding	-24.3dB (4-ch. bonding)			
	50.10Gb/s 64QAM 10.44GHz BW.	-23.2dB (10.44 BW.)			

*estimated from the material.

V. CONCLUSION

This paper presents a 60-GHz CMOS transceiver designed for the IEEE 802.11ay standard. A calibration block for LOFT and I/Q imbalance featuring high accuracy and low power is implemented with the transceiver. The RF building blocks are optimized for high SNDR and flat gain response. The proposed transceiver supports the channels defined in the existing IEEE 802.11ad standard together with the bonded channels defined in the IEEE 802.11ay standard. This paper reports the first 128 QAM 60-GHz transceiver. In addition, a four-channel-bonding data rate of 42.24 Gb/s in 64 QAM is available with a single-element transceiver. A maximum data rate of 50.1 Gb/s in 64 QAM is realized, which is the highest data rate achieved by using the 60-GHz band.

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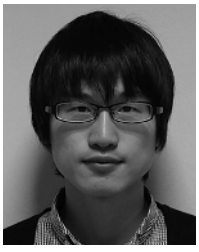

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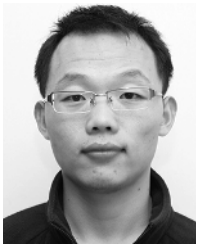

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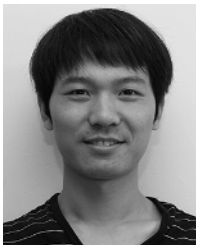
His main research filed includes digital phase-locked loops (PLLs), fully synthesizable analog/RF circuits, and digital-intensive/digitally assisted mixed-signal systems.



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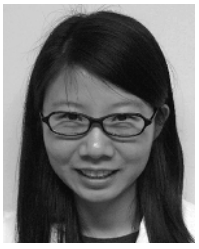

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