A 53-nW 9.1-ENOB 1-kS/s SAR ADC in 0.13-m CMOS for Medical Implant Devices

Dai Zhang, Ameya Bhide and Atila Alvandpour

Dai Zhang, Ameya Bhide and Atila Alvandpour, A 53-nW 9.1-ENOB 1-kS/s SAR ADC in 0.13-m CMOS for Medical Implant Devices, 2012, IEEE Journal of Solid-State Circuits, (47), 7, 1585-1593.
http://dx.doi.org/10.1109/JSSC.2012.2191209
Postprint available at: Linköping University Electronic Press
http://urn.kb.se/resolve?urn=urn:nbn:se:liu:diva-80792

Paper title: A 53-nW 9.1-ENOB 1-kS/s SAR ADC in 0.13-μm CMOS for Medical Implant Devices

Authors: Dai Zhang, Ameya Bhide, and Atila Alvandpour

Affiliation: Department of Electrical Engineering, Linköping University, Linköping, Sweden

Authors' contact information:

Dai Zhang	Ameya Bhide	Atila Alvandpour
Student Member, IEEE	Student Member, IEEE	Senior Member, IEEE
Email: dai@isy.liu.se	Email: ameya@isy.liu.se	Email: atila@isy.liu.se
Tel: +46(0)13-282703	Tel: +46(0)13-288946	Tel: +46(0)13-285818

Abstract

This paper describes an ultra-low power SAR ADC for medical implant devices. To achieve the nano-watt range power consumption, an ultra-low power design strategy has been utilized, imposing maximum simplicity on the ADC architecture, low transistor count and matched capacitive DAC with a switching scheme which results in full-range sampling without switch bootstrapping and extra reset voltage. Furthermore, a dual-supply voltage scheme allows the SAR logic to operate at 0.4 V, reducing the overall power consumption of the ADC by 15% without any loss in performance. The ADC was fabricated in 0.13-μm CMOS. In dual-supply mode (1.0 V for analog and 0.4 V for digital), the ADC consumes 53 nW at a sampling rate of 1 kS/s and achieves the ENOB of 9.1 bits. The leakage power constitutes 25% of the 53-nW total power.

Index Terms – ADC, analog-to-digital conversion, low-power electronics, successive approximation, leakage power consumption, medical implant devices.

I. INTRODUCTION

Medical implant devices, such as pacemakers and implantable cardiac defibrillators, target increasingly advanced signal acquisition and signal processing systems. Such devices, which are to be implanted in the human body, require extremely low power consumption in order to operate up to 10 years or more [1]. Analog-to-digital converters (ADCs) are among the most critical and power hungry components of medical implant devices for measurements of various electrophysiological signals (DC to a few kHz [2]). Conversion of the low-frequency analog signals does not need high speed, but requires ultra-low-power operation (e.g. in nW range). This combined with the required conversion accuracy makes the design of such ADCs a major challenge. So far, most of the research on ADCs has been focused on moderate and particularly high-speed applications, while efficient design methodologies and circuit techniques for low-speed and ultra-low-power ADCs have not been explored in depth.

This paper describes a 10-bit 1-kS/s successive approximation register (SAR) ADC in 0.13-μm CMOS for medical implant devices [3]. Trading speed for lower power at such slow sampling rates is not a straightforward task. The major challenge is how to efficiently reduce the unnecessary speed and bandwidth for ultra-low-power operation using inherently fast devices in advanced CMOS technologies. Moreover, the leakage currents contribute to a significant portion of the total power consumption. As an example, 0 shows the average power consumption of an inverter in a 0.13-μm CMOS technology as a function of its switching frequency. The power consumption was simulated at two different supplies (1.0 V and 0.4 V) over two different sizes (W_{min}/L_{min} and $W_{min}/2L_{min}$). It can be seen that the leakage power at 1-10 kHz can constitute more than 50% (50% at 10 kHz) of the total power.

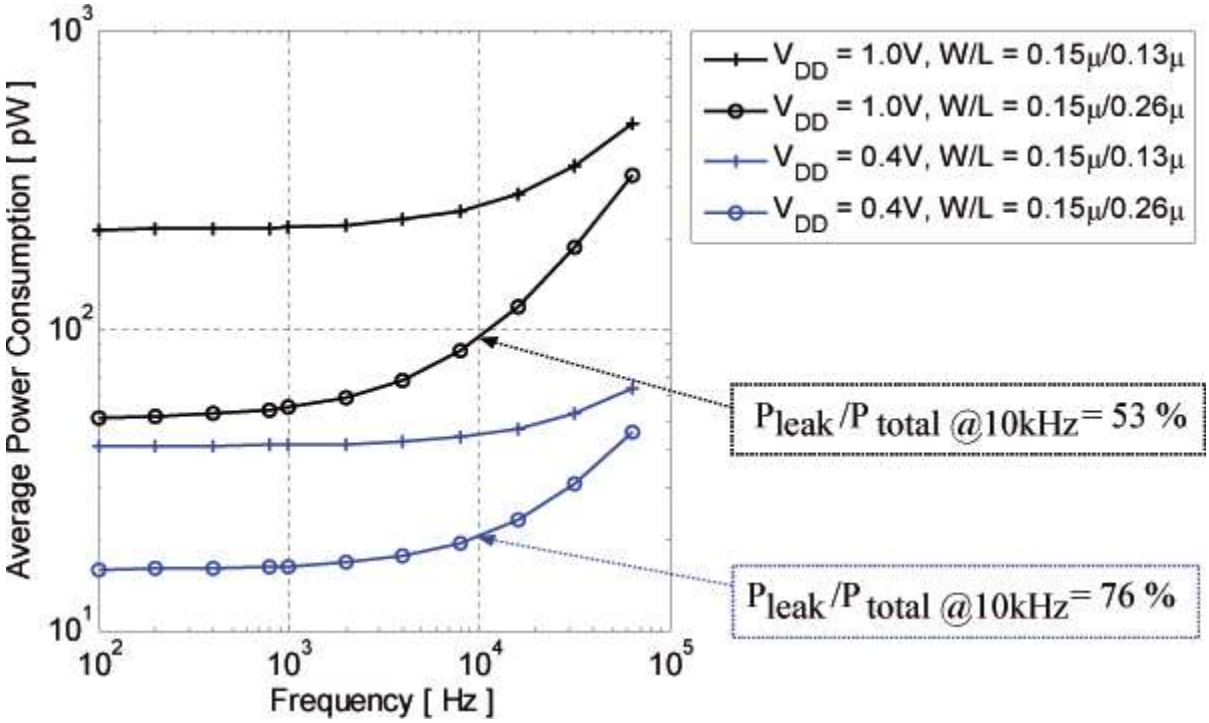

Fig.1: Simulated average power consumption versus switching frequency of an inverter with a fan-out of four in 0.13-μm CMOS.

Considering the above discussion and the fact that every nano-watt counts for such ADCs, the main key to achieve the ultra-low-power operation turns out to be the maximal simplicity in the ADC architecture and low transistor count. This essentially means that we avoid ADC techniques with additional complexity and circuit overhead, which are useful for higher sampling rates. Digital error correction [4]-[6] has been frequently used in high-speed ADCs, where capacitor redundancy is utilized to meet the linearity requirement without degrading the speed. However, the circuit overhead required for the digital post-processing leads to additional switching and leakage power consumption. On-chip digital calibration [7][8] serves as an alternative solution without large amount of digital post-processing, but it requires additional calibrating capacitor arrays and registers. Besides, to ensure the calibration efficiency, the comparator offset should be removed prior to linearity calibration. Taking advantage of the low

speed, the proposed ADC utilizes a matched capacitive DAC, being sized to achieve the 10-bit conversion accuracy without digital error correction or calibration, thus eliminating additional devices and significant leakage currents. Moreover, the matched capacitive DAC uses a switching scheme that allows full-range sampling without switch bootstrapping and extra reset voltages. Compared to the energy-efficient switching schemes [9]-[11], the employed approach introduces less overhead in the SAR control logic [9][10] and avoids additional bias voltages in the comparator [11]. To further reduce the power consumption, a dual-supply voltage scheme was employed, allowing the SAR logic to operate at 0.4 V. Utilizing the above design strategy combined with low-leakage circuit techniques, careful circuit optimizations, and circuit layout, the SAR ADC consumes 53 nW power at a sampling rate of 1 kS/s, achieving 9.1 ENOB.

The paper is organized as follows. Section II describes the ADC architecture. Section III presents the detailed circuit design of the ADC. The measurement results and comparison with previous works are shown in section IV, followed by conclusions in section V.

II. ADC ARCHITECTURE

0 shows the block diagram of the proposed ADC. It comprises a matched binary-weighted capacitive DAC, a low-power dynamic latch comparator, a low-leakage/low-voltage synchronous SAR digital logic, and level shifters between the digital logic and the analog blocks. In addition, a differential architecture was employed to have a good common-mode noise rejection.

In a conventional SAR ADC [12], the input voltage is sampled on the bottom-plate nodes of the capacitor array and the top-plate nodes are reset with a fixed voltage. The fixed voltage is commonly chosen to be one of the power rails in order to avoid extra voltage levels. However,

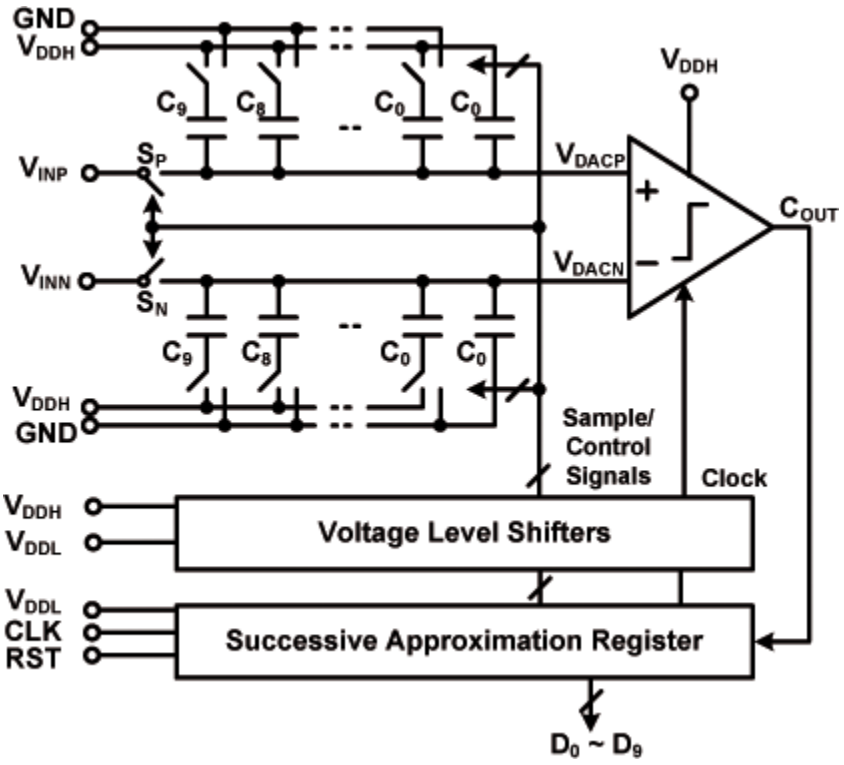

Fig. 2: Architecture of the SAR ADC.

this makes the DAC outputs go beyond the rails during the conversion when full-range input sampling is applied. One common way to solve this problem is to decrease the input range with the penalty of degrading the signal-to-noise ratio. Another alternative is to make the top-plate switches bootstrapped. In this work, we use top-plate sampling [10] with MSB preset to achieve full-range sampling without switch bootstrapping and extra reset voltages. As shown in 0, the differential inputs are initially connected to the top-plates of the capacitor array, and simultaneously the MSB is reset to high and all other bits are reset to low. Next, the top-plate sampling switch is open and the input data is sampled on the capacitor array. The comparator then performs the first comparison. If V_{DACP} is higher than V_{DACN}, the MSB remains high. Otherwise, it goes low. Then, the second approximation step starts by setting MSB-1 to high, and

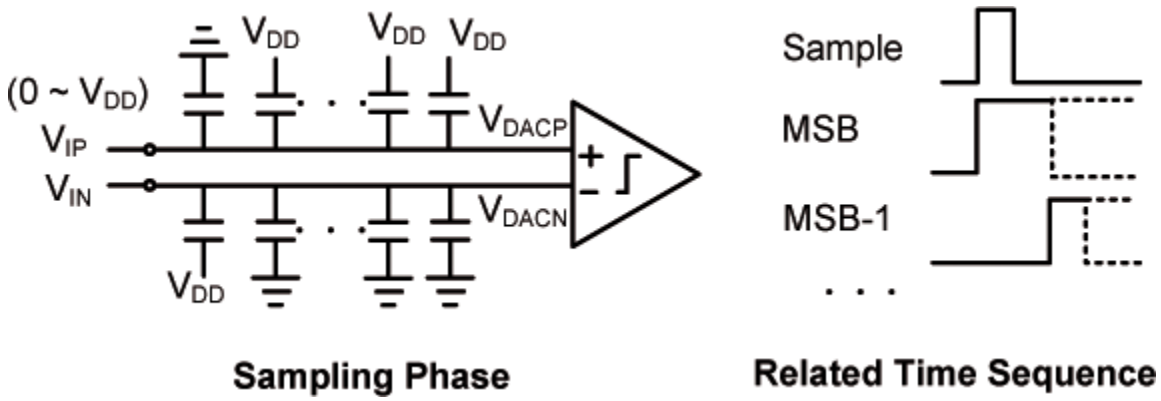

Fig. 3: The sampling phase of capacitive DAC with MSB preset.

the comparator does the comparison again. The ADC repeats this procedure until all 10 bits are decided. During the entire conversion, the DAC outputs always remain within the rails. Moreover, the common-mode voltage of the DAC outputs is the same as that of the differential inputs, which is equal to mid-rail voltage for full-range input sampling, as shown in 0. The constant common-mode voltage reduces the signal-dependent dynamic offset of the comparator [11].

Lowering the supply voltage is an efficient technique to reduce both the switching and leakage power consumption. This is particularly true at low data-rates, where transistors can be slow but still meet the target speed. However, for the analog circuits operating with low supply voltages, noise and a reduced dynamic range can degrade the ADC performance. To avoid the analog performance degradation, in this design, we use a dual-supply voltage scheme, which allows the SAR logic to operate at low supply voltages. Our measurement results (in Sec. IV) show that this voltage scaling has reduced the overall power consumption of the ADC by 15% without any loss in performance.

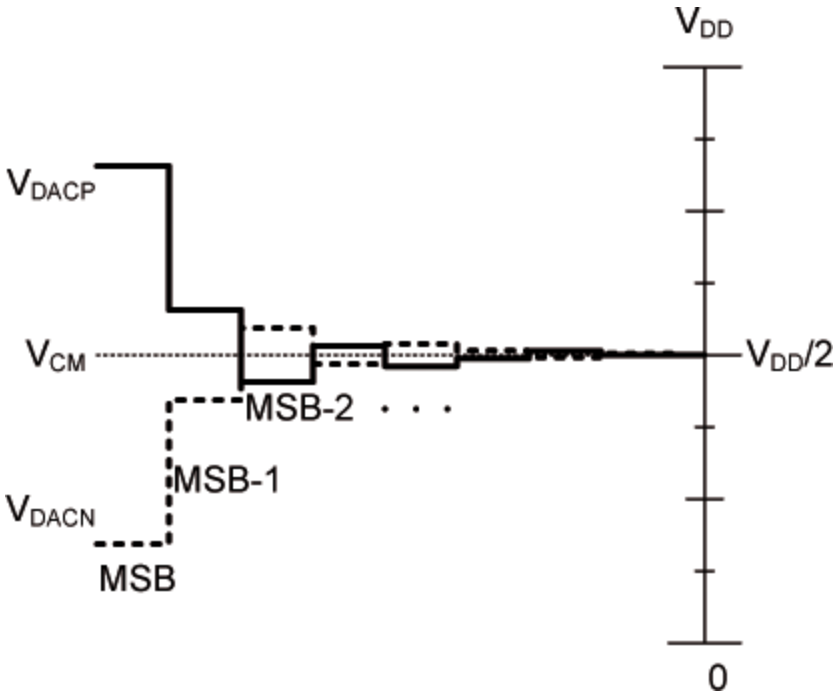

Fig. 4: Waveform of the DAC switching procedure.

III. Circuit Implementation

In this section, the circuit level design of the DAC, switches, comparator, and SAR digital logic are described. Since these components are critical with regards to power consumption, speed, and accuracy of the entire ADC, much of the design effort was focused on characterizing and optimizing their performance.

A. Capacitive DAC

The capacitive DAC was implemented with a binary-weighted capacitor array instead of split architecture with an attenuating capacitor [13]-[15]. The split architecture is commonly used to reduce the total number of capacitors. However, this technique is sensitive to mismatch as well as to parasitic capacitance. In addition, to meet the linearity requirements, the total capacitance

(and the power consumption) of the split architecture can be comparable to those of a conventional binary-weighted structure [16].

The unit capacitor in the DAC should be kept as small as possible for power saving. In practice, it is usually determined by the thermal noise and capacitor mismatch. In this design, mismatch is dominant over thermal noise. Generally, the unit capacitor is modeled with a nominal value of C_u and a standard deviation of σ_u. For a binary-weighted capacitor array, the worst-case standard deviation of differential nonlinearity (DNL) and integral nonlinearity (INL) occur at the MSB code transition due to the accumulation of the capacitor mismatch. Following the analysis in [17], they can be expressed in terms of LSB as

$$\sigma_{DNL,MAX} = \sqrt{2^N - 1}\,\frac{\sigma_u}{C_u} LSB, \tag{1}$$

$$\sigma_{INL,MAX} = \sqrt{2^{N-1}}\,\frac{\sigma_u}{C_u} LSB, \tag{2}$$

where N is the ADC resolution. Comparing (1) with (2), the derived worst-case standard deviation of DNL is larger than that of INL. Therefore, (1) is chosen to be a reference in the following analysis. For a typical metal-insulator-metal (MIM) capacitor, it has

$$\sigma\left(\frac{\Delta C}{C}\right) = \frac{K_\sigma}{\sqrt{A}}, \text{and } C = K_C \cdot A, \tag{3}$$

where $\sigma(\Delta C/C)$ is the standard deviation of capacitor mismatch, K_σ is the matching coefficient, A is the capacitor area, and K_C is the capacitor density parameter. The standard deviation of a single capacitor to the nominal value is by factor $\sqrt{2}$ smaller than that of the difference between two capacitors. Thus, $\sigma(\Delta C/C)$ divided by $\sqrt{2}$ is equal to σ_u/C_u. For high yield, it is necessary to

maintain $3\sigma_{DNL,MAX} < {}^1/_2$LSB. Combining the earlier equations, we obtain a lower bound for the mismatch-limited unit capacitor

$$C_U = 18 \cdot (2^N - 1) \cdot K_\sigma^2 \cdot K_{C.} \tag{4}$$

In this technology, a MIM capacitor has a density of 2 fF/μm^2 and a matching of 1% μm. It leads to a minimum unit capacitance of 4 fF. So far, the discussion is for the single-ended architecture. For the differential configuration in this design, the unit capacitance can be reduced by half while still satisfying the mismatch requirement. This is because the differential mode doubles the signal range but only increases $\sqrt{2}$ times of the voltage error introduced by the mismatch.

Apart from the mismatch, the design rule will also set a minimum value on the MIM capacitance. The minimum MIM capacitance defined by this process is 27 fF. Consequently, the unit capacitance was set to be 13.5 fF in our work, which was implemented by two minimum process-defined MIM capacitors in series. Hence, the total array capacitance is about 14 pF.

Besides capacitor sizing, a careful layout to avoid linearity degradation is important as well. In this work, we have utilized a partial common-centroid layout strategy for the capacitor array. 0 illustrates the layout floor plan. The MSB capacitors (C_9 – C_5) follow a common-centroid configuration to minimize the errors from the non-uniform oxide growth in the MIM capacitors. However, the smaller LSB capacitors (C_4 – C_0) have been placed close to the bottom-plate switches to simplify the routing, thereby reducing the parasitic capacitances and resistances of the interconnection. Post-layout simulations showed that the reduced parasitic of the employed partial common-centroid layout results in better DAC linearity, compared to a capacitor array with a full common-centroid layout (where the LSB capacitors were placed in the middle of the array). Based on the simulations, the DAC with the partial common-centroid layout had a peak

DNL of +0.18/-0.20 LSB and INL of +0.30/-0.23 LSB, while the DAC with a full common-centroid layout had a peak DNL of +0.35/-0.16 LSB and INL of +0.40/-0.36 LSB.

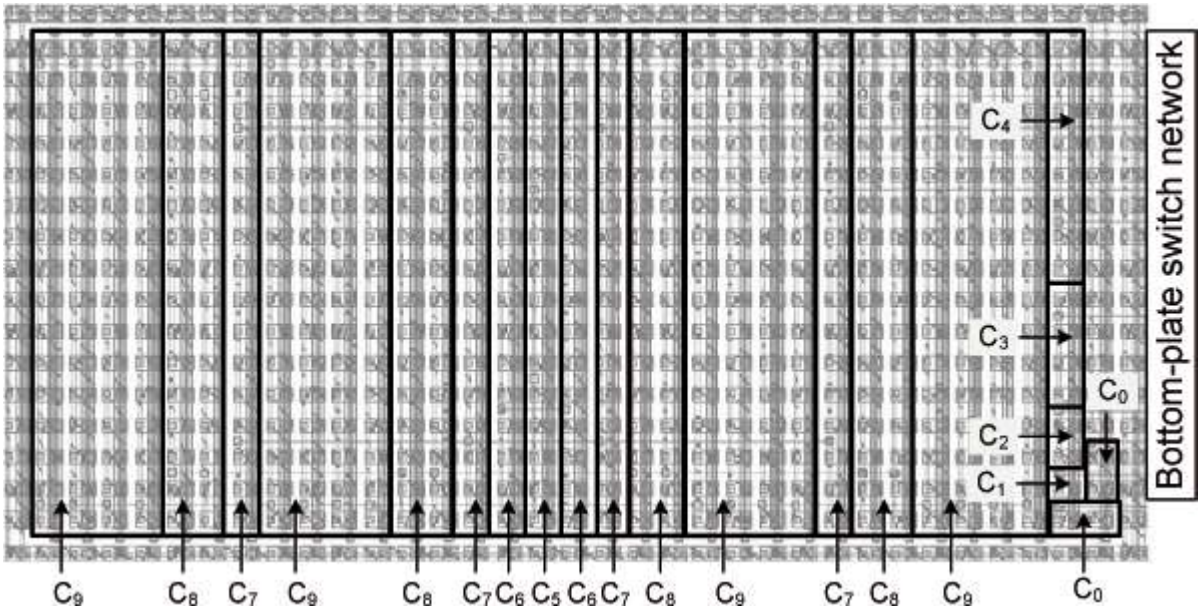

Fig. 5: Layout of the capacitor array which follows a partial common-centroid configuration. The capacitors are indicated according to 0.

B. Switch Design

The top-plate sampling switch was implemented using transmission gate, shown in 0, to achieve full-range input sampling. The switch together with the DAC capacitor array acts as the sample-and-hold circuit of the ADC. If the sampling circuit is designed for an *N*-bit performance, then the settling error of the sampled voltage must be less than half of LSB. This requires [18]

$$f_{3dB} > \frac{(N+1)\cdot \ln 2}{\pi} f_S, \tag{5}$$

where f_S is the sampling frequency. In this design, the sampling time is determined by the system clock, which is *N+2* times the sampling rate. Hence, (5) can be modified to

$$f_{3dB} > \frac{(N+1)\cdot (N+2)\cdot \ln 2}{\pi} f_S. \tag{6}$$

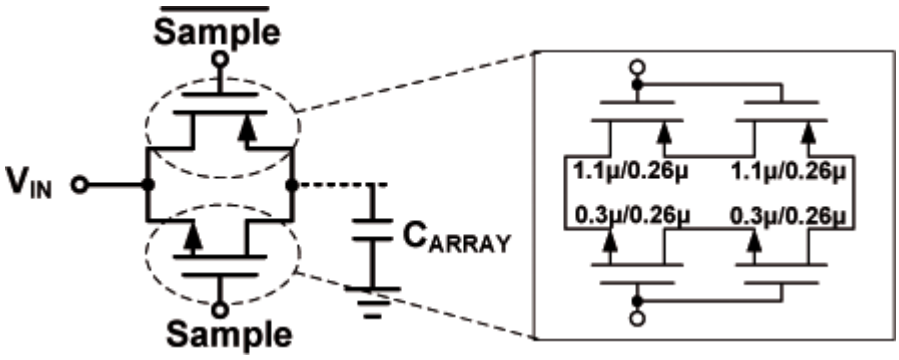

Fig. 6: Top-plate sampling switch.

Based on (6), for a 10-bit 1-kS/s SAR ADC, the required minimum f_{3dB} is about 30 kHz. Taking account of the 14-pF sampling capacitance, the switch on-resistance (R_{ON}) should be designed to be less than 380 kΩ.

Apart from the bandwidth requirement, the voltage drop introduced by the leakage current of the switch can also degrade the conversion accuracy due to the low sampling rate. The sub-threshold leakage current of the transistor is the dominant leakage contributor to the switch. In addition, the leakage current shows nonlinear dependence on the input-output voltage difference across the switch, thus introducing harmonic distortion. Increasing the channel length is an effective solution to reduce the sub-threshold leakage current. To further reduce the leakage current, we have utilized a two-transistor stack [19] (shown in 0). 0 shows the simulated sub-threshold leakage currents of two different switches versus their input voltages. The figure compares the leakage current of a single transistor with a channel length of $4L_{min}$ to two transistors in series with channel lengths of $2L_{min}$. It can be seen that the stacked transistors show lower leakage for small input voltages in the range from 0 V to 0.1 V.

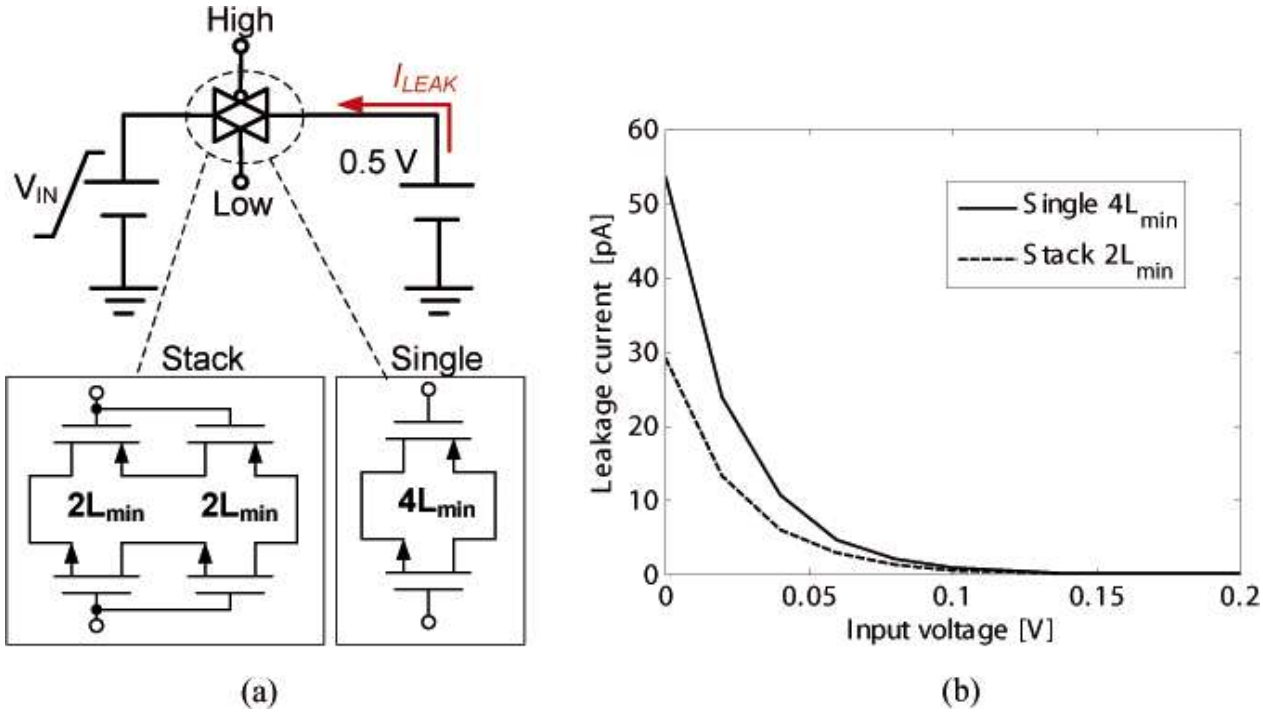

Fig. 7: Simulated leakage current of the sampling switch: (a) test-bench (b) leakage current versus input voltage

To determine the channel length of the stacked transistors, the sampling circuit was simulated at 1-kHz sampling frequency with full-range input signal for three different switch lengths (L_{min}+L_{min}, $2L_{min}$+$2L_{min}$, and $3L_{min}$+$3L_{min}$). The frequency of the input signal was swept from near-DC to near-Nyquist bandwidth. The voltage of the sampled output signal was recorded at the end of the hold phase to track the voltage drop. The simulated worst-case signal-to-noise-and-distortion ratio (SNDR) of the recorded voltage was found at near-Nyquist operation. The results of SNDR for three different switch lengths were 60.9 dB, 67.4 dB, and 67.5 dB, respectively. Thus increasing the total channel length beyond $4L_{min}$ ($2L_{min}$+$2L_{min}$) did not introduce much benefit for the leakage reduction. Hence, in this work, the channel length of the stacked transistors was chosen to be $2L_{min}$ (0.26μm).

Furthermore, we sized the transistor width and simulated the switch R_{ON} over the entire input range under -40°C at the slow process corner. The simulated maximum R_{ON} based on the chosen transistor widths (0.3μm for NMOS and 1.1μm for PMOS) is about 80 kΩ. With the total array capacitance of 14 pF, the f_{3dB} of the sampling circuit is then calculated to be about 140 kHz, which gives a design margin with more than four times the required minimum f_{3dB}.

At the bottom-plate sides, inverters connect the capacitors to the power rails. Ideally, minimum-size transistors can be used for all the inverters because of the low sampling rate, thus minimizing power consumption. In practice, however, special care must be taken during sizing of the MSB inverter. The NMOS top-plate sampling switch introduces parasitic PN-junction on the top-plate node. After an input voltage close to ground is sampled, during the MSB to MSB-1 transition, the voltage on the top-plate node can undershoot below ground, forward-biasing the PN-junction and causing charge loss. To avoid the undershoot voltage, the PMOS transistor in the MSB inverter was sized up to six times the minimum width.

C. Dynamic Latch Comparator

The dynamic latch comparator [20] is shown in 0. Buffers have been used to make the output loading identical, followed by an SR latch which stores the comparison result for the entire clock cycle.

Since the input common-mode voltage of the comparator is kept at mid-rail voltage, the total comparator offset appears as static offset, which does not affect the linearity of the ADC [11]. The fundamental limitation on the achievable comparator resolution is thermal noise, which has the usual form as *kT/C* [21][22]. The post-layout extracted capacitor at the comparator output is

about 10 fF, which makes the thermal noise of the comparator in the same order as the quantization noise of the ADC [10].

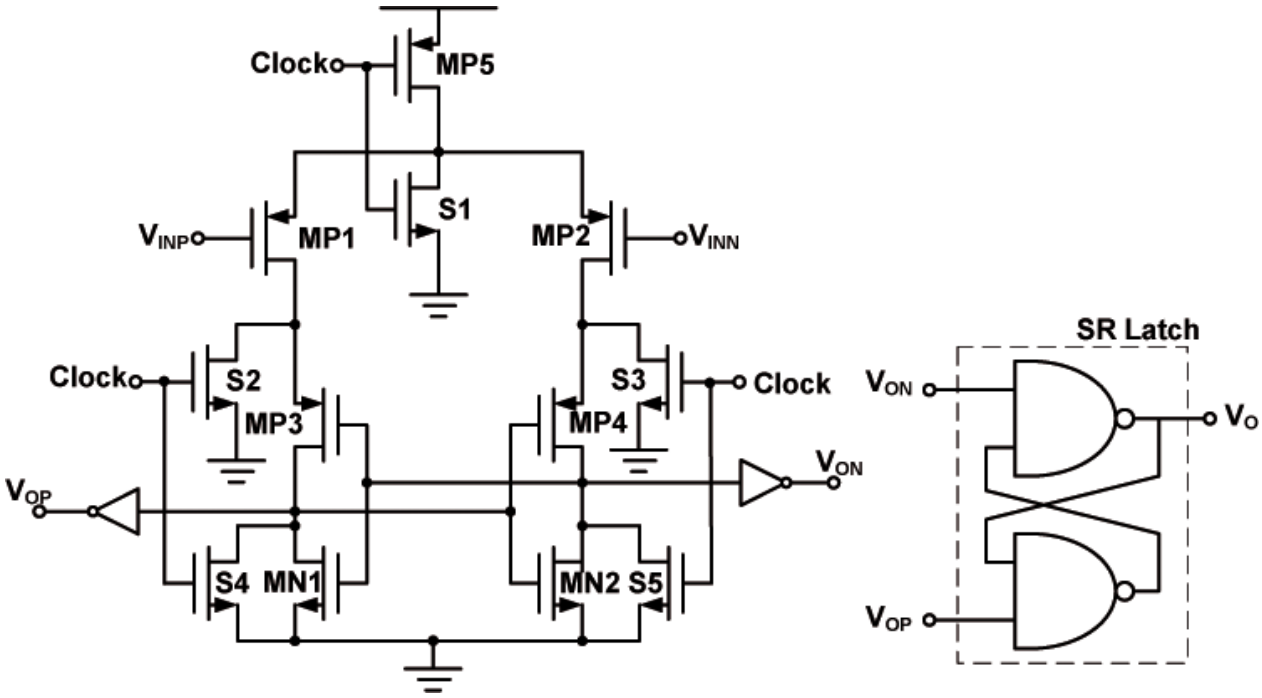

Fig. 8: Dynamic latch comparator [20] and its succeeding SR latch

Though the offset of the comparator does not affect the accuracy, it will decrease the input voltage range, thus degrading the signal-to-noise ratio. Monte Carlo simulations of the comparator offset showed a mean offset of 7.8 mV and a standard deviation of 9.1 mV. Assuming 3σ is considered, it results in a total offset voltage of 35.1 mV, decreasing the SNR by 0.31 dB. The decreased SNR introduces a loss of 0.05-ENOB, which is acceptable in this work.

D. SAR Control Logic

For low power SAR control logic, we investigated both synchronous and asynchronous solutions. Asynchronous processing [23] has been frequently used for high-speed SAR ADCs in order to avoid a high-frequency system clock. The SAR control logic starts the conversion on the

rising edge of a sampling clock, and triggers the internal comparison from MSB to LSB successively. The delay, usually generated by an inverter line [10], has a large dependency on process, voltage, and temperature variations, which makes it difficult to ensure the DAC settling. Moreover, the short-circuit currents caused by the slow transition of the inverters introduce extra power [10].

The proposed ADC utilizes a synchronous SAR logic, shown in 0. It generates the sample signal and the switch control signals for the DAC. The operation of its multiple-input 10-bit shift resister is similar to [24]. A 4-bit counter and a decoder generate the control signals for the 10-bit shift register. The entire logic uses 16 transmission-gate flip-flops and the decoder has been optimized for minimum logic depth and gate count. 0 shows the time sequence of the SAR logic. A 12-kHz system clock has been used, and the sampling clock of 1 kHz is generated by the SAR logic.

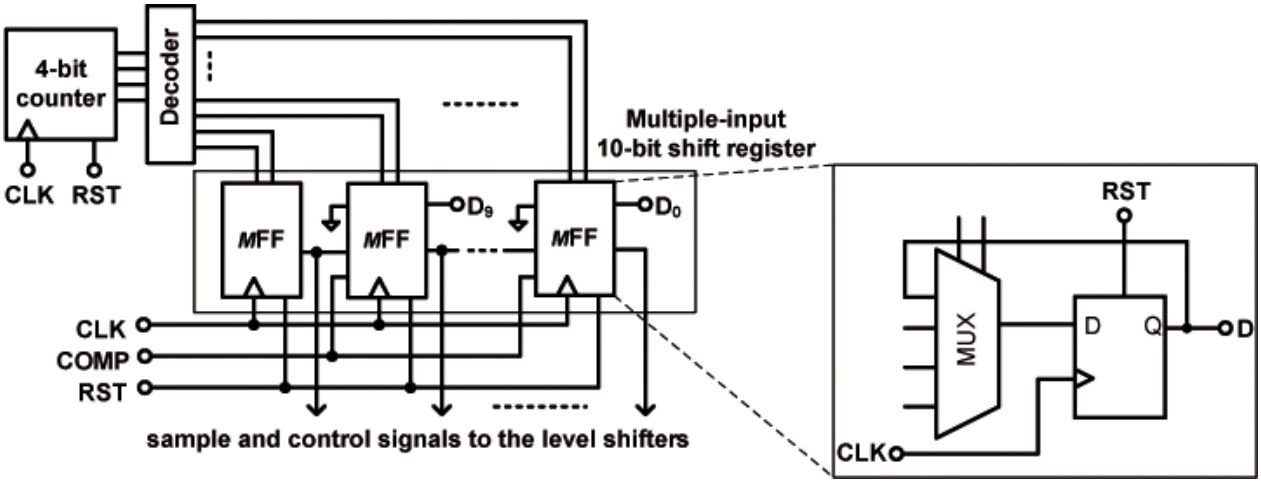

Fig. 9: SAR logic.

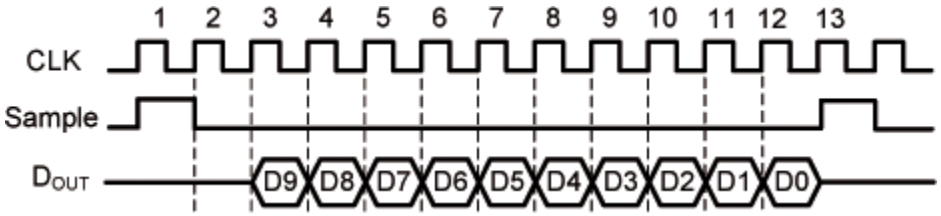

Fig. 10: Time sequence of the synchronous SAR control logic.

Since the operating frequency of the SAR logic is 12 kHz, and its switching activity is not high, the leakage power dominates the total power. Several techniques have been used to reduce the leakage currents, including increased channel length, minimum transistor width, and replacing the gate transistors with stacked pairs [25].

To further reduce the switching and leakage power consumption, a dual-supply voltage scheme has been employed, allowing the SAR logic to operate at 0.4 V. The level shifter [26], shown in 0, has been used to convert the logic levels between the SAR and the analog parts. In the entire ADC, twelve level shifters have been used: ten for the DAC control signals, one for the sampling signal of the top-plate switch, and one for the clock signal of the comparator.

IV. Measurement Results

The prototype SAR ADC with a core area of 357 × 536 μm^2 was designed and fabricated in a general purpose 0.13-μm one-poly six-metal (1P6M) CMOS process. It was packaged in a 1.27 mm pitch JLCC package. A photograph of the chip is shown in 0. The unmarked part around the ADC core includes the decoupling capacitors and the I/O buffers for the pads.

Histogram test [27] was conducted to measure the linearity of the ADC. A full-swing, differential sinusoidal input near DC frequency with amplitude of 1 V was applied to the 1-kS/s

ADC. 0 shows the measured DNL and INL error with respect to the output code. The peak DNL error is +0.54/-0.61 LSB, and the peak INL error is +0.45/-0.46 LSB.

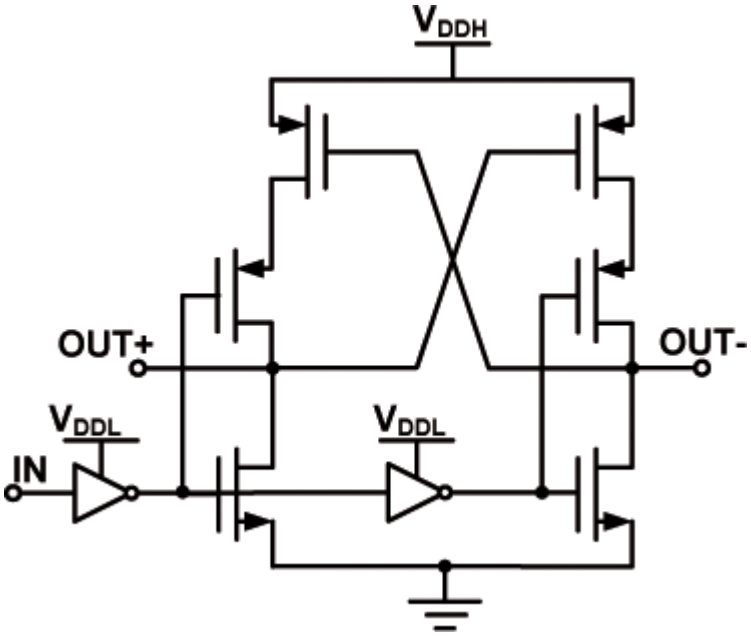

Fig. 11: Level shifter [26].

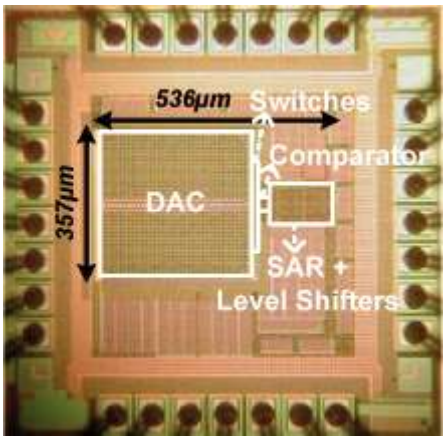

Fig. 12: Die photograph of the ADC in 0.13-μm CMOS technology.

The SNDR of the ADC was measured using tone testing. A fast Fourier transform (FFT) of the 1-kS/s ADC at near-Nyquist operation is shown in 0. The amplitude of the test stimulus was set to -0.5 dBFS. The measured SNDR is 56.7 dB, providing an effective number of bits (ENOB)

of 9.1 bits. 0 shows the ENOB of this ADC with respect to the input frequency, where the ENOB remains almost constant over the entire bandwidth. Hence, the effective resolution bandwidth (ERBW) is higher than the Nyquist bandwidth.

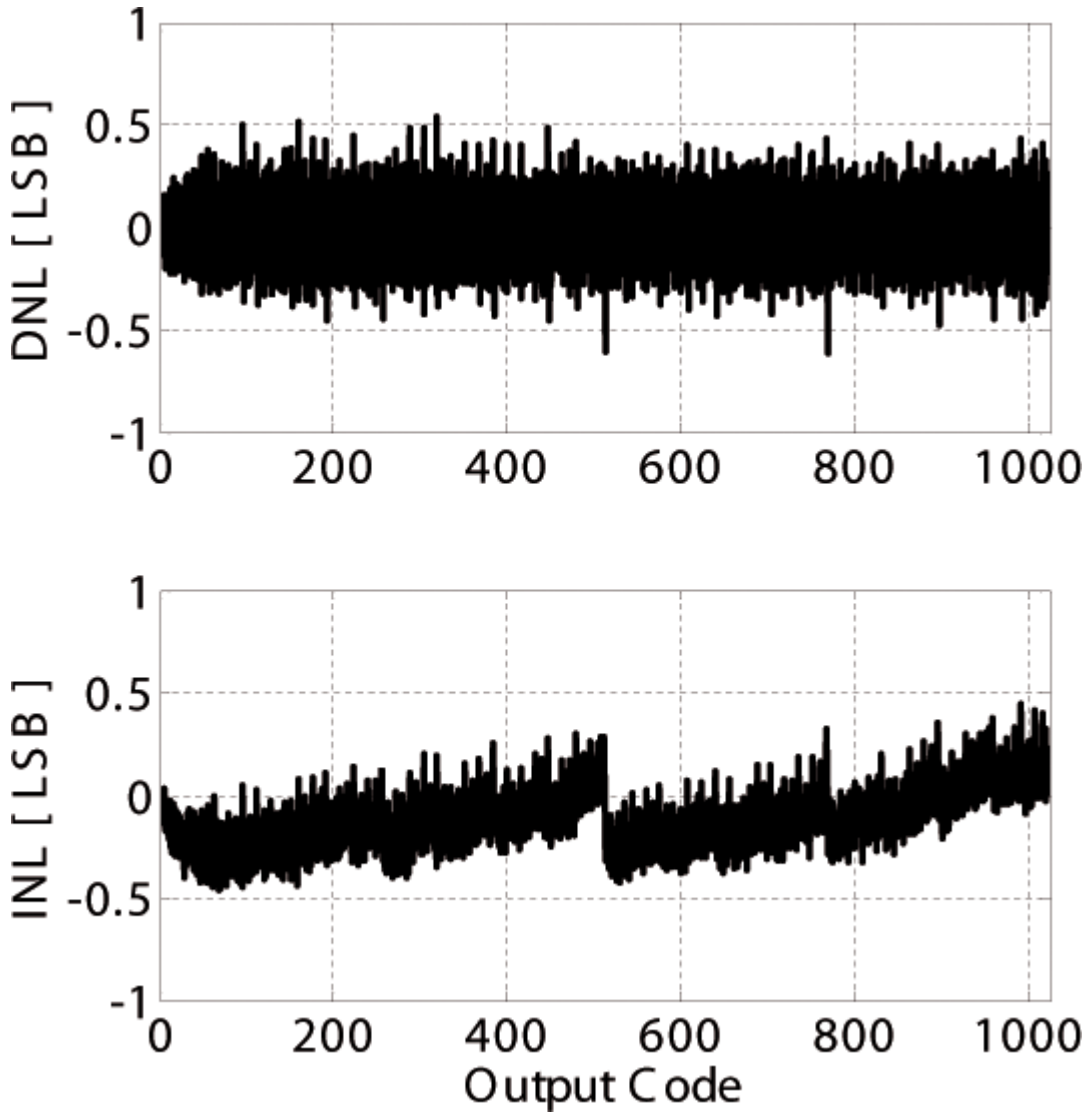

Fig. 13: Measured DNL and INL errors.

Multiple supply voltage domains were utilized, allowing detailed measurement of the power consumption in the DAC, comparator, and SAR control logic, respectively. The total measured power consumption of the 1-kS/s ADC is 53 nW in dual-supply mode (V_{DDH} of 1.0 V for DAC

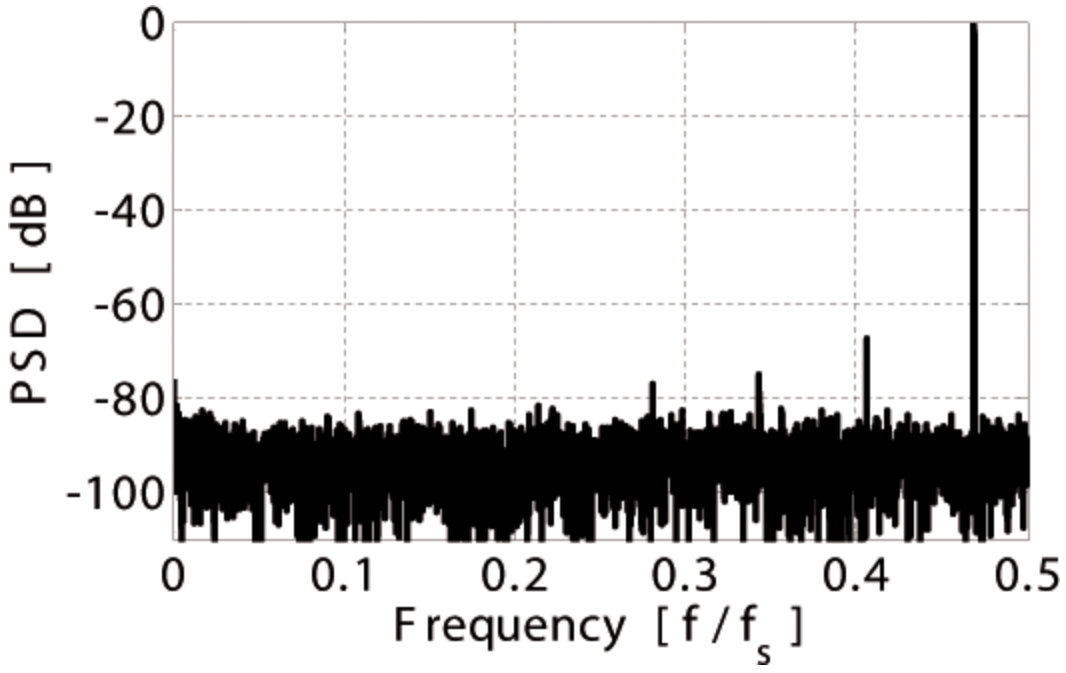

Fig. 14: Measured 8,192-point FFT spectrum at 1 kS/s.

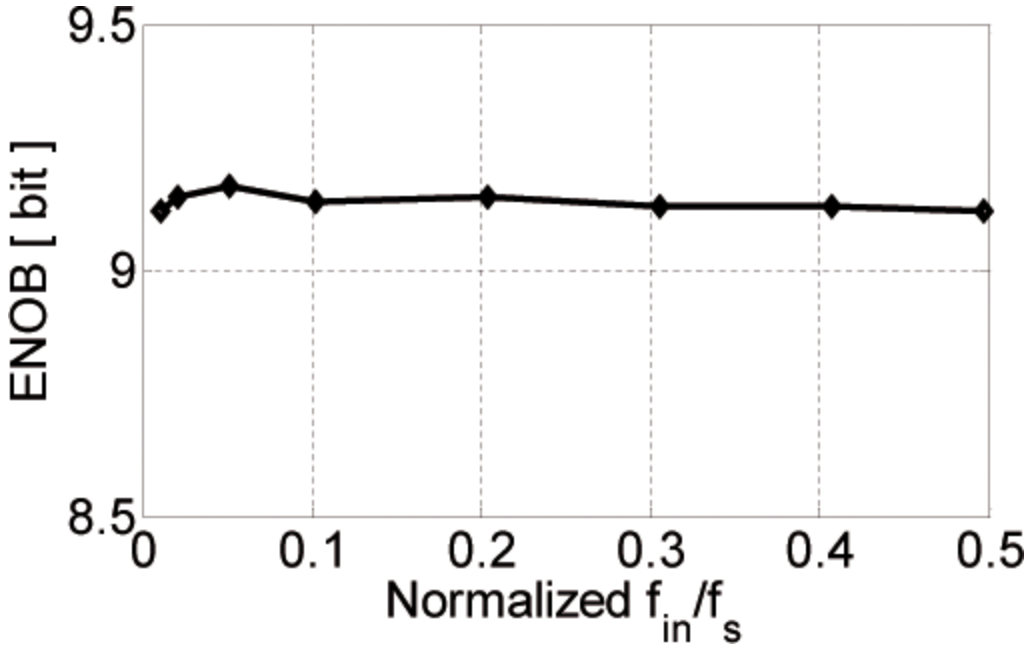

Fig. 15: ENOB of the ADC versus input frequency.

and comparator, and V_{DDL} of 0.4 V for SAR logic) and 72 nW in 1-V single-supply mode. The measured leakage power of the digital part is 13 nW in dual-supply mode and 22 nW in 1-V single-supply mode, which constitutes 25% and 31% of the total power, respectively. It implies that the digital leakage power consumption is a major contributor to the total power. The power of the level shifters was simulated based on post-layout extraction. In dual-supply mode, the level shifters consume 12 nW power and in 1-V single-supply mode, they consume 10 nW power. Excluding the 10-nW power of level shifters from the total 72-nW power in the single-supply mode would result in a total ADC power of 62 nW. This indicates that the voltage scaling has reduced the overall power consumption of the ADC by 15% without any loss in performance. 0 shows the power breakdown of the ADC in the two modes. Table I summarizes the measured performance of the ADC.

The power and dynamic performance of the 1-kS/s ADC under different supply settings were measured. The figure-of-merit (FOM) which has been used to compare the ADC performance is defined as

$$FOM = \frac{Power}{\min\{f_S, 2 \times ERBW\} \times 2^{ENOB}} \tag{7}$$

Table II shows the measurement results together with the corresponding FOM. The ADC achieves the optimal performance at V_{DDH} = 1.0 V and V_{DDL} = 0.4 V with the lowest FOM of 94.5 fJ/Conversion.

As demonstrated in this work, at such low-sampling rates, leakage power becomes a significant portion of the total power, degrading the FOM as compared to ADCs for higher sampling rates. Therefore, Table III compares the measurement results of this work to previously

TABLE I ADC MEASUREMENT SUMMARY

ADC Performance		
Technology	0.13-μm CMOS	
Sampling Rate	1 kS/s	
Die Area	357 × 536 μm^2	
DNL	+0.54 / -0.61 LSB	
INL	+0.45 / -0.46 LSB	
SNDR (at Nyquist)	56.7 dB	
SFDR (at Nyquist)	67.6 dB	
ADC Power Breakdown		
Supply Voltage		
Comparator, DAC	1.0 V	1.0 V
SAR	0.4 V	1.0 V
Comparator	2 nW	2 nW
Capacitive DAC	33 nW	33 nW
Control Logic (SAR + Level Shifter)	18 nW	37 nW
Total Power	53 nW	72 nW

TABLE II ADC PERFORMANCE UNDER DIFFERENT SUPPLY SETTINGS

V_{DDH} / V_{DDL} [V]	*0.8/0.4*	*1.0/0.4*	*1.0/1.0*	*1.2/1.2*
Power [nW]	45	53	72	94
ENOB (at Nyquist) [bit]	8.7	9.1	9.1	9.2
FOM [fJ/Conv.]	108.1	94.5	129.4	159.8

TABLE III ADC COMPARISON

Author/ Year	Sauerbrey 2003 [28]	Bechen 2006 [29]	Zou 2009 [30]	This Work
Technology [µm]	0.18	0.8	0.35	0.13
Sampling Rate [kS/s]	4.1	0.8	1 †	1
Power [nW]	850	3000	230	53
ENOB [bit]	6.9	9	10.2	9.1
FOM [fJ/Conv.]	1700	7300	195	94.5

† The sampling rate of 1 kS/s was reported in [31] and referred in [30] by the same authors.

published SAR ADCs with comparable sampling rates [28]-[30]. As the table shows, this ADC achieves the lowest power and FOM.

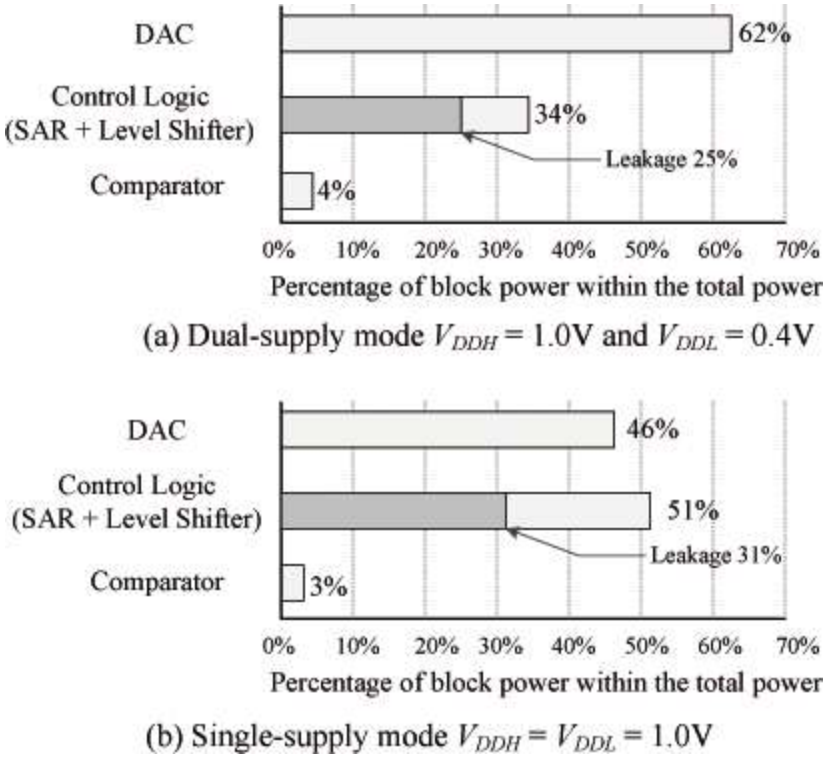

Fig. 16: The ADC power breakdown in dual and single supply modes, where the percentage of digital leakage power is indicated by dark color.

V. CONCLUSION

In this paper, we have presented an ultra-low-power SAR ADC in 0.13-μm CMOS technology for medical implant devices. The ADC achieves 9.1 ENOB with a power consumption of 53 nW at a sampling rate of 1 kS/s. It utilizes an ultra-low power design strategy, imposing maximum simplicity on ADC architecture, low transistor count, low leakage circuit techniques, and a matched capacitive DAC with a switching scheme which results in full-range sampling without switch bootstrapping and extra reset voltage. Furthermore, a dual-supply scheme allows the SAR logic to operate at 0.4 V, resulting in 15% power reduction compared to

the 1-V single-supply mode without any loss in ADC performance. The paper has also shown that at such low-sampling rates, leakage power can be a significant portion of the total ADC power consumption, degrading the energy efficiency and FOM.

References

[1] L. S. Y. Wong, S. Hossain, A. Ta, J. Edvinsson, D. H. Rivas, and H. Nääs, "A very low-power CMOS mixed-signal IC for implantable pacemaker applications," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2446-2456, Dec. 2004.

[2] J. G. Webster, *Medical Instrumentation Application and Design*, Wiley, 1998.

[3] D. Zhang, A. Bhide, and A. Alvandpour, "A 53-nW 9.12-ENOB 1-kS/s SAR ADC in 0.13-µm CMOS for medical implant devices," in *Proc. ESSCIRC*, pp.467-470, Sep. 2011.

[4] F. Kuttner, "A 1.2V 10b 20MSample/s non-binary successive approximation ADC in 0.13 µm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, pp.176-177, Feb. 2002.

[5] W. Liu, P. Huang, and Y. Chiu, "A 12b 22.5/45MS/s 3.0mW 0.059 mm^2 CMOS SAR ADC achieving over 90dB SFDR," in *IEEE ISSCC Dig. Tech. Papers*, pp.380-381, Feb. 2010.

[6] C. C. Liu, S. J. Chang, G. Y. Huang, Y. Z. Lin, C. M. Huang, C. H. Huang, L. Bu, and C. C. Tsai, "A 10b 100MS/s 1.13mW SAR ADC with binary-scaled error compensation," in *ISSCC Dig. Tech. Papers*, pp.386-387, Feb. 2010.

[7] Y. Chen, X. Zhu, H. Tamura, M. Kibune, Y. Tomita, T. Hamada, M. Yoshioka, K. Ishikawa, T. Takayama, J. Ogawa, S. Tsukamoto, and T. Kuroda, "Split capacitor DAC mismatch calibration in successive approximation ADC, " in *Proc. IEEE Custom Integrated Circuit Conf.*, pp. 279-282, Sep. 2009.

[8] M. Yoshioka, K. Ishikawa, T. Takayama, and S. Tsukamono, "A 10-b 50-MS/s 820-µW SAR ADC with on-chip digital calibration," in *IEEE ISSCC Dig. Tech. Papers*, pp.384-385, Feb. 2010.

[9] B. P. Ginsburg and A. P. Chandrakasan, "500-MS/s 5-bit ADC in 65-nm CMOS with split capacitor array DAC," *IEEE J. Solid-State Circuits*, vol. 42, no.4, pp. 739-747, April 2007.

[10] M. van Elzakker, E. van Tujil, P. Geraedts, D. Schinkel, E. A. M. Klumperink, and B. Nauta, "A 10-bit charge-redistribution ADC consuming 1.9 µW at 1 MS/s," *IEEE J. Solid-State Circuits*, vol. 45, no.5, pp. 1007-1015, May 2010.

[11] C. C. Liu, S. J. Chang, G. Y. Huang, and Y. Z. Lin, "A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure," *IEEE J. Solid-State Circuits*, vol. 45, no.4, pp. 731-740, April 2010.

[12] J. L. McCreary and P. R. Gray, "All-MOS charge-redistribution analog-to-digital conversion techniques–Part I," *IEEE J. Solid-State Circuits*, vol. SC-10, pp. 371-379, Dec. 1975.

[13] N. Verma and A. P. Chandrakasan, "An ultra low energy 12-bit rate-resolution scalable SAR ADC for wireless sensor node," *IEEE J. Solid-State circuits*, vol. 42, no. 6, pp. 1196-1205, Jun. 2007.

[14] M. Yip and A. P. Chandrakasan, "A resolution-reconfigurable 5-to-10b 0.4-to-1V power scalable SAR ADC," in *IEEE ISSCC Dig. Tech. Papers*, pp.190-191, Feb. 2011.

[15] Y. Zhu, C. H. Chan, U. F. Chio, S. W. Sin, S. P. U, R. P. Martins, and F. Maloberti , "A 10-bit 100-MS/s reference-free SAR ADC in 90 nm CMOS, " *IEEE J. Solid-State circuits*, vol. 45, no. 6, pp. 1111-1121, Jun. 2010.

[16] M. Saberi, R. Lotfi, K. Mafinezhad, and W. A. Serdijn, "Analysis of power consumption and linearity in capacitive digital-to-analog converters used in successive approximation

ADCs," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, no. 8, pp. 1736 -1748, Aug. 2011.
[17] T. Wakimoto, H. Li, and K. Murase, "Statistical analysis on the effect of capacitance mismatch in a high-resolution successive-approximation ADC", *IEEJ Trans. on Electrical and Electronic Engineering*, vol. 6, pp. s89–s93, 2011.
[18] R. Schreier, J. Silva, J. Steensgaard, and G. C. Temes, "Design-oriented estimation of thermal noise in switched-capacitor circuits," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 52, no. 11, pp. 2358 - 2368, Nov. 2005.
[19] K. Ishida, K. Kanda, A. Tamtrakarn, H. Kawaguchi, and T. Sakurai, "Managing subthreshold leakage in charge-based analog circuits with low-V_{TH} transistors by analog T-swtich (AT-Switch) and super cut-off CMOS (SCCMOS)", *IEEE J. of Solid-State Circuits*, vol. 41, no. 4, pp.859-867, April 2006.
[20] G. Van der Plas and B. Verbruggen, "A 150MS/s 133µW 7b ADC in 90nm digital CMOS using a comparator-based asynchronous binary-search sub-ADC," in *ISSCC Dig. Tech. Papers*, pp.242-243, Feb. 2008.
[21] J. Kim, B. Leibowitz, J. Ren. and C. Madden, "Simulation and analysisof random decision errors in clocked comparators," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 56, no. 8, pp. 1844 -1857, Aug. 2009.
[22] P. Nuzzo, F. De Bernardinis, P.Terreni, and G. Van der Plas, "Noise analysis of regenerative comparators for reconfigurable ADC architecture," *IEEE Trans. Circuits Syst. II*, vol. 55, no.6, pp. 1441–1454, Jul. 2008.
[23] S. W. M. Chen and R. W. Brodersen, "A 6-bit 600-MS/s 5.3-mW asynchronous ADC in 0.13-µm CMOS," *IEEE J. Solid-State Circuits*, vol. 41, no.12, pp. 2669-2680, Dec. 2006.
[24] A. Rossi and G. Fucilli, "Nonredundant successive approximation register for A/D converters," *Electronics Letters*, vol. 32, no. 12, pp. 1055-1056, June 1996.
[25] S. Narendra, V. De, S. Borkar, D. A. Antoniadis, A. P. Chandrakasan, "Full-chip subthreshold leakage power prediction and reduction techniques for sub-0.18-μm CMOS", *IEEE J. of Solid-State Circuits*, vol. 39, no. 2, pp.501-510, Feb. 2004.
[26] C. Q. Tran, H. Kawaguchi, and T. Sakurai, "Low-power high-speed level shifter design for block-level dynamic voltage scaling environment," in *International Conference on Integrated Circuit Design and Technology*, pp. 229-232, May 2005.
[27] J. Doernberg, H.-S. Lee, and D. A. Hodges, "Full-speed testing of A/D converters," *IEEE J. Solid-State Circuits*, vol. SC-19, no.6, pp. 820-827, Dec. 1984.
[28] J. Sauerbery and D. Schmitt-Landsiedel, "A 0.5-V 1-µW successive approximation ADC", *IEEE J. of Solid-State Circuits*, vol. 38, no. 7, pp.1261-1265, July 2003.
[29] B. Bechen, D. Weiler, T. v. d. Boom, and B.J. Hosticka, "A 10 bit very low-power CMOS SAR-ADC for capacitive micro-mechanical pressure measurement in implants," *Advances in Radio Science*, Vol. 4, pp. 243-246, 2006.
[30] X. Zou, X. Xu, L. Yao, and Y. Lian, "A 1-V 450-nW fully integrated programmable biomedical sensor interface chip," *IEEE J. Solid-State Circuits*, vol. 44, no.4, pp. 1067-1077, April 2009.
[31] X. Xu, X. Zou, L. Yao, and Y. Lian, "A 1-V 450-nW fully integrated biomedical sensor interface system," in *Proc. Symposium VLSI Circuits*, pp. 78-79, June 2008.