A 540–640-GHz High-Efficiency Four-Anode Frequency Tripler

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***Abstract*—We report on the design and performance of a broad-band, high-power 540–640-GHz fix-tuned balanced frequency tripler chip that utilizes four planar Schottky anodes. The suspended strip-line circuit is fabricated with a 12-μm-thick support frame and is mounted in a split waveguide block. The chip is supported by thick beam leads that are also used to provide precise RF grounding. At room temperature, the tripler delivers 0.9–1.8 mW across the band with an estimated efficiency of 4.5%–9%. When cooled to 120 K, the tripler provides 2.0–4.2 mW across the band with an estimated efficiency of 8%–12%.**

***Index Terms*—Balanced tripler, frequency multiplier, frequency tripler, local oscillator, planar diode, Schottky diode, sextupler, submillimeter wavelengths, varactor.**

I. Introduction

SOURCES for submillimeter wavelengths have been the subject of intense research for several decades [1]. Backward-wave oscillators (BWOs), also known as "O-Carcinotrons," introduced in the late 1950s [2], are versatile since they are sweepable, can produce several milliwatts above 300 GHz, and can operate above 1 THz. Unfortunately, they are difficult to build, bulky, and require high-voltage power supplies and external cooling. Also, their lifetimes may be only a few hundred hours if they are used at their full potential. Miniaturized klystrons, using nano-tubes, and micromachining techniques are being investigated to try to push tube technology into the terahertz regime. Whether these efforts will yield successful submillimeter-wave oscillators remains to be seen [3]. For applications that require power levels in the range of a few microwatts, sideband generators can provide the desired continuous frequency coverage by beating a submillimeter-wave laser and a continuous millimeter source [4]. When quantum cascade laser (QCL) technology [5] reaches maturity, QCLs could be used to create low-power all-solid-state terahertz tunable sources.

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Technological advances in submillimeter-wave sources have been mainly driven by the build-up of ground-based and space-borne heterodyne receivers for astrophysics and planetary science. The Heterodyne Instrument for the Far Infrared (HIFI) of the Herschel Space Observatory [6] and, more recently, the Atacama Large Millimeter Array (ALMA) [7], are two instruments that have focused research and development in this field. Both use sensitive heterodyne receivers incorporating superconductor insulator superconductor (SIS) mixers [8], [9] or hot electron bolometer (HEB) mixers [10] that require low local oscillator (LO) power. Photo mixing in nonlinear crystals of two phase-locked laser beams is an interesting solution to provide low-power LO sources [11] and can potentially be distributed in-phase to several mixers [12]. For SIS mixers, another interesting possibility is to use flux flow oscillators [13] to provide on-chip LO sources. However, to date, the most common way to build frequency-tunable sources at submillimeter wavelengths is by frequency multiplication. This solution is used for all of the LOs for HIFI and ALMA.

Within the semiconductor frequency multiplier field, several competing technologies have been demonstrated. Heterostructure barrier varactors (HBV), first introduced in [14], produce only odd harmonics of an incident signal due to their internal symmetry. Thus, they are attractive devices to design high-order odd harmonic multipliers such as triplers [15], [16] or quintuplers that can reach conversion efficiencies up to 5% at 210 GHz [17]. Another technique to build devices that exhibit internal symmetries was recently explored in [18]. It gave a state-of-the-art conversion efficiency of 22% for a 230-GHz planar diode tripler. Nevertheless, for millimeter- and submillimeter-wave frequency multipliers, Schottky planar varactors are still providing the best performance in terms of efficiency, output power, and instantaneous bandwidth. Planar Schottky diodes were introduced over a decade ago [19], [20] and now have been successfully demonstrated well into the terahertz range [21]–[26], replacing whisker-contacted Schottky diodes [27]–[29].

Balanced doublers, proposed and demonstrated in [30]–[33], have become the standard topology for frequency multiplication due to their good performance. Significant progress has been made since that time both in device fabrication technology and design methodology. The devices have become MMIC-like and consequently have been able to work well at submillimeter wavelengths. One device fabrication technology consists of transferring the epilayer on quartz (or some other application-optimized substrate) to decrease the losses and dispersion or, on high thermal conductivity substrates, to address heat dissipation issues [34]. An alternative approach is to decrease dielectric loading by removing most of the substrate from the chip [35], [36] or by using GaAs membrane technology

[21]–[26]. The introduction of beam leads to facilitate chip handling and placement and provide more precise RF and dc grounding brought significant further improvement to this technology [37].

Planar Schottky balanced frequency triplers were introduced at millimeter wavelengths in [38] and at submillimeter wavelengths in [39]. They share the same technology as the doublers but their performance has been somewhat overshadowed by the success of balanced doublers. Recently, they have been demonstrated to work at terahertz frequencies with record output power and bandwidth [22], [24], [26].

The purpose of this study was to determine if Schottky balanced triplers could compete with balanced doublers in terms of bandwidth, flatness, power handling, and output power below 1 THz. The ultimate goal was to design a tripler in the 540–640-GHz band to be used as a driver for LO chains to the 1650–1910-GHz band, where a number of spectral lines of astrophysical interest lie, such as the ionized carbon fine structure line at 1900.5 GHz. The multiplier was originally designed to deliver 2.5 mW from an input power low enough to never put the diodes at risk. Power handling was therefore a very important issue. These specifications had to be met at 120 K, which is the expected operating temperature of the LO subsystem on HIFI.

II. Design Topology

An efficient topology for submillimeter-wave balanced triplers has been demonstrated in [39]. The present design, however, adopted a configuration used in [38] at millimeter wavelengths and more recently at terahertz frequencies [21], [22], [26] that has the advantage of allowing four or more anodes per chip, dramatically increasing power handling capabilities and consequently the output power.

The tripler is a split-block waveguide design that features four Schottky planar varactor diodes, monolithically fabricated on a GaAs-based substrate and connected in series at dc (see Fig. 1). The anodes are about 2 μm $\times$ 3 μm, the mesas are about 100 μm^2, and the doping of the epilayer is 1.10^{17} cm^{-3}. The chip is inserted between the input and the output waveguides in a channel of 80 μm $\times$160 μm cross section and approximately 600 μm long. An E-plane probe located in the input waveguide couples the signal at the fundamental frequency to a suspended microstrip line that can propagate only a true TEM mode (as explained later in this section, no dielectric is present). This line has several sections of low and high impedance used to match the diodes at the input and output frequency and to prevent the third harmonic from leaking into the input waveguide. The third harmonic produced by the diodes is coupled to the output waveguide by a second E-plane probe.

Inside the chip channel, the circuit is quasi-symmetrical (small asymmetries are introduced by the physical structure of the Schottky diodes). The fundamental excites the diodes on one side of the symmetry line 180° out of phase with respect to the diodes on the opposite side. As a result, the even harmonics are generated on a TE mode while the odds harmonics are generated on a TEM mode. Consequently, to balance the circuit, it is necessary to cut off the parasitic TE mode at the second harmonic by adequately dimensioning both the cross section of the chip channel and the width of the suspended microstrip line. The second harmonic is then trapped in a virtual loop, i.e., the line of diodes. More detail about this topology can be found in [40].

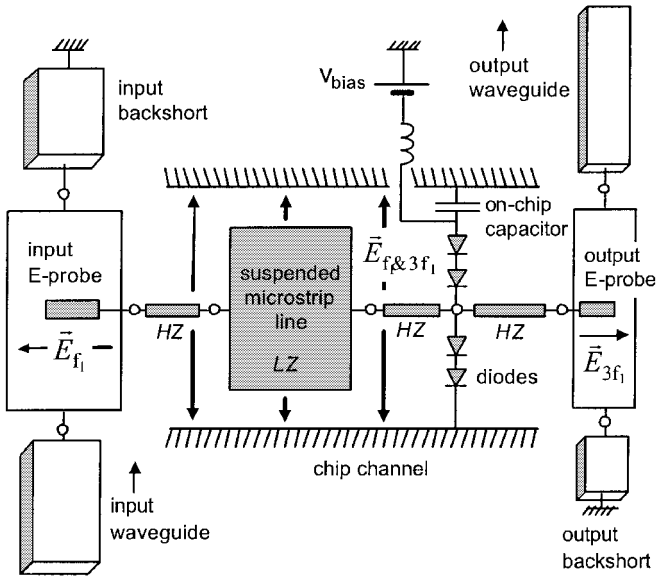

Fig. 1. Block diagram of the 600-GHz balanced tripler. Additional waveguide sections of different impedances and lengths (not shown) are used for the input and output matching. HZ and LZ stand, respectively, for high and low impedance. $\vec{E}_{f_1}$, $\vec{E}_{3f_1}$ and $\vec{E}_{f_1\&3f_1}$ stand, respectively, for the electric field at the fundamental frequency f_1, at the output frequency $3f_1$, and both at the input and output frequency.

The circuit features additional matching elements in the input and output waveguides, made with a succession of waveguide sections of different heights and lengths. The output waveguide is dimensioned to cut off any residual leakage at the second harmonic. The second harmonic at the high end of the design band is at 426.7 GHz. The output waveguide was dimensioned to cut off any signal below 500 GHz. This will allow for fabrication margins and yet not affect the signal at 540 GHz, which is the low end of the design band.

Thanks to this topology, the bias scheme is very simple. It consists of an on-chip capacitor at one end of the series of diodes near a narrow aperture in the wall of the chip channel. Extensive simulations were done to confirm that the bias circuit has almost no impact at RF frequencies.

The chip was fabricated using Jet Propulsion Laboratory (JPL) substrateless technology [25], [37], which consists of removing the substrate in the center part of the circuit and leaving only a frame that supports the diodes at one end. In this design, three out of four sides of the supporting frame are outside the chip channel. To fit in the waveguide block, this frame requires that two slots be machined parallel to the channel.

The chip incorporates suspended stripline circuitry held by a 12-μm thick frame and suspended above the bottom half of the channel by thick gold beam leads spaced around the substrate. Two of these beam leads provide the required dc and RF connections for the diodes when clamped between the two halves of the split block. Figs. 2 and 3 show the structure of the multiplier, while Fig. 4 shows details of the diode area.

III. Design Optimization

This section will present a practical methodology that was used to design a wide-band, fix-tuned, high-efficiency fre-

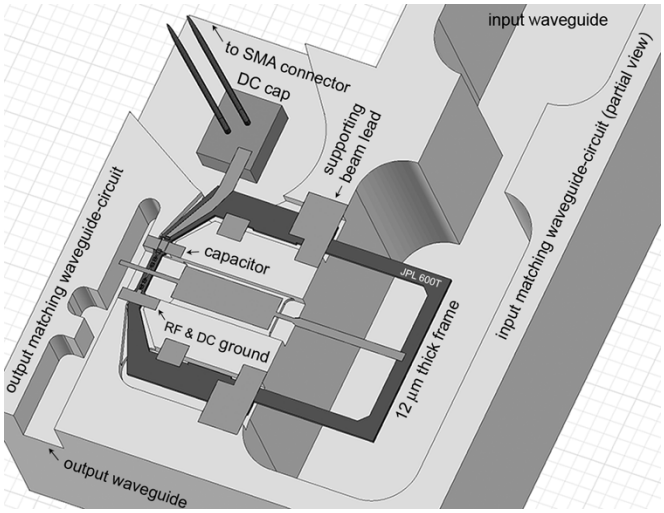

Fig. 2. Three-dimensional view of the bottom part of the waveguide block with the 600-GHz tripler chip and the dc capacitor. The top part of the waveguide block (not shown) is symmetrical. The complete input matching waveguide circuit (cut off in the figures) consists of four reduced-height rectangular waveguide sections and four standard-height rectangular waveguide sections.

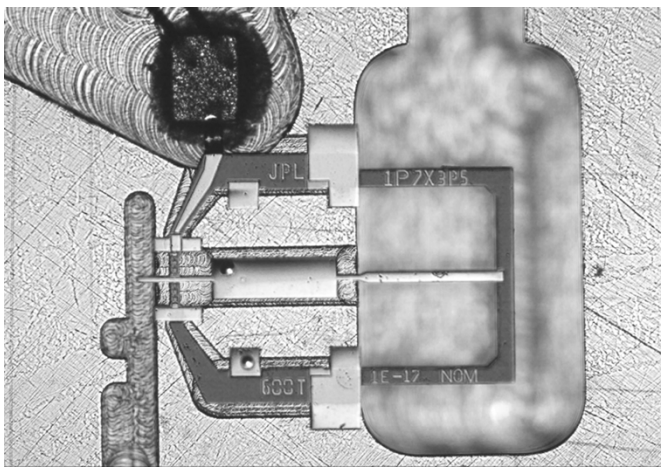

Fig. 3. Photograph of the bottom part of the waveguide block with a 600-GHz tripler chip and the dc capacitor installed.

quency tripler at 600 GHz. While a number of concepts defined in [33] for balanced doublers are utilized for this optimization, a number of significant points must be addressed for the current balanced tripler design.

Design Methodology: Usually, the first step in the design of a frequency multiplier is to determine the characteristics of the diodes along with the operating conditions that best suit the application. In this case, it consists of optimizing the doping level, the anode dimensions, and the bias voltage for a given input power. Once these parameters are fixed and the optimum embedding impedances of the diodes are determined, a linear circuit can be synthesized [41].

For the design of the 540–640-GHz tripler, the chip topology as well as the diode characteristics are iteratively modified until a suitable compromise is achieved between the efficiency and bandwidth. Commercially available harmonic balance software codes are used to carry out the optimization. During this design

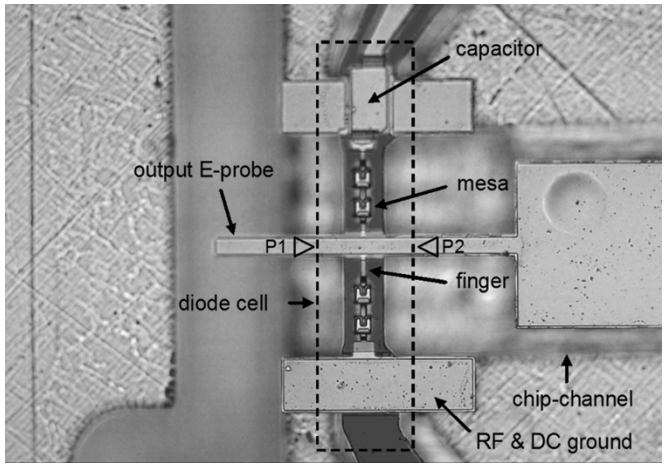

Fig. 4. Detail of the 600-GHz tripler chip showing the four anodes, the on-chip capacitor, the output E-probe and part of the on-chip matching circuit. The dashed line rectangle defines the diode cell used for the first step of optimization. P1 and P2 define the localization of the HFSS wave ports used in the simulations (see Section III).

process, it is important to make sure that coupling balance between the anodes is preserved and realistic circuit losses are accounted for. Contrary to the balanced doublers proposed in [30], both the input and the output signals propagate with the same mode in the region immediately around the diodes. Therefore, a filter is required and it can be optimized more easily using the nonlinear simulations.

Nonlinear Modeling of the Schottky Diode: Abundant literature is available about the modeling of Schottky diodes at millimeter and submillimeter wavelengths working at room temperature [42]–[47] and at cryogenic temperatures [48]. For this design, we use a simplified electrical model, consisting of a nonlinear junction capacitance C_j in parallel with a nonlinear conductance G_j and in series with a resistance R_s.

1) The junction capacitance is classically modeled as follows [49]:

$$\text{for } V \leq \frac{V_j}{2}, \qquad C_j(V) = \frac{A\varepsilon_s}{t(V)} \tag{1}$$

where

$$t(V) = \sqrt{\frac{2\varepsilon_s}{qN_D}(V_j - V)}. \tag{2}$$

For $V \geq V_j/2$, $C_j(V)$ is defined by a linear extrapolation of (1) from $V = V_j/2$, to avoid the singularity of (1) at $V = V_j$. V is the bias voltage, V_j is the built-in potential, ε_s is the semiconductor electric permittivity, A is the junction area, $t(V)$ is the thickness of the depletion layer, q is the charge of the electron, and N_D is the doping of the semiconductor epilayer. For the GaAs Schottky diodes fabricated at JPL, V_j is approximately 0.85 V at room temperature.

As the anodes get smaller and smaller, a correction term should be added to $C_j(V)$ to take into account the edge effects. This term has two components: a first-order term that is not modulated and a second-order term that is modulated [44]. The correction terms given in [44] apply to circular anodes and are a function of the anode radius. As

TABLE I
PHYSICAL AND ELECTRICAL DIODE PARAMETERS OF THE JPL 600-GHz BALANCED TRIPLER. THE VALUES OF THE SERIES RESISTANCE R_s AND THE REVERSE SATURATION CURRENT $I_{\rm sat}$ USED IN THE SIMULATIONS WERE OBTAINED AFTER A FIT OF THE EXPERIMENTAL DATA

Physical parameters	*Electrical parameters*	
Epilayer doping = $1{\cdot}10^{17}$ cm^{-3} Epilayer thickness = 500 nm	V_j $C_j(0)$	0.85 V ≈ 6 fF
	R_s measured at DC R_s from equation (3) R_s in simulations, *T=295K* R_s in simulations, *T=120K*	8 Ω ≈ 20 Ω 17 Ω 14 Ω
N^+ layer thickness ≈ 1.2 μm N^+ layer doping = $7{\cdot}10^{18}$ cm^{-3}	I_{sat} measured, *T=295 K* I_{sat} in simulations, *T=295K* I_{sat} in simulations, *T=120K*	$8{\cdot}10^{-15}$ A $1{\cdot}10^{-13}$ A $1{\cdot}10^{-20}$ A
Anode width ≈ 2 μm Anode length ≈ 3 μm	η measured, *T=295K* η in simulations, *T=295K* η in simulations, *T=120K*	1.22 1.20 1.10
Substrate thickness = 12 μm	V_{br} calculated	-16 V

the multipliers fabricated at JPL use rectangular anodes, we modified the correction term to be a function of their length and width. We only kept the first-order correction term that corresponds to a linear capacitance in parallel to the nonlinear plate capacitance of the junction; the other term is negligible for anodes of approximately 2 μm $\times 3$ μm each and a doping of 1.10^{17} cm^{-3}. We found that the first-order correction term represents about 15% of the plate capacitance of the junction at $V = 0$.

2) The nonlinear conductance is derived from the classic equations of thermionic emission in Schottky contacts [49].

Breakdown effects are not directly included in the simulations. However, time-domain simulations are performed to check that the voltage across the diodes never enters breakdown to minimize the risk of damaging the diodes [50]. For the same reasons, the dc current through the diodes is kept below about 2 mA [50]. As no velocity saturation effects [42]–[44] are taken into account, the peak current is not limited during the simulations.

The value of the reverse saturation current $I_{\rm sat}$ influences significantly the predicted performance, especially when the input power is high enough to create a direct current through the diodes. Its value depends strongly on the actual temperature of the junction, which is difficult both to measure and to predict. Therefore, some uncertainty is introduced by this parameter into the model. As shown in Table I, at an ambient temperature of 295 K, the measured value of the saturation current at dc is lower than the value used in the simulations to fit the RF measurements. This may be caused by heating of the diode by dissipated RF power.

3) The series resistance R_s of the planar diode affects the efficiency of the multiplier. Significantly underestimating the value of R_s affects the optimization of the design itself: the optimized junction capacitances would be too big and the bias voltage too far in the reverse regime. With respect to the predictions, the actual multiplier performance would be degraded and shifted down in frequency. To partially compensate for the frequency shift, one would have to use devices with smaller anodes.

DC measurements of R_s give an indication of the quality of the diodes, but the measured values are usually too low to be used in the RF simulations. On the other hand, calculations of the series resistance have to take into account the particular topology of the planar diode, where skin effects play a major role. In addition, any physical model of the Schottky barrier has to be properly implemented in a circuit simulator, unless only linear impedances of the diodes are used. Our approach relies on the empirical rule introduced in [51] that consists in fixing the product $R_s \times C_j(0)$. This value is derived empirically. For submillimeter-wave multipliers working at room temperature and for a doping of 1.10^{17} cm^{-3}, R_s is set to

$$R_s \times C_j(0) = 120\ \Omega \cdot \text{fF}. \tag{3}$$

For our tripler, this rule gives $R_s \approx 20\ \Omega$ per diode compared to the dc measured value of $R_s = 8\ \Omega$ per diode. As shown in the next section, this value appears to be slightly too high to simulate the actual behavior of our 600-GHz tripler at room temperature: we find that the value of the series resistance should be $R_s = 17\ \Omega$. At an ambient temperature of 120 K, the series resistance was set to $R_s = 14\ \Omega$ in the simulations to fit the experimental data. Note that, in both cases, R_s used in the simulations is higher than the measured dc value.

Three-Dimensional Modeling of the Diodes: The electromagnetic field around the diode is calculated with Ansoft HFSS[1] and is measured with a virtual probe placed at the location of the Schottky contact. This probe is defined as an internal wave-port in HFSS. The anode itself defines the inner conductor; the outer conductor is defined by the edges of a small rectangle that lies on the top face of the mesa around the anode (thus, the probe has no length). The gap between the edges of the anode and this rectangle has to be very narrow to avoid underestimating the parasitic capacitance. The definition of the port and the meshing around the diode are critical to get accurate results. The 3-D geometrical structure of the diode must also be drawn accurately. Details such as the passivation layers greatly contribute to the parasitic capacitances and must be included in any accurate 3-D representation of the diode.

Input Power Issue: Multiplier designs are always optimized for a given input power. In this particular case, the design was optimized for 50-mW input, based on data of several available 200-GHz drivers [25], [35]. The choice of a low doping level should make our four-diode tripler able to safely handle up to about 70 mW of input power. However, for the measurements presented in this paper, the input power was about 22–27 mW when operating the multiplier at room temperature and about 30–40 mW when operating the multiplier at a temperature of 120 K.

Modeling of the Diode Cell: For triplers, the second-harmonic idler plays an essential role in the transfer of energy from the fundamental to the third harmonic [52]. Therefore, the diodes need to be properly matched at the idler frequency. Indeed, their embedding impedances should be as close as pos-

[1]High Frequency Structure Simulator, Ansoft Corporation, Pittsburgh, PA.

sible to pure reactances. To greatly facilitate the synthesis of such impedances, the circuit has to be balanced. This requires that the diode cell satisfy the conditions mentioned in Section II. In addition, the capacitance of each diode needs to be compensated by adjusting the length and the width of the fingers, the size of the mesas, and the dimensions of the cross section of the chip channel (see Fig. 4). Diodes with small junction capacitance require longer fingers (implying wider channels) or higher channels than diodes with large junction capacitances.

An initial diode cell is drawn based on the chip topology. Its S-parameters are first calculated with Ansoft HFSS and then used in harmonic-balance simulations to determine which junction capacitance and bias voltage give the maximum output power. It is important to take into account the ohmic and dielectric losses of the circuit in all the simulations. The balance between the diodes is monitored for all the relevant frequencies. We used Agilent ADS[2] suite for these calculations.

The diode cell alone cannot be an efficient tripler; thus, harmonic-dependant complex impedances are connected to the ports of the ADS simulation bench that correspond to the HFSS wave-ports P1 and P2 (see Fig. 4). These ports excite only the TEM mode of the suspended microstrip line. The complex impedances are optimized for the center of the band. The output power is calculated at either port P1 or port P2. To have some idea of the instantaneous bandwidth, the frequency is swept across the band. Then, the 3-D stucture is modified according to these results and the rules mentioned earlier in this paragraph. Many iterations are often required to converge to a satisfactory solution.

Input and Output Matching Circuits: Once the diode cell and the size of the anodes are fixed, the different sections of the suspended-microstrip line and the input and output E-probes are optimized to maximize the conversion efficiency and the input coupling. The design is driven by the necessity to minimize the number of on-chip matching elements in order to reduce both the chip dimensions and the losses. At this stage of the design, most of the multiplier is already in place and a fine-tuning of the diode cell and anode size is performed. Upon completion of this step, the chip topology is fixed.

To extend the bandwidth, we add to the input waveguide a succession of sections of high and low impedance (see Fig. 2). As they have no impact on the output match, it is possible to use only linear simulations. To broaden the output match, the same method is applied to the output waveguide.

IV. Simulations and Measurements

The balance between the diodes at the input frequency was investigated in detail to avoid the risk of overdriving a diode. Fig. 5 shows simulations of the input coupling balance for a flat input power of 35 mW. All of the simulations include waveguide losses. The diodes situated symmetrically to the suspended microstrip line (diodes 1 and 4 and diodes 2 and 3) receive the same amount of power. The imbalance between these two pairs is about 10%. The average input coupling is about 75%–80% from 540 to 600 GHz, but it degrades above 600 GHz to 50% at 640 GHz. Unfortunately, at the current stage of the technology, no direct measurements can be done to verify these values. The simulated output power of the 600-GHz tripler at

[2]Advanced Design System, Agilent Technology, Palo Alto, CA.

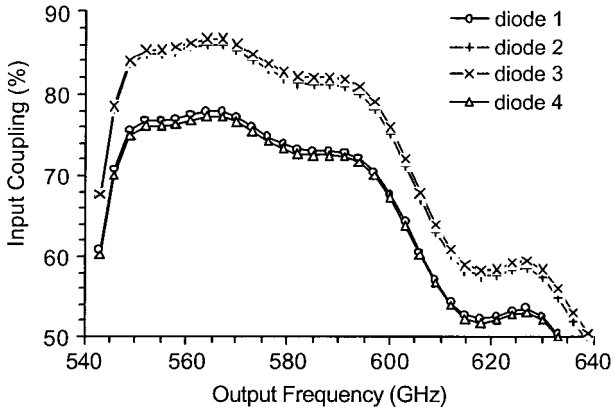

Fig. 5. Simulated input coupling per diode of the 600-GHz balanced triplers at 120 K with a flat input power of 35 mW and the bias voltage fixed to $V_{\rm bias} = -9$ V. An input coupling of 100% corresponds to 25% of the total input power coupled to that diode. Due to the losses of the circuit, the maximum coupling is approximately 85%.

the ambient temperatures of 295 K and 120 K are plotted in Figs. 6 and 7 along with measured data. The simulations were performed using measured values of the input power at 200 GHz, and the diode parameters are taken from Table I.

For the experiments, a commercial synthesizer with sextupler head was used to drive a MMIC-based W-band power amplifier [53], [54]. Although this amplifier can provide more than 200 mW from 89 to 106 GHz, the W-band power was kept constant at 100 mW for measurements at room temperature or 150 mW for measurements at 120 K, due to the reliability concerns explained earlier. The output power from the first-stage 200-GHz doubler was measured with an Erickson calorimeter [55] that provides a broad-band match. For room-temperature measurements, a calibrated WR10–WR5 waveguide transition was used; for cryogenic measurements at 120 K, the Erickson power meter was insulated with a WR10 stainless steel waveguide and a vacuum window, whose losses were also calibrated.

The power produced by the 600-GHz tripler was measured at room temperature with the same power meter by attaching an external WR1.7–WR10 waveguide transition directly to the tripler output flange. A separate calibration of the transmission of this transition gave a loss of 0.6 dB. At 120 K, the measurements were performed with a Thomas Keating[3] power meter by attaching a Picket–Potter horn [56] directly to the tripler output flange. A more detailed description of the test setup can be found in [25]. A loss of 0.4 dB was measured for the horn and an additional loss of 0.2 dB was estimated for the spill-over and the mirror. A separate calibration of the transmission of the cryostat window gave a loss of 0.3 dB at 600 GHz.

No detailed investigation of the tripler's noise properties or output spectrum was carried out. However, similar multipliers have been used to successfully pump sensitive mixers without any degradation in performance as long as the power amplifiers are saturated [57], [58]. The second harmonic is expected to be attenuated by more than 50 dB due to the length of the output waveguide (in cutoff mode.) Simulations show the fourth harmonic to be down by more than -20 dB with respect to the third harmonic.

[3]Thomas Keating Ltd, Station Mills, Billingshurst, U.K. [Online]. Available: http://www.terahertz.co.uk

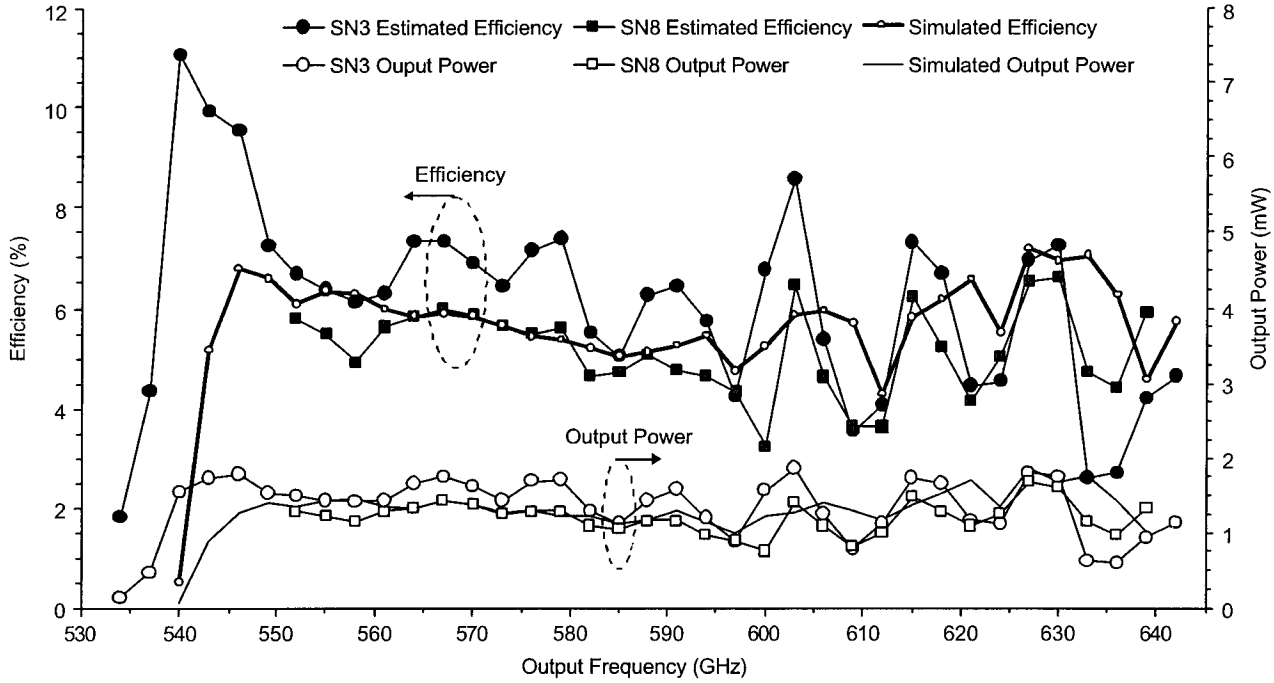

Fig. 6. Measured estimated efficiency (top curves with filled markers) and measured output power (bottom curves with open markers) of two 600-GHz balanced triplers (SN3 & SN8) at an ambient temperature of 295 K. The top plain curve with small open circles and the bottom plain curve correspond, respectively, to the simulated efficiency and the simulated output power. From 552 to 645 GHz, the input power is in the range 22–25 mW.

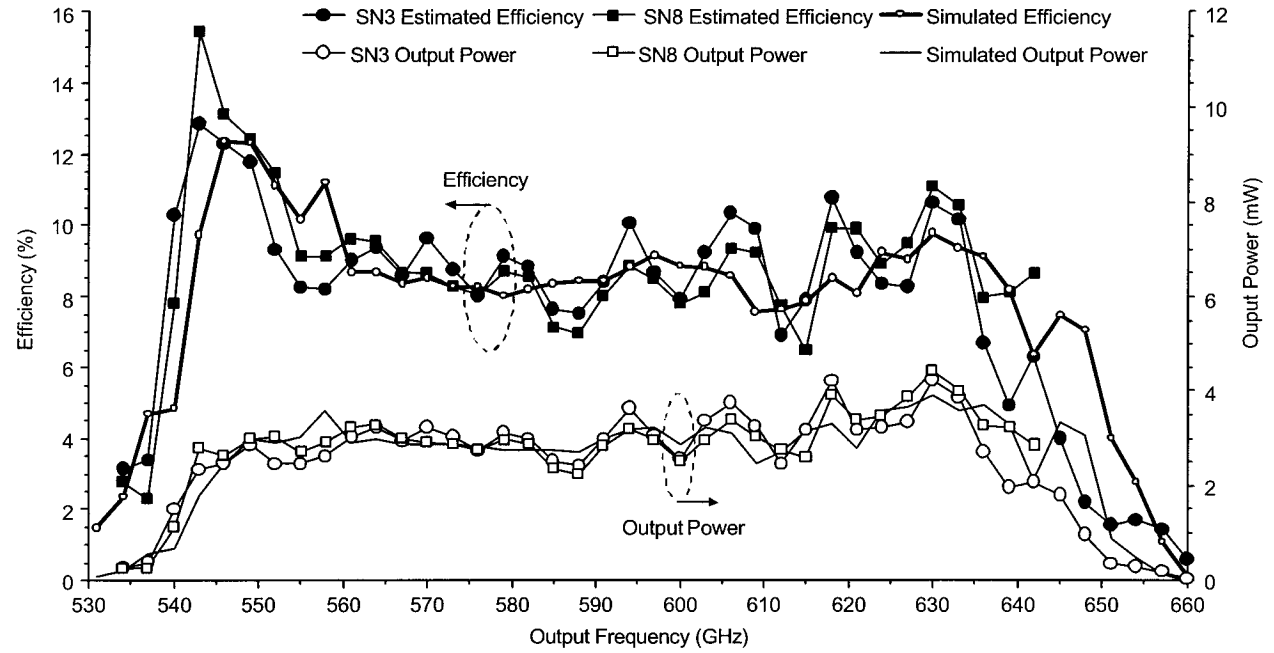

Fig. 7. Measured estimated efficiency (top curves with filled markers) and measured output power (bottom curves with open markers) of two 600-GHz balanced triplers (SN3 & SN8) at an ambient temperature of 120 K. The top plain curve with small open circles and the bottom plain curve correspond, respectively, to the simulated efficiency and the simulated output power. From 555 to 645 GHz, the input power is in the range 30–44 mW.

The measured results of two multipliers are shown at room temperature in Fig. 6 and at 120 K in Fig. 7. The bias was optimized for each frequency point, ranging from -12 to -1 V total across four diodes in series at dc (the bias voltage of the 200 GHz was also optimized for each frequency point.) The measured dc currents were in the range 0.1–0.47 mA at room temperature, and 0.25–1.5 mA at 120 K. Since there was no isolator between the doubler and tripler, the efficiency was estimated by dividing the chain output power by the separately measured output power of the 200-GHz driver chain.

At room temperature, the input power was 5–21 mW from 525 to 549 GHz and 22–25 mW from 552 to 645 GHz. The measured output power was 0.9–1.8 mW in the band 540–640 GHz. The output power exhibits an increased level of standing waves in the upper part of the band that possibly corresponds to interactions between the multipliers. Actually, in this part of

the band, the expected input matching of the 600-GHz tripler is only in the order of −6 dB. At 120 K, the input power was 5–29 mW from 531 to 552 GHz and 30–44 mW from 555 to 648 GHz. The measured performance shows record output power for a solid state source of 2.0–4.2 mW in the band 540–640 GHz. The standing wave decreased due to improved input coupling in the upper part of the band.

With respect to the simulations, the actual band is shifted by about 1% down in frequency. Note also that the two different triplers have very similar performance.

V. Conclusion

In recent years, tremendous progress in the modeling and fabrication of frequency multipliers at submillimeter wavelengths has been made, thanks to the introduction of MMIC-like circuits and the use of precision simulation tools like Ansoft HFSS and Agilent ADS. These advances enabled the design and fabrication of a 540–640-GHz fix-tuned balanced tripler that exhibits, to the best of the authors' knowledge, state-of-the-art performance in terms of efficiency, bandwidth, flatness, and power-handling capability.

This multiplier with its driver forms a broad-band 600-GHz sextupler chain. At room temperature, with 100 mW of pump power at 100 GHz, its electronically tunable bandwidth reaches 17% and its peak flange-to-flange conversion efficiency is 1.8%. At 120 K with an input power of 150 mW, this chain exhibits the same bandwidth and has a peak flange-to-flange conversion efficiency of 2.7%.

The performance of this tripler makes it suitable to use as a driver for even higher frequency multipliers. It has been successfully used to pump the 1.7–1.9-THz balanced tripler presented in [26]. Updated results will be reported later and will show a major improvement in the output power from this solid-state LO chain as compared with [26].

It is believed that the topology of this frequency tripler is suitable for lower frequency circuits, since it offers the possibility to add more diodes on the chip and therefore increase input power-handling capability. This circuit topology can in principle be scaled to higher operating frequencies and will ultimately be limited by the minimum feature size possible for the lithographic technology that is used.

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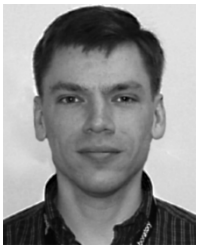

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