A 56–65 GHz Injection-Locked Frequency Tripler With Quadrature Outputs in 90-nm CMOS

Wei L. Chan, *Student Member, IEEE*, and John R. Long, *Member, IEEE*

***Abstract*—A sub-harmonic injection-locked tripler multiplies a 20-GHz differential input to 60-GHz quadrature (I/Q) output signals. The tripler consists of a two-stage ring oscillator driven by a single-stage polyphase input filter and 50-Ω I and Q-signal output buffers. Each gain stage incorporates a hard limiter to triple the input frequency for injection locking and a negative resistance cell with two positive feedback loops to increase gain. Regenerative peaking is also used to optimize the gain/bandwidth performance of the 50-Ω output buffers. Fabricated in 90-nm CMOS, the tripler has a free-running frequency of 60.6 GHz. From a 0-dBm RF source, the measured output lock range is 56.5–64.5 GHz, and the measured phase noise penalty is 9.2 $\pm$ 1 dB with respect to a 20.2-GHz input. The 0.3×0.3 mm^2 tripler (including passives) consumes 9.6 mW, while the output buffers consume 14.2 mW, all from a 1-V supply.**

***Index Terms*—Frequency tripler, injection-locked, millimeter-wave, quadrature voltage-controlled oscillator, regenerative peaking, wide locking range.**

I. Introduction

EXCITING new opportunities are envisioned for silicon integrated circuits that are capable of mm-wave operation. Potential consumer applications include: gigabit per second short-range wireless communication in the 60-GHz (defined in the IEEE 802.15.3c standard) and 120-GHz bands, long-range collision avoidance radar for automobiles at 77 and 79 GHz, and sub-terahertz imaging (94 GHz and above) [1]–[3]. Production silicon VLSI technologies have demonstrated a peak transit frequency, f_T, above 200 GHz for bipolar (NPN) devices [4], [5] and higher than 300 GHz for CMOS (NFET) transistors [6], [7], which has focused commercial interest towards millimeter-wave (mm-wave) frequency applications for silicon integrated circuits. Implementation of mm-wave transceivers in baseline CMOS technology is attractive because of its high potential for both low cost in volume production and RF/baseband co-integration.

Single-sideband modulation or demodulation in a mm-wave transceiver requires a mm-wave local oscillator (LO) with quadrature (i.e., I and Q) outputs. A phase and amplitude tuning mechanism with about 5° and 0.5 dB [8] of correction range is required in order to tune out the unwanted sideband, as sideband rejection is often degraded by phase and amplitude errors arising from process, voltage and temperature (PVT) variations. An output swing of around 300 mV-pk from the LO source is needed to drive a mm-wave active mixer, and the LO output must have adequate spectral purity for the intended application. Low power consumption (i.e., not more than 50 mW) is also desired for portable applications, especially if antenna arrays are used to implement beam steering and beamforming at mm-wave frequencies because of increased circuit complexity. Frequency multipliers are commonly used to up-convert lower frequency sources to mm-wave frequencies in low-volume applications (e.g., laboratory test equipment). The low-power CMOS frequency tripler described in this work is a practical alternative to direct synthesis of the LO using phase-locked techniques.

In this paper, a differential CMOS frequency tripler with I/Q outputs is proposed. The circuit is designed around a two-stage, injection-locked ring oscillator with tuned LC loads. Sub-harmonic injection-locking occurs when the third harmonic of the input is injected into the LC tank of the oscillator, thereby creating an output at three times the input frequency. The quality factor, Q, of the LC tank loading each ring oscillator stage is decreased by resistive loading to widen the lock range. Each gain stage in the ring oscillator uses two positive feedback loops to provide loop gain sufficient to sustain oscillation. Regenerative peaking is also used to optimize the response of the 50-Ω output buffer and reduces its power consumption. Implemented in 90-nm CMOS technology, the tripler achieves a lock range from 56-65 GHz with a phase noise penalty of less than 10 dB (compared to the injecting source), while consuming a total of 24 mW from a 1-V supply [9].

Section II of this paper explores the options for mm-wave frequency synthesis, and discusses their merits. Section III describes the design of the I/Q-output frequency tripler, including circuit schematics of the oscillator gain stage and the output buffer. Key experimental results are highlighted in Section IV.

II. Frequency Synthesis

Fig. 1 illustrates three possible LO generation schemes for a radio receiver. The phase-locked loop (PLL) in Fig. 1(a) locks the VCO to a high quality frequency reference, thereby obtaining frequency stability at the desired LO frequency. In a 60-GHz transceiver with zero or low intermediate frequency baseband processing, the LO operates very close to the received radio-frequency (RF input), placing the LO in the 60-GHz band [10], [11]. At such high frequencies, the phase noise performance of a mm-wave VCO may be adversely affected by tank quality factor, layout parasitics and power consumption constraints. For example, [12] reports a 30-GHz VCO with

Manuscript received April 20, 2008; revised June 27, 2008. Current version published December 10, 2008. This work was supported by the Dutch BSIK—Freeband Communication project *WiComm*.

The authors are with the Electronics Research Laboratory/DIMES, Delft University of Technology, 2628 CD Delft, The Netherlands (e-mail: w.l.chan@tudelft.nl; j.r.long@tudelft.nl).

Digital Object Identifier 10.1109/JSSC.2008.2004869

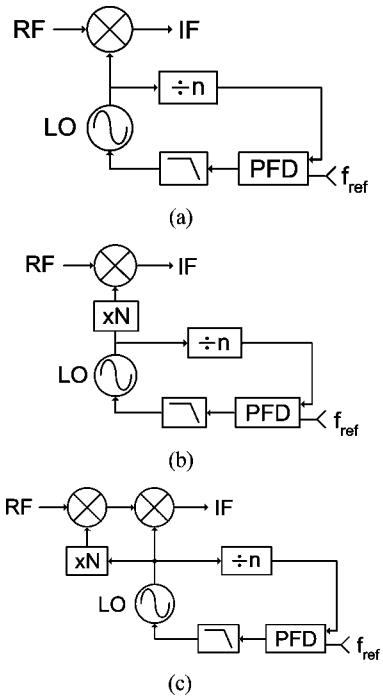


Fig. 1. Frequency synthesis with: (a) PLL, (b) frequency multipler in single conversion, and (c) multiplier in a dual conversion front-end architecture.

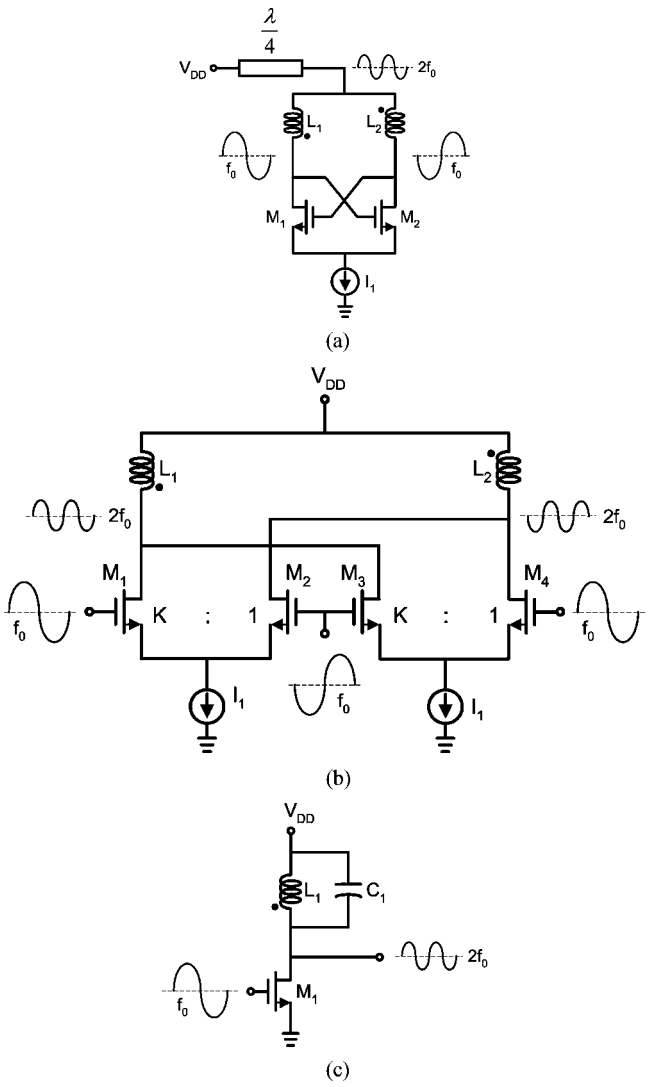


Fig. 2. Frequency doubling: (a) push-push oscillator, (b) unbalanced source-coupled pairs, and (c) tuned amplifier.

−87 dBc/Hz phase noise at 1-MHz offset, whereas the phase noise of a 10-GHz VCO [13] is −102 dBc/Hz at 1-MHz offset, which is 5.5 dB more than the theoretical 9.5 dB penalty due to increasing the frequency by a factor of 3 (i.e., from 10 to 30 GHz). Moreover, the local oscillator usually needs to drive high-speed dividers in the PLL as shown in Fig. 1(a). Frequency divider stages become more difficult to implement and are power hungry at mm-wave frequencies, which increases the total power consumption of the receiver. For example, a 2:1 static frequency divider with buffers in 0.12-μm CMOS operating at 25.4 GHz, reportedly consumes 61.5 mW [14].

Alternatively, a frequency multiplier can be used following the PLL-stage to provide the desired LO frequency. Fig. 1(b) and (c) illustrate single and dual downconverters using a multiplier, which is especially attractive for use in the mm-wave regime. In the homodyne or low-IF topologies (see Fig. 1(b)), the LO drives the multiplier (where N is an integer) to generate an output signal N times larger that is used for RF down-conversion. The LO frequency may be reduced if more than one stage of down-conversion is used, as in a heterodyne architecture (e.g., to 30 GHz [12]). Note, that the LO frequency is an even smaller fraction of the RF (i.e., $1/(N+1)$) in the heterodyne architecture of Fig. 1(c). In both cases where a multiplier is used, the LO operates at a lower frequency than the incoming (RF) frequency. Hence, the multiplier eases the design requirements on the PLL, as it may be operated at a lower frequency where stringent phase noise requirements are easier to satisfy with reduced power consumption.

Low-order multipliers (e.g., frequency doubler or tripler) are more amenable to monolithic integration than higher multiplication factors. The IC multiplier relies upon harmonic frequency generation, where the harmonic energy necessarily decreases with increasing frequency. More amplifying stages are required to provide a given signal swing as the multiplication factor is increased, which drives up power consumption. A separate frequency-doubling circuit may not be required if a differential VCO implementation is employed, given that a strong second-harmonic tone appears at the virtual ground nodes in differential oscillator topologies (e.g., the power-supply node as shown in Fig. 2(a)) [15]. This may arise due to asymmetry in the differential outputs or can be generated by the nonlinearity of the transistors. The doubled output signal requires amplification before driving an on-chip mixer, which increases the overall power consumption in the receiver. Also, the driving source is now single-ended, and thus immunity to common-mode noise is compromised.

An IC doubler constructed with unbalanced source-coupled pairs is shown in Fig. 2(b) [16]. Due to the different transistor sizes required (K:1 ratio of sizes in each pair), the AC output is unbalanced (e.g., the parasitics differ between the two output nodes), and this affects the symmetry of the output waveforms. A frequency multiplied signal can also be obtained by driving an

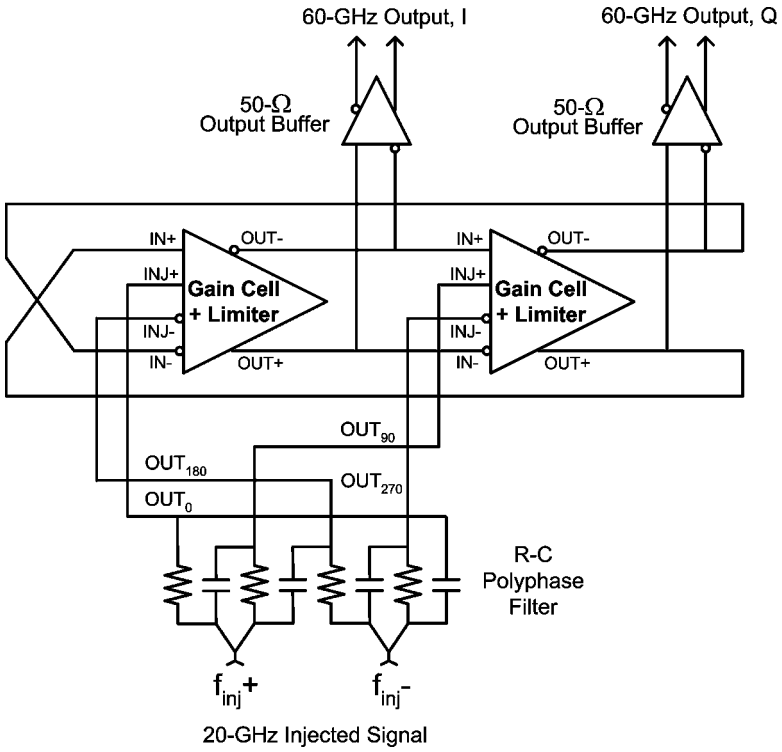


Fig. 3. Block diagram of the proposed tripler.

inductively-loaded common-source amplifier biased Class-B, as illustrated in Fig. 2(c). The amplifier load is tuned to the desired harmonic frequency, and the weak output signal requires several amplification stages.

From the above discussion, conventional frequency multipliers can consume substantial power, and can only provide single-ended or poorly balanced outputs. To reduce power consumption, a ring oscillator, which can be sub-harmonically injection-locked [17], [18] to an input at 1/3 the oscillator's free running frequency is preferred. Moreover, a two-stage ring oscillator readily produces quadrature signals, which are required for advanced modulation and demodulation schemes.

III. Frequency Tripler Architecture and Design

Fig. 3 shows the block diagram of the proposed frequency tripler. Two identical self-oscillating differential cores are connected in series to form a ring oscillator that free-runs at 60 GHz. The phase shift across each stage is 90°, and the anti-phase feedback connection adds another 180° for a total loop phase shift of 360°. Each core circuit consists of a gain cell operating in parallel with a differential hard limiter. The gain cell incorporates a negative resistance cell to compensate for resistive losses, which helps to sustain oscillation in the overall loop. The hard limiter is a tuned differential amplifier that generates a strong third-harmonic component from its input signal. The third-harmonic, being close to the free-running frequency of the ring oscillator, injection-locks the two-stage ring oscillator resulting in a tripled output. The tripler generates quadrature, differential outputs when it is injection locked, and these outputs are buffered by 50-Ω drivers to external loads in order to minimize loading on the oscillator.

A single-stage R-C polyphase filter (PPF) centered at 20 GHz (also shown in Fig. 3) produces the quadrature differential signals that drive the limiters from a single, differential input. The typical process mismatches for both the resistors and capacitors of the PPF designed for 20 GHz become less critical as they have relatively large physical dimensions on-chip. Thus, higher phase and amplitude accuracies between the quadrature signals can be expected compared to direct synthesis of quadrature signal from a PPF at 60 GHz. Quadrature signals are fed into the limiters in order to minimize the quadrature signal error at the tripler outputs.

A. Injection-Locked Oscillators

The trade-offs inherent to the design of the two-stage ring oscillator used in the tripler are better understood by first reviewing the parameters which define the lock range of an injection locked-oscillator. The lock range ($\Delta\omega$) of a fundamental injection-locked LC oscillator can be written as [19]

$$\Delta\omega = \frac{\omega_0}{Q}\cdot\frac{I_{\rm INJ}}{I_{\rm OSC}}\cdot\frac{1}{\sqrt{1-\left(\frac{I_{\rm INJ}}{I_{\rm OSC}}\right)^2}} \tag{1}$$

where ω_0 is the oscillation frequency, $Q(=\omega_0 L/R)$ is the quality factor of the LC tank, and $I_{\rm INJ}$ and $I_{\rm OSC}$ refer to the magnitude of the injection and oscillator signal currents, respectively.

Equation (1) predicts that the Q of the tank must be decreased in order to increase the lock range. Similarly, $I_{\rm INJ}$ can be increased by driving the injection amplifier ($\rm M_3$ and $\rm M_4$ as in Fig. 4) with larger signal amplitude ($\rm INJ+$, $\rm INJ-$), or by increasing the gain of the injection amplifier, which also implies

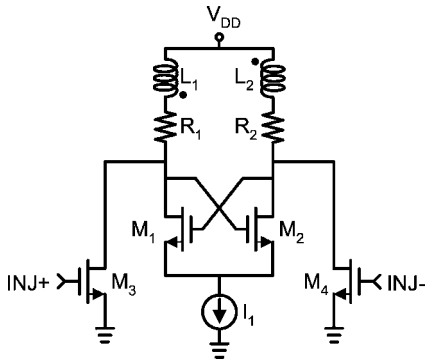


Fig. 4. Simplified schematic of an injection-locked oscillator.

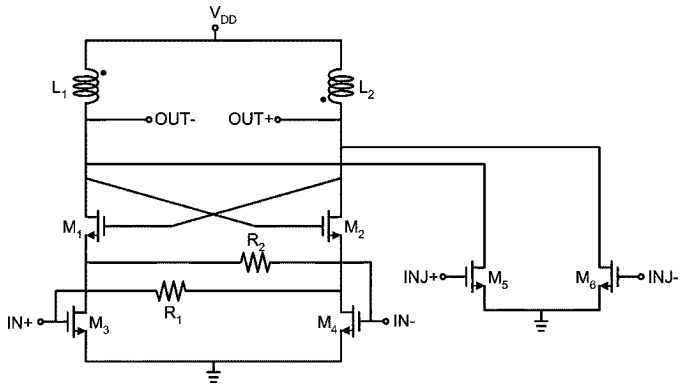


Fig. 5. Oscillator gain stage with hard limiter.

greater power consumption. Likewise, $\mathrm{I_{OSC}}$ can be reduced by decreasing the bias current of the oscillator ($\mathrm{I_1}$). This increases the lock range for a given $\mathrm{I_{INJ}}$ but the oscillator may not reliably start. Similarly, a lower tank-Q implies lower gain, which compromises start-up of the oscillator. To account for modeling inaccuracies and circuit variations caused by PVT variations, it is assumed that the loop gain must be greater than two. Thus, lowering the Q to widen the lock range necessitates a higher oscillator bias current, which decreases the lock range. Thus, the lock range remains unchanged. Moreover, the transconductance of the transistors is lower in CMOS compared to bipolar technology for a given DC bias current, and therefore more current is required to provide the same gain for a given load. Thus, the Q of the tank must be maximized to reduce power consumption of a CMOS design, and hence, the injection locking range will be relatively narrow. For a Q-factor of 10, assuming $(I_{\mathrm{INJ}}/I_{\mathrm{OSC}})$ equal to 0.5, the lock range is 5.8% of the oscillation frequency.

With this qualitative understanding, the design of this tripler aims to achieve a wide locking range with enough margin to ensure oscillation and power consumption in the low mW range.

B. Oscillator Gain Core

The circuit implementation of the gain core is presented in Fig. 5. It uses only NMOS transistors, polysilicon resistors and inductors. In the gain stage, a cross-coupled differential pair consisting of $\mathrm{M_1}$ and $\mathrm{M_2}$, provides the negative resistance to compensate the losses of the LC-tank, where the tank resonant frequency is determined by $\mathrm{L_1}$ and $\mathrm{L_2}$, and the parasitic capacitances at the output (i.e., drain) nodes. The tank inductance is 200 pH, which is chosen as large as possible in order to maximize the lock range. A varactor (not present in the prototype) could be connected across the tank for fine frequency tuning, if desired.

Another input differential pair ($\mathrm{M_3}$ and $\mathrm{M_4}$) with cross-connected feedback resistors ($\mathrm{R_1}$ and $\mathrm{R_2}$) re-use the bias current flowing through $\mathrm{M_1}$ and $\mathrm{M_2}$. With positive feedback incorporated around $\mathrm{M_1}$, $\mathrm{M_2}$ and $\mathrm{M_3}$, $\mathrm{M_4}$ (via $\mathrm{R_1}$, $\mathrm{R_2}$), the overall loop gain increases without any penalty in current consumption or the need to increase the supply headroom. High quadrature accuracy can also be expected from the proposed design, as the RF output current from the LC tank does not need to be shared between the coupling and switching transistors as in a typical quadrature oscillator [20] where both of their drain terminals are coupled to the LC tank. Also, $\mathrm{R_1}$ and $\mathrm{R_2}$ load the outputs of the previous gain stage, which reduces the Q-factor of the two-stage ring oscillator, thereby increasing the injection-locking range. With $\mathrm{R_1}$ and $\mathrm{R_2}$ equal to 500 Ω, multiple oscillation modes are dampened, and at the same time, the resulting high-gain stage ensures reliable start-up with loop gain of about two for the 60-GHz quadrature oscillator.

$\mathrm{M_5}$ and $\mathrm{M_6}$ in Fig. 5 generate strong fundamental and third-harmonic outputs by hard-limiting the (20-GHz) quadrature signal fed to the $\mathrm{INJ+}$ and $\mathrm{INJ-}$ inputs from the PPF. All other higher harmonics can be safely ignored as they are considerably weaker (by more than 10 dB). The second harmonic is largely suppressed by the differential circuit topology. The fundamental component is strongly attenuated at the output by bandpass filtering of the LC tank, whereas the third harmonic signal is amplified and injection-locks the ring oscillator. The lock range, in turn, depends on the injected third harmonic signal strength, which is largely determined by the sizes of $\mathrm{M_5}$ and $\mathrm{M_6}$, and their gate bias voltage. Class-B biasing of $\mathrm{M_5}$ and $\mathrm{M_6}$ maximizes the third harmonic signal strength. The current consumption of the oscillator core is 4 mA in simulation.

C. Output Driver

The output driver schematic is depicted in Fig. 6. A differential pair ($\mathrm{M_1}$ and $\mathrm{M_2}$) is cascaded with a second differential amplifier ($\mathrm{M_3}$ and $\mathrm{M_4}$). Each pair is biased independently by current sources $\mathrm{I_1}$ (2 mA) and $\mathrm{I_2}$ (4 mA), respectively. A transformer, formed by $\mathrm{L_1}$, $\mathrm{L_2}$ and $\mathrm{L_3}$, $\mathrm{L_4}$, is driven anti-phase such that it provides positive feedback for the second differential pair ($\mathrm{M_3}$, $\mathrm{M_4}$). This increases the gain of the output buffer without any increase in bias current consumption. In this design, a magnetic coupling factor (k) of 0.3 is chosen between the primary and secondary coils of the transformer. At mm-wave frequencies, single turn coils are used to achieve low inductance. A planar transformer is best suited to realize low coupling coefficient as the distance between the coils can easily be changed. Fig. 7 compares the frequency response of the output buffer for cases with ($k = 0.3$), and without inductive coupling ($k = 0$). For $k = 0$, the circuit reduces to two inductively-loaded differential amplifiers in cascade. It is clear from the plot of Fig. 7 that there is a trade-off between the differential gain of the output driver and its bandwidth. For $k = 0.3$, an increase of 7 dB in differential gain is obtained at the expense of narrower bandwidth,

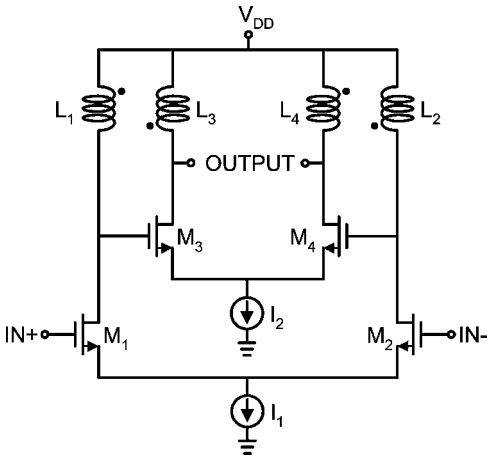


Fig. 6. Output buffer with transformer feedback.

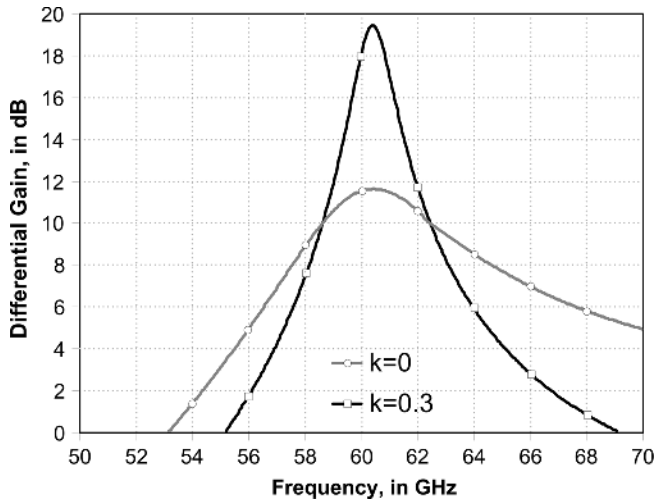


Fig. 7. Comparison of simulated output buffer gain with ($k = 0.3$) and without ($k = 0$) inductive coupling.

which is sufficient for this application. Also, a low k-factor is preferred to prevent parasitic oscillations in the buffer.

D. Simulated Response Under Injection-Locking

Fig. 8 tracks the output phase of the free-running ring oscillator with changes in the injected signal. The frequency is normalized to the difference between three times the injected frequency and the free-running frequency, divided by the lock range. At the two ends of the lock range, the relative phase change of the tripler output with respect to the phase at the free-running frequency, f_0, changes from -90° to $+90^\circ$, which confirms the theoretical prediction of $\pm 90^\circ$ phase variation under injection locking [21]. Also, as the phase change from -60° to $+60^\circ$ is relatively linear, it may be further exploited for phase shifting in a beamforming application.

The sensitivity of the tripler to the simulated phase and amplitude errors of the 20-GHz injected quadrature signals is also investigated. In Fig. 9(a), 1° in phase error between the quadrature inputs gives about 1.2 dB amplitude difference and a phase error of 15° at the output. However, 1 dB amplitude difference between the quadrature inputs (as in Fig. 9(b)) results in 12 dB output amplitude imbalance and 43° phase error. As the injected quadrature signals are provided by an on-chip PPF, Monte Carlo simulation of the PPF gives smaller than 0.2° quadrature error, and 0.1 dB amplitude imbalance, which gives 1.9° output phase and 0.7 dB amplitude errors for the tripler.

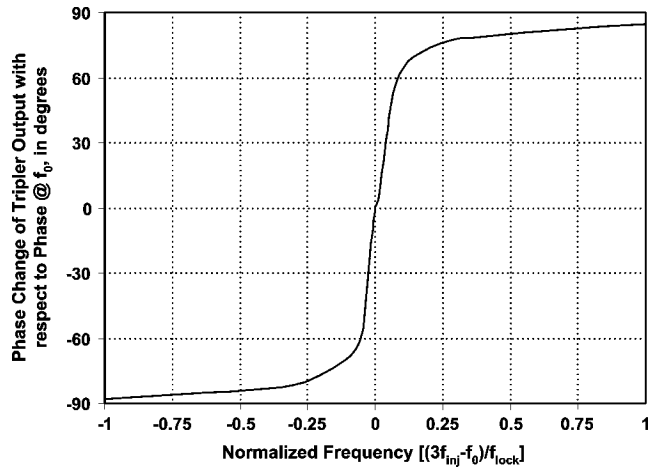


Fig. 8. Simulated relative phase change of the tripler output with injection-locking.

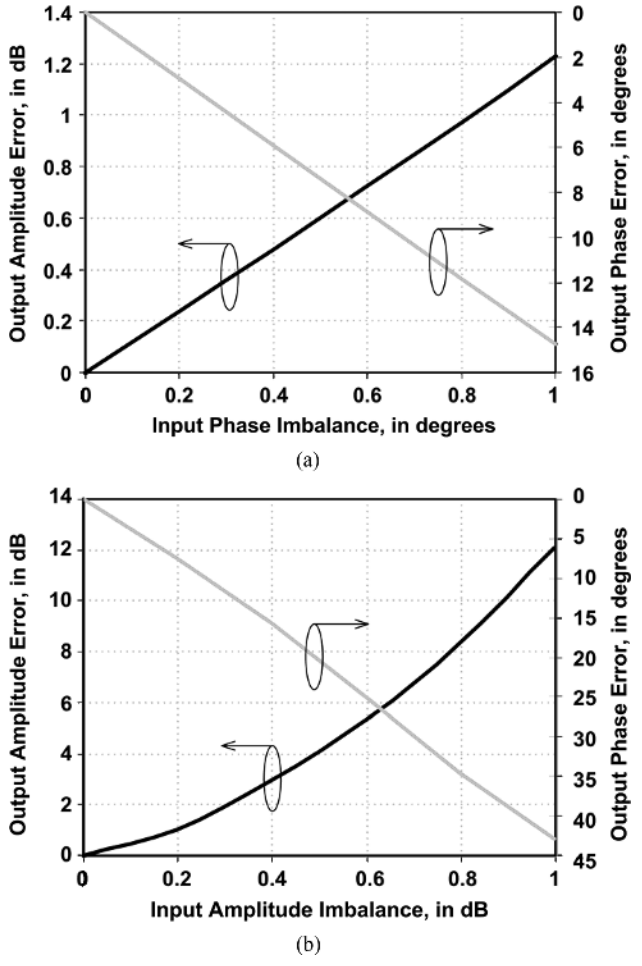


Fig. 9. Simulated output amplitude and phase error: (a) with input phase imbalance, and (b) with input amplitude error.

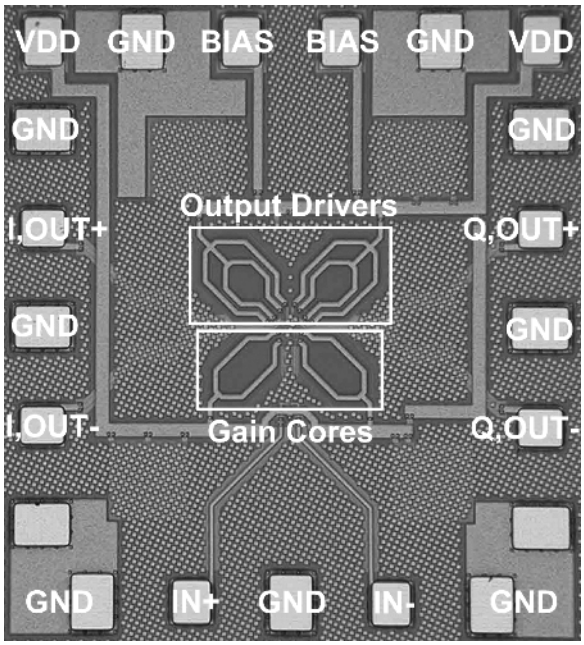


Fig. 10. Photomicrograph of the tripler test chip.

IV. Experimental Results

A chip microphotograph of the proposed injection-locked frequency tripler prototype with single-stage poly-phase input filter (input PPF) manufactured in a 90-nm bulk CMOS process [22] is shown in Fig. 10. All of the on-chip magnetic components are realized in the 1.3-μm-thick aluminum top-metal on a 1.5 Ω-cm substrate. The passive components are oriented orthogonal to each other so as to minimize parasitic inductive coupling between them. Also, the signal interconnects between the I/Q oscillator and its output buffers are kept as short as possible in a compact physical layout. The $950\times850\mu\text{m}^2$ test chip has an active area of $300\times300\mu\text{m}^2$, including the inductors and transformers. All of the following data were collected from measurements performed using on-wafer probing of the IC. At its default bias setting, the tripler consumes 23.8 mW from a 1-V supply; the two oscillator gain cores dissipate 9.6 mW and the two output buffers dissipate an additional 14.2 mW. Ten samples from the same batch were measured, and their free-running oscillation frequencies ranged from 59.7 to 60.6 GHz, which is close to the simulated value of 59.6 GHz. Fig. 11 shows the single-ended output spectrum measured for the free-running tripler driving 50-Ω loads at 60.6 GHz. The measured output power is -24.7 dBm. Spurious components are visible in the measured output spectrum a few hundred megahertz away from the main oscillation frequency. This is expected, as the free-running ring oscillator is susceptible to disturbances from a variety of internal and external sources (e.g., device-generated noise and power supply noise).

The spurious components are easily removed through injection locking. When the tripler is injection-locked by a 0-dBm input signal at 20.2 GHz from an external signal generator, the resulting injection-locked spectrum is shown in Fig. 12. The oscillator tracks the noise behavior of the signal source, and consequently the spurious components are negligible if a high-quality source is used (as seen in Fig. 12). This also means that under injection locking, the oscillator phase noise becomes secondary as

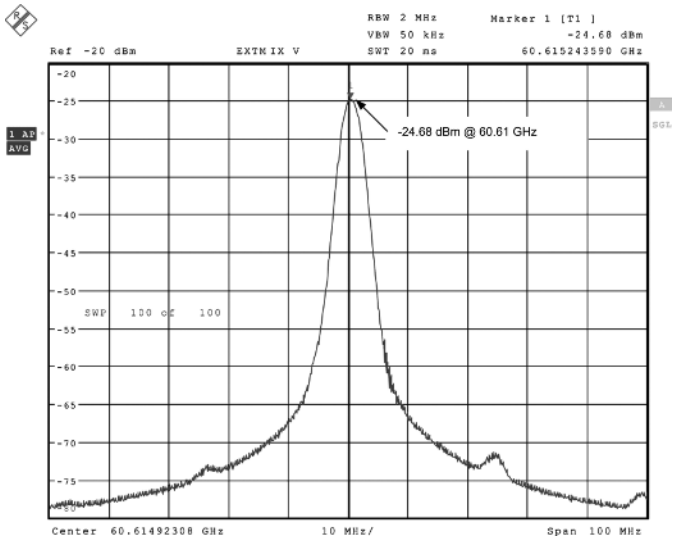


Fig. 11. Free-running output spectrum centered at 60.6 GHz.

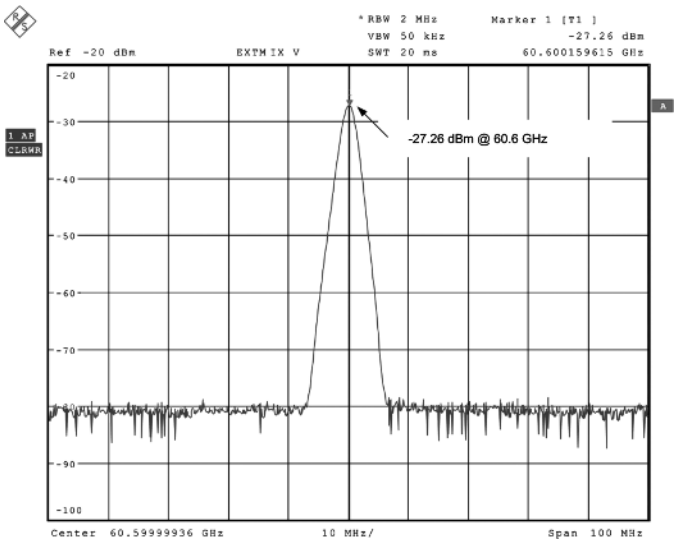


Fig. 12. Injection-locked spectrum at 60.6 GHz for 0-dBm injected signal at 20.2 GHz.

the spectral purity of the tripler is dominated by the characteristics of the input source. The measured phase noise performance of a single-ended output from the tripler under sub-harmonic injection locking (shown in Fig. 13) is plotted together with the phase noise of the signal source for comparison. At 100-kHz offset from the carrier frequency (i.e., 20.2-GHz external source, 60.6-GHz tripler output), a measured phase noise difference of approximately 9.2 ± 1 dB is evident. Accounting for any time-varying measurement fluctuations and/or errors in data acquisition from the spectrum analyzer screen, this value is close to the 9.54-dB limit predicted from theory (i.e., $20 * \log_{10} 3$) [21]. Also, similar results are observed from the 30-kHz to 1-MHz offset range (within the locking range of the tripler) until both source and tripler phase noise curves reach the thermal noise floor at about 2-MHz offset.

Fig. 14 shows the injection-locking range for varying injected signal power levels. The input power refers to a single-ended RF signal source (after accounting for losses) which is coupled to the on-chip PPF via an external passive balun to generate differential input signals to the tripler. It is evident that the lock

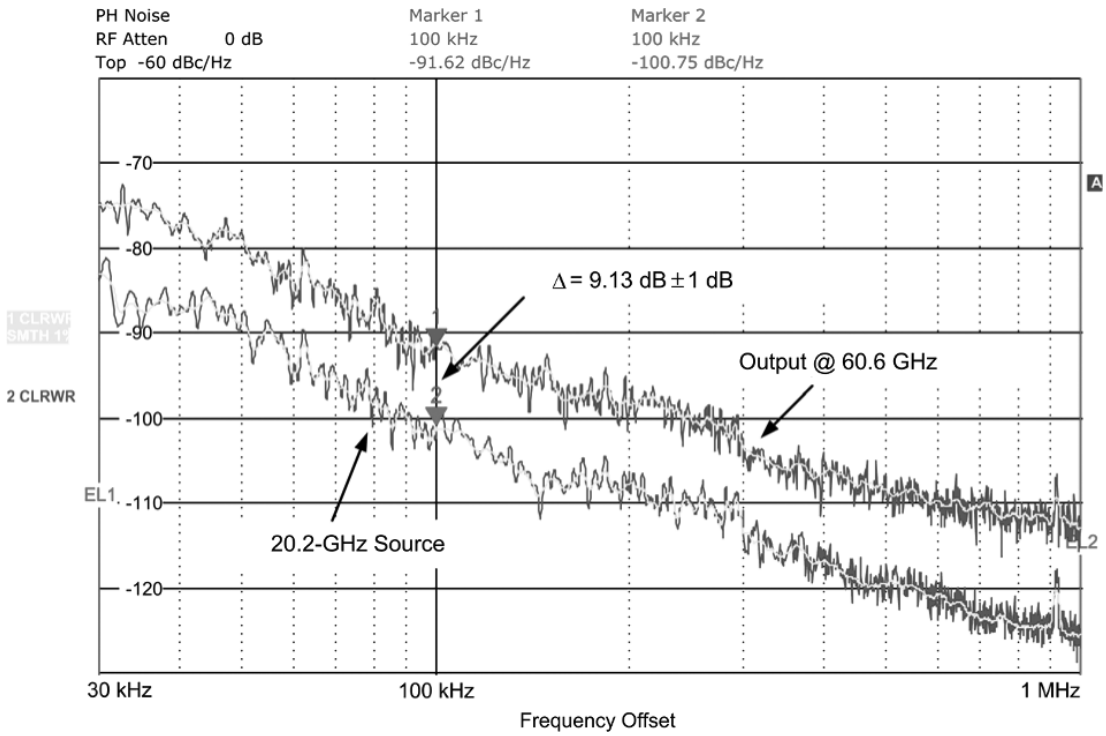


Fig. 13. Measured SSB phase noise of the 20.2-GHz RF input source (bottom) and tripler output at 60.6 GHz (top).

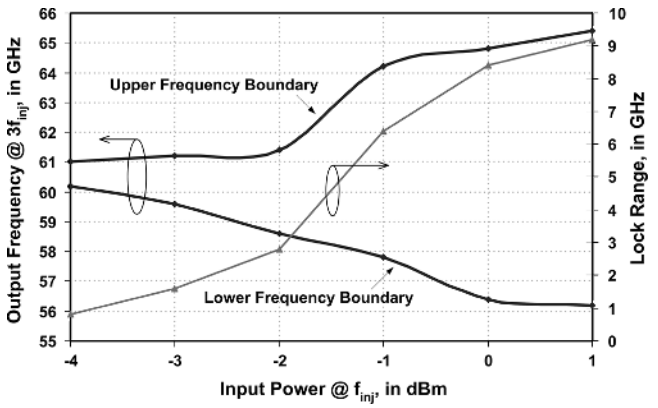


Fig. 14. Measured upper (f_u) and lower (f_l) frequencies under injection-locking (left) and the resulting lock-range ($f_u - f_l$, right) versus RF input power.

TABLE I
MEASURED PERFORMANCE SUMMARY OF TRIPLER

Technology	90-nm CMOS
Power Consumption	23.8 mW from 1 V (Core – 9.6 mW, Output buffer – 14.2 mW)
Self-oscillation Frequency	59.7 – 60.6 GHz (10 samples measured)
Lock Range	56 – 65 GHz
Phase Noise referenced to Source	10.3 ± 1 dB (lower edge of range) 9.2 ± 1 dB (center of lock range) 11.5 ± 1 dB (upper edge of range)
Simulated I/Q Error	0.4° (phase) 0.04 dB (amplitude)

range increases with an increase in input power, due to stronger third harmonic generation. With injected signal levels in excess of 0 dBm, injection locking becomes less efficient and the curves saturate. With 0-dBm source power (316 mV-pk relative to 50 Ohm), the tripler has 8 GHz measured (9 GHz simulated) lock range from 56.5 to 64.5 GHz. At 56.5 GHz, the output power of the tripler is 8.6 dB lower than the -27 dBm peak power at 60.6 GHz in Fig. 12, and the phase noise difference at 100-kHz offset is 10.3 ± 1 dB, compared to 9.2 ± 1 dB in Fig. 13. At 64.5 GHz, the corresponding output power and phase noise differences are 10.9 dB and 11.5 ± 1 dB, respectively. The smaller output power at the edges of the lock range is due to the bandpass nature of both the ring oscillator and the output buffer, and the widening phase noise difference is consistent with known principles of injection locking.

Table I summarizes the measurement results. Measuring I/Q errors at 60 GHz was not possible with sufficient precision, hence only the simulated phase and amplitude errors (assuming nominal process and matching) of the quadrature outputs, 0.4° and 0.04 dB, respectively, are given.

It is interesting to note that a 60-GHz PLL (from a 60-GHz fundamental oscillator) with a power consumption of 80 mW produces a phase noise of -85.1 dBc/Hz at 1-MHz offset [23], whereas a 21-GHz PLL (from the recent literature [24]) consumes about one-quarter of the power (22.5 mW) and has phase noise of -95.7 dBc/Hz at 1-MHz offset, or more than 10 dB better than the 60-GHz PLL. If the tripler described in this work were used with the 21-GHz PLL, the total power consumption will be slightly more than one-half of that required by the 60-GHz PLL, yet the phase noise performance will be comparable. This supports the proposed advantage of using frequency multiplication, and this tripler in particular, for mm-wave signal generation.

V. Conclusion

A sub-harmonic injection-locked I/Q tripler is implemented in a 90-nm production bulk-CMOS technology. With a lock range of 8 GHz from 0-dBm injected power, the entire 60-GHz unlicensed band proposed for gigabit communication applications is covered. The results achieved in this work establish the feasibility of frequency multiplication in CMOS for mm-wave frequency synthesis, easing the design requirements for a lower frequency driving source PLL with respect to desired phase noise performance. The proposed design can be used in any desired transceiver architecture and frequency plan, and it creates alternatives to fundamental LO signal generation with the potential for lower overall power consumption. Also, as quadrature accuracy and phase noise are not coupled in this design, the I/Q tripler can be designed to provide high quadrature phase accuracy, and its output phase noise (when injection-locked) tracks the spectral characteristics of the lower-frequency source oscillator with a negligible penalty in phase noise performance.

Acknowledgment

The authors gratefully acknowledge J. Pekarik and D. Harame of IBM Microelectronics, Essex Junction, VT, for foundry access, and Prof. M. Spirito of TU Delft for measurement support.

References

[1] S. Pinel, S. Sarkar, P. Sen, B. Perumana, D. Yeh, D. Dawn, and J. Laskar, "A 90 nm CMOS 60 GHz radio," in *IEEE ISSCC Dig. Tech. Papers*, 2008, pp. 130–131.

[2] S. Trotta, H. Knapp, D. Dbra, K. Aufinger, T. F. Meister, J. Böck, W. Simbürger, and A. L. Scholtz, "A 79 GHz sige-bipolar spread-spectrum TX for automotive radar," in *IEEE ISSCC Dig. Tech. Papers*, 2007, pp. 20–21.

[3] E. Laskin, M. Khanpour, R. Aroca, K. W. Tang, P. Garcia, and S. P. Voinigescu, "A 95 GHz receiver with fundamental-frequency VCO and static frequency divider in 65 nm digital CMOS," in *IEEE ISSCC Dig. Tech. Papers*, 2008, pp. 180–181.

[4] A. J. Joseph, D. L. Harame, B. Jagannathan, D. Coolbaugh, D. Ahlgren, J. Magerlein, L. Lanzerotti, N. Feilchenfeld, S. S. Onge, J. Dunn, and E. Nowak, "Status and direction of communication technologies—SiGe BiCMOS and RFCMOS," *Proc. IEEE*, vol. 93, no. 9, pp. 1539–1558, Sep. 2005.

[5] P. Chevalier, C. Fellous, L. Rubaldo, F. Pourchon, S. Pruvost, R. Beerkens, F. Saguin, N. Zerounian, B. Barbalat, S. Lepilliet, D. D. D. Céli, I. Telliez, D. Gloria, F. A. F. Danneville, and A. Chantre, "230-GHz self-aligned SiGeC HBT for optical and millimeter-wave applications," *IEEE J. Solid-State Circuits*, vol. 40, no. 10, pp. 2025–2034, Oct. 2005.

[6] H. Li, B. Jagannathan, J. Wang, T.-C. Su, S. Sweeney, J. J. Pekarik, and Y. Shi, "Technology scaling and device design for 350 GHz RF performance in a 45 nm bulk CMOS process," in *Symp. VLSI Technology Dig. Tech. Papers*, 2007, pp. 56–57.

[7] S. Lee, B. Jagannathan, S. Narasimha, A. Chou, N. Zamdmer, J. Johnson, R. Williams, L. Wagner, J. Kim, J.-O. Plouchart, J. Pekarik, S. Springer, and G. Freeman, "Record RF performance of 45 nm SOI CMOS technology," in *IEDM Dig. Tech. Papers*, 2007, pp. 255–258.

[8] S. K. Reynolds, B. A. Floyds, U. R. Pfeiffer, T. Beukema, J. Grzyb, C. Haymes, B. Gaucher, and M. Soyuer, "A silicon 60-GHz receiver and transmitter chipset for broadband communications," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2820–2831, Dec. 2006.

[9] W. L. Chan, J. R. Long, and J. J. Pekarik, "A 56-to-65 GHz injection-locked frequency tripler with quadrature outputs in 90 nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, 2008, pp. 480–481.

[10] S. Emami, C. H. Doan, A. M. Niknejad, and R. W. Brodersen, "A highly integrated 60 GHz CMOS front-end receiver," in *IEEE ISSCC Dig. Tech. Papers*, 2007, pp. 190–191.

[11] C.-H. Wang, H,-Y. Chang, P.-S. Wu, K.-Y. Lin, T.-W. Huang, H. Wang, and C. H. Chen, "A 60 GHz low-power six-port transceiver for gigabit software-defined transceiver applications," in *IEEE ISSCC Dig. Tech. Papers*, 2007, pp. 192–193.

[12] A. Parsa and B. Razavi, "A 60 GHz CMOS receiver using a 30 GHz LO," in *IEEE ISSCC Dig. Tech. Papers*, 2008, pp. 190–191.

[13] N. D. Dalt, C. Knopf, M. Burian, T. Hartig, and H. Eul, "A 10 b 10 GHz digitally controlled LC oscillator in 65 nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, 2006, pp. 669–670.

[14] H. Knapp, H.-D. Wohlmuth, M. Wurzer, and M. Rest, "25 GHz static frequency divider and 25 Gb/s multiplexer in 0.12μm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, 2002, pp. 302–303.

[15] E. Seok, C. Cao, D. Shim, D. J. Areans, D. B. Tanner, C.-M. Hung, and K. K. O , "A 410 GHz CMOS push-push oscillator with an on-chip patch antenna," in *IEEE ISSCC Dig. Tech. Papers*, 2008, pp. 472–473.

[16] K. Kimura, "A bipolar four-quadrant analog quarter-square multiplier consisting of unbalanced emitter-coupled pairs and expansion of its input ranges," *IEEE J. Solid-State Circuits*, vol. 29, no. 1, pp. 46–55, Jan. 1994.

[17] J. P. Maligeorgos and J. R. Long, "A low-voltage 5.1-5.8-GHz image-reject receiver with wide dynamic range," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1917–1926, Dec. 2000.

[18] D. K. Ma and J. R. Long, "A subharmonically injected LC delay line oscillator for 17-GHz quadrature LO generation," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1434–1445, Sep. 2004.

[19] B. Razavi, "A study of injection locking and pulling in oscillators," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1415–1424, Sep. 2004.

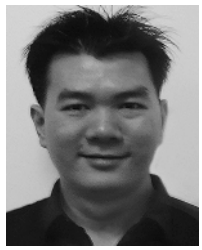
[20] T.-P. Liu and E. Westerwick, "5-GHz CMOS radio transceiver front-end chipset," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1927–1933, Dec. 2000.

[21] X. Zhang, X. Zhou, and A. S. Daryoush, "A theoretical and experimental study of the noise behavior of subharmonically injection-locked local oscillators," *IEEE Trans. Microw. Theory Tech.*, vol. 40, no. 5, pp. 895–902, May 1992.

[22] Foundry technologies 90-nm CMOS IBM product brief IBM, 2004.

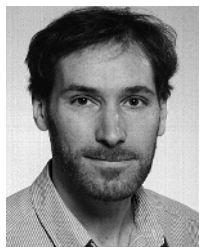
[23] C. Lee and S.-I. Liu, "A 58-to-60.4 GHz frequency synthesizer in 90 nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, 2007, pp. 196–197.

[24] Y. Ding and K. K. O , "A 21-GHz 8-modulus prescaler and a 20-GHz phase-locked loop fabricated in 130-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 42, no. 6, pp. 1240–1249, Jun. 2007.



Wei L. Chan (S'05) received the B.Eng. (Electrical) degree from the National University of Singapore, Singapore in 2002. In 2004, he received the M.Sc. degree in electrical engineering from the Delft University of Technology, Delft, The Netherlands, where he is currently working toward the Ph.D. degree.

His research interests include RF and mm-wave circuit design.



John R. Long (M'83) received the B.Sc. degree in electrical engineering from the University of Calgary, Canada, in 1984, and the M.Eng. and Ph.D. degrees in electronics from Carleton University, Ottawa, Canada, in 1992 and 1996, respectively.

He was employed for 10 years by Bell-Northern Research, Ottawa (now Nortel Networks R&D) involved in the design of ASICs for Gb/s fibre-optic transmission systems, and from 1996 to 2001 as an Assistant and then Associate Professor at the University of Toronto in Canada. Since January 2002, he has been Chair of the Electronics Research Laboratory at the Delft University of Technology, Delft, The Netherlands. His current research interests include transceiver circuits for integrated wireless and high-speed wireline data communications systems.

Prof. Long is a former Associate Editor of the IEEE Journal of Solid-State Circuits, and is currently a Distinguished Lecturer for the IEEE Solid-State Circuits Society. He received the NSERC Doctoral Prize and Douglas R. Colton and Governor General's Medals for research excellence, and is a co-recipient of Best Paper Awards from the International Solid-State Circuits Conference (ISSCC) in 2000 and 2007, the RFIC and European Wireless Symposia in 2006, and IEEE-BCTM in 2003. He was general chair and local organizer for the 2006 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), held in Maastricht, NL. He chairs the RF circuits subcommittee for ISSCC 2009, and is a member of the technical program committees for the European Solid-State Circuits (ESSCIRC), EuMIC and ICUWB conferences.