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A 56-GS/s 8-Bit Time-Interleaved SAR ADC in 28-nm CMOS

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SAR ADC

IN 28-NM CMOS

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Optical communication standards from 100 Gb/s to 200 Gb/s to 400 Gb/s generate the growing demands on the performance of ADC than ever before. For example, the 400 Gb/s interconnect framework requires 28 GHz, 37 GHz, 56 GHz and 112 GHz bandwidth ADC for 256-QAM, 64-QAM, 16-QAM and QPSK modulation, respectively.

This thesis presents a 56 GS/s 8 bit ADC in 28 nm CMOS. A low-noise parametric amplifier constituted by T/H circuit and sub-channel buffer is proposed to amplify the signal for the improvement of SNR and maintain the good linearity. A switched sub-channel buffer is also proposed that can be turned off during the track phase, thus avoiding the settling errors and achieving better linearity. To enhance the bandwidth, the ESD protection circuit is moved to the common-mode node instead of the input signal nodes to reduce the input parasitic capacitance; The input buffers are utilized to drive the heavy load presented by the T/H circuits; The inductive peaking is exploited at the inputs to tune out some parasitic capacitance; The parasitic capacitors of T/H circuits are used as sampling capacitors instead of adding extra sampling capacitor. The measurement results show that input bandwidth of the ADC is 31.5 GHz and the ENOB is larger than 5.2 bit up to Nyquist frequency, fulfilling the ADC requirements of 224 Gb/s DP-16QAM coherent receivers.

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INTRODUCTION

1.1. Motivation

WDM (Wavelength Division Multiplexing) optical networks are often used for modern optical systems because of communication traffic demands and economical consideration that push optical networks towards high-bit-rate long haul systems. The WDM system for long haul networks can transmit the light signals through optical fibers hundreds to thousands kilometers with only optical amplifiers to compensate power loss, rather than an entire array of expensive regenerators, to reduce the cost [39]. For example, Figure 1.1 shows a block diagram of the conventional optical link with expensive optical DCM (Dispersion Compensation Module); Figure 1.2 shows the block diagram of an economical digital coherent receiver with dispersion compensation completed in DSP (Digital Signal Processing).

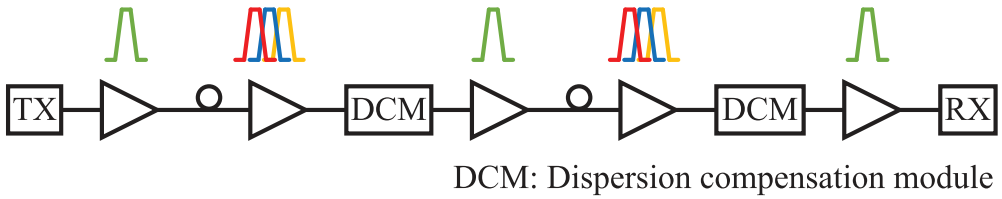

Figure 1.1. Conventional optical link with expensive optical DCM.

The light pulse propagation in optical fiber yields the nonlinear Schrodinger equation (NLSE). The non-ideal factors of fibers include chromatic dispersion (CD), polarization mode dispersion (PMD), self-phase modulation (SPM), cross-phase modulation (XPM), stimulated Raman scattering (SRS), stimulated Brillouin scattering (SBS), and four-wave mixing (FWM). Among those non-ideal factors, the chromatic dispersion and polarization-mode

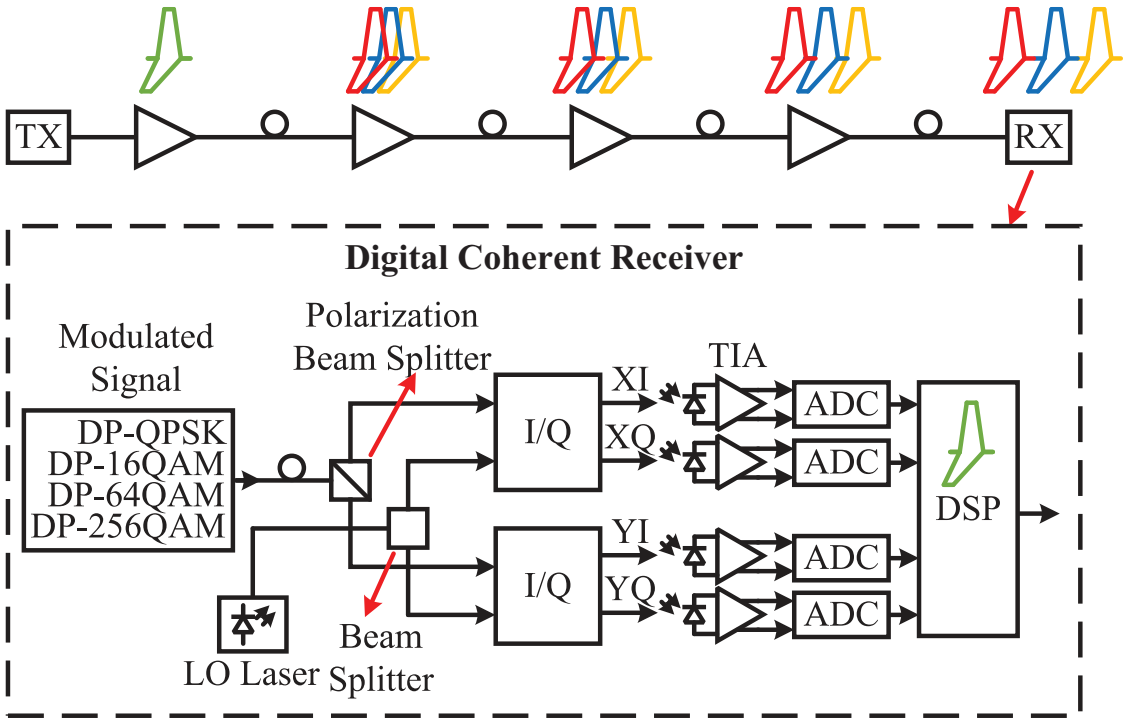

Figure 1.2. Digital coherent optical link with electronic dispersion compensation.

dispersion are two important linear factors that degrade the performance of optical communication system, and can be addressed by FIR-filter based equalization. In principle, the transmitted signal can be reconstructed by solving the nonlinear Schrodinger equation and computing the back propagation. By neglecting the loss coefficient and nonlinear effects, and using a frame of reference that is traveling with the pulse at the group delay, the nonlinear Schrodinger equation reduces to a linear partial-differential equation, which can be solved by computing the Fourier transform and inverse Fourier transform.

To perform the FIR-filter based equalization and compute Fourier transform and inverse Fourier transform, a digital signal processor (DSP) is needed. Compared with costly optical signal-processing, DSP can provide more flexibility and can integrate the optical receiver in CMOS technology. One key component to realize a DSP based optical receiver is the high-speed ADC (Analog-to-digital Converter). Several stringent requirements are imposed on the sampling rate, bandwidth (BW) and effective number of bits (ENOB) of the front-end

ADCs

The goal of this thesis is to design and implement a high-performance ADC for 112 G/224 Gb/s coherent receivers. Multiple solutions are proposed to overcome the design challenges.

1.2. Chapter Organization

The rest of thesis is organized as follows. In Chapter 2, we briefly introduce the fundamentals of analog-to-digital conversions, including the performance specifics, the design challenges. In Chapter 3, we describe a 64-way time-interleaved ADC. In Chapter 4, 64-way front-end interleaver is presented. Conclusions and an outlook are found in Chapter 5.

Chapter 2

OVERVIEW

In this chapter, the ADC concept and its specifications are reviewed. Understanding the ADC basics can give a good insight about how the ADC works and where the non-ideal errors come from.

2.1. Ideal Analog-to-Digital Conversion

Our natural world is analog: for example, sound, light and temperature are all continuous-time and continuous-amplitude signals. Compared with direct analog signal processing, digital signal processing has many metrics, such large noise tolerance, power efficiency, accuracy. Moreover, with the computer-aided design tools, the digital circuits design is quite compatible with the advances of new CMOS technology, resulting in very short design period. The register-transfer level (RTL) language for digital circuits design makes it easier to realize a delicate and complex algorithm. Based on the above advantages, digital signal processing shows its potentials to replace analog signal processing. As a result, ADC plays an important role in the interface circuits between analog signal and digital circuits.

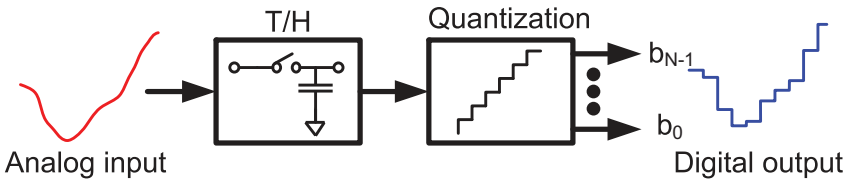

Figure 2.1. General block diagram of an ADC.

An ADC performs the function to sample the analog signal at discrete time intervals and quantize the signal amplitude into discrete steps. A basic block diagram of ADC is shown in Figure 2.1. The sample-and-hold (S/H) block is used to track the continuous-time analog signal and then hold the signal value for following quantization.

The solid lines in Figure 2.2 and Figure 2.4 show the transfer curves of mid-rise quantizer and mid-tread quantizer, respectively. In the curve of the Figure 2.2, the V_{in}=0 coincides with a step (rise), and hence it is called a mid-rise characteristic. In the curve of Figure 2.4, the V_{in}=0 occurs in the middle of flat portion (tread) of the curve. Such devices are called mid-tread quantizers [35]. It is often desirable to approximate the transfer curve with a straight line, as shown the dashed lines in Figure 2.2 and Figure 2.4. The deviation of the actual characteristics from the approximate one is called the quantization error or the quantization noise [35], as shown in Figure 2.3 and Figure 2.5. The analog input value Vin is converted into a digital value Dout using the Equation 2.1.

$$V_{\text{in}} = D_{\text{out}}\Delta - \epsilon_{\text{q}} \tag{2.1}$$

Here Δ is the least significant bit (LSB), $\Delta = V_{\text{FS}}/2^N$; V_{FS} represents the full scale input range; N represents the number of ADC bits; ϵ_{q} represents the quantization error, $-0.5\Delta < \epsilon_{\text{q}} < 0.5\Delta$. In the mid-rise quantizer case, $D_{\text{out}} = \cdots, -1.5, -0.5, 0.5, 1.5, \cdots$; In the mid-tread quantizer case, $Dout = \cdots, -2, -1, 0, 1, 2, \cdots$; Note that in both mid-rise quantizer case and mid-tread quantizer case, an offset can be simply added to map the value of D_{out} to $0, 1, \cdots, 2^N - 1$.

After sampling input analog signals, the high frequency beyond Nyquist frequency will be folded back to the Nyquist frequency band. Thus to avoid aliasing of the spectrum, the bandwidth of input signal should be less than the Nyquist frequency.

2.2. Track and Hold

The track-and-hold (T/H) block works in the most front of an ADC to convert the continuous-amplitude signal into discrete level signal. The accuracy of T/H circuits greatly determines the ADC performance.

Figure 2.6 shows the transfer curve of zero order hold (ZOH). Every period T_{s}, the T/H will update its output. The acquisition time of ideal T/H can be zero. However, the actual

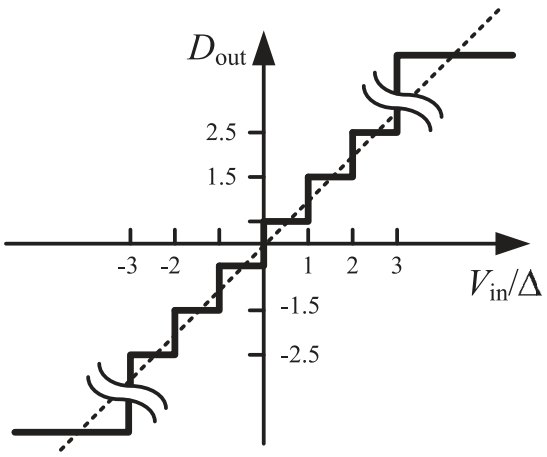

Figure 2.2. Transfer curve of the analog input and digital output of a symmetric mid-rise quantizer.

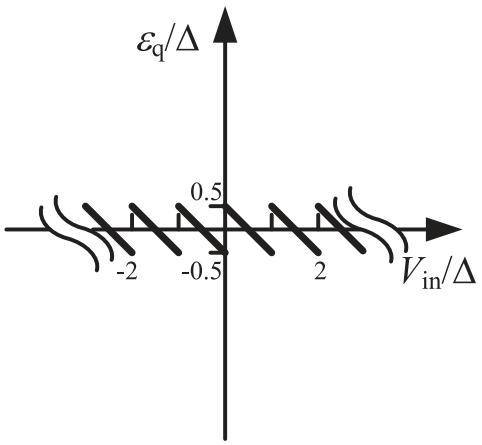

Figure 2.3. Quantization error function of a symmetric mid-rise quantizer.

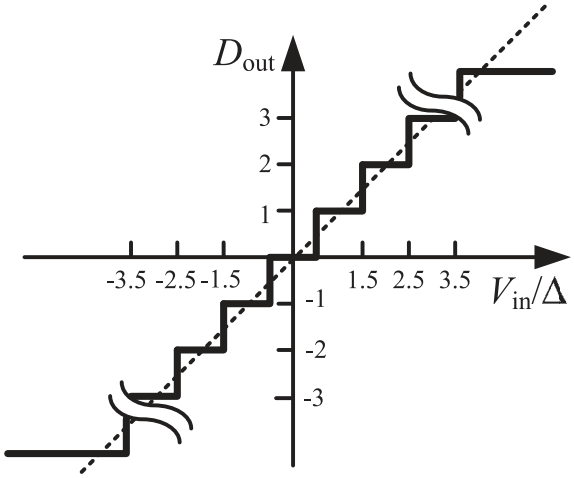

Figure 2.4. Transfer curve of the analog input and digital output of a symmetric mid-tread quantizer.

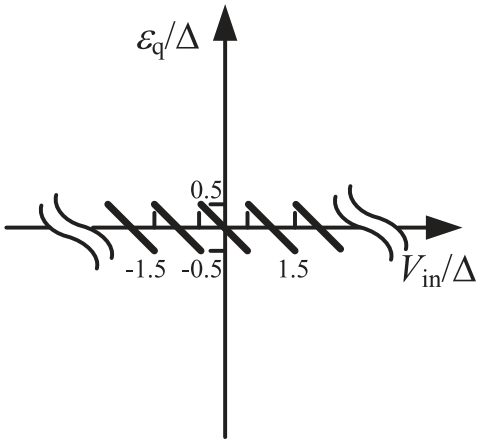

Figure 2.5. Quantization error function of a symmetric mid-tread quantizer.

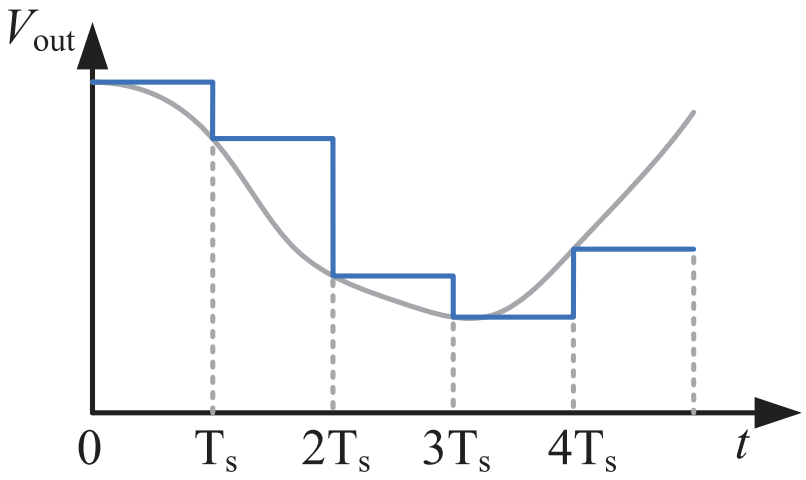

Figure 2.6. Transfer curve of ZOH.

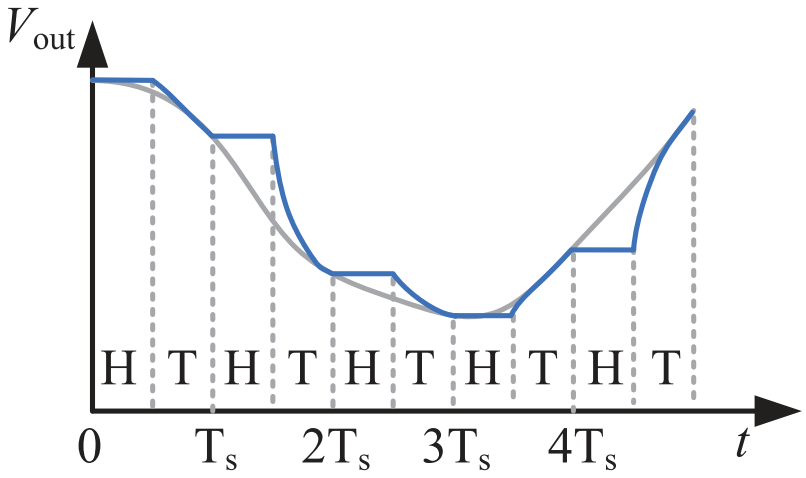

Figure 2.7. Actual transfer curve of T/H.

T/H circuit has finite bandwidth, which means it takes some acquisition time to track the input signal and leaves the rest time for the following signal quantization. The lower the track-mode bandwidth of T/H, the more acquisition time the T/H needs to track the input signal, resulting in less time for holding the output value. Thus high bandwidth of T/H circuit is preferred. Figure 2.7 shows the actual transfer curve of T/H circuit with $T_s/2$ acquisition time.

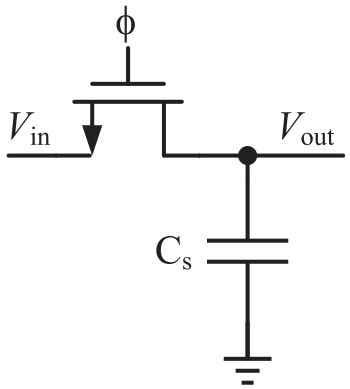

Figure 2.8. NMOS T/H circuit.

Figure 2.8 shows the circuit of NMOS T/H block, which contains a MOS switch and a sampling capacitor. The input/output waveform of the T/H circuit is shown in Figure 2.9. The T/H circuit is controlled by a clock signal named ϕ. When ϕ is high, the NMOS switch is closed and the T/H works in track mode. At the instant the switch opens, the T/H acquires the exact value of V_{in} and holds the value for the hold period.

Although the T/H looks quite simple, there are many non-ideal factors that will have impact on the ADC performance. The non-ideal factors include thermal noise, finite tracking bandwidth, clock jitter, signal dependent sampling instant, clock feedthrough, charge injection, switch off-mode feedthrough, track mode nonlinearity and droop.

2.2.1. Thermal Noise

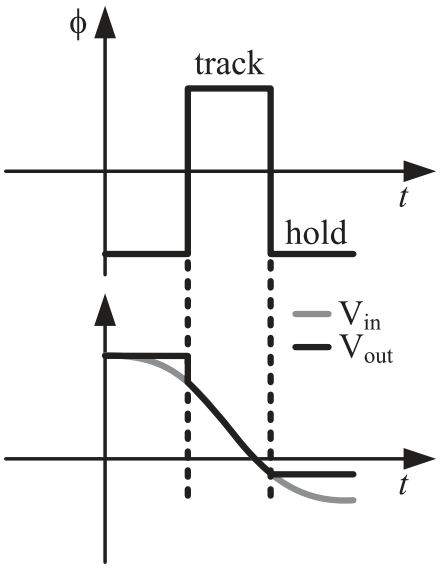

Figure 2.9. Input/output waveform of T/H circuit.

When the T/H works in track mode, the equivalent circuit to analyze the thermal noise is shown in Figure 2.10. The thermal noise power $\overline{v_{\mathrm{o,tot}}^2}$ impose on the output of T/H can be represented in Equation 2.2.

$$\overline{v_{\mathrm{o,tot}}^2} = kT/C \tag{2.2}$$

where $k = 1.3810^{-23}$J/K, represents the Boltzmann constant; T is the turned-on resistors absolute temperature in kelvins; C_{s} represents the value of sampling capacitor.

If the sampling capacitor C_{s} is too small, then thermal noise becomes the dominant noise, resulting in the degradation of performance. In contrary, if the sampling capacitor C_{s} is too large, quantization noise becomes the dominant noise (exclude other noise sources), which means the ADC performance will not be improved obviously by increasing the capacitor size, but the speed is slowed down. For Nyquist rate ADCs, the sampling capacitor size is usually chosen based on having thermal noise smaller or equal or at times larger compared to quantization noise. If we make kT/C_{s} noise equal quantization noise, the required value of

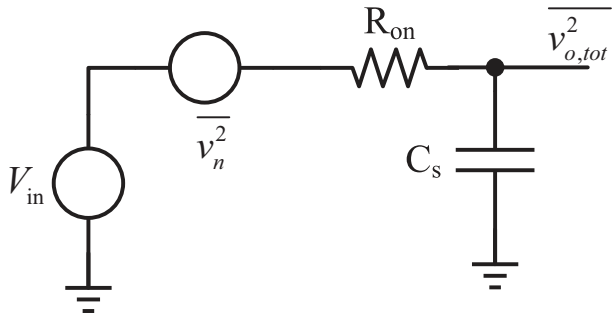

Figure 2.10. Equivalent circuit in track mode to analyze the thermal noise power.

sampling capacitor size of an 8 bit ADC with 1.2 V_{pp} input range is calculated in Equation 2.3.

$$\frac{kT}{C_s} = \frac{\Delta^2}{12} \Rightarrow C_s = 12kT\left(\frac{2^N}{V_{FS}}\right) = 2.26 \text{ fF} \tag{2.3}$$

Such small sampling capacitor size is quite easy to achieve in the circuit for the target of designing a 56 GS/s 8 bit ADC.

2.2.2. Finite Track-mode Bandwidth

When the T/H circuit works in track mode, the switch is turned on and the resistance of the switch combined with sampling capacitor turns the sampling network into a low-pass filter with a time constant $\tau = R_{on}C_s$, as shown in Figure 2.11.

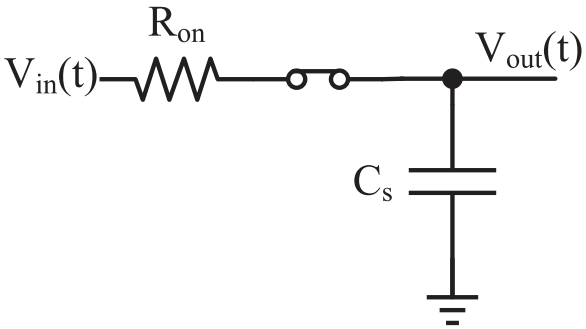

Figure 2.11. Track mode T/H circuit with turn-on resistor R_{on}.

Assuming V_{in} is constant (actually V_{in} can be a variable signal) during the sampling period and C_{s} is initially discharged before the track mode period, the output of T/H $V_{\text{out}}(t)$ can be expressed in Equation 2.4.

$$V_{\text{out}}(t) = (1 - e^{-t/\tau})V_{\text{in}}(t) \tag{2.4}$$

At the instant $t = T_{\text{s}}/2$ the switch opens, the output value of T/H is held. By letting the track mode error between $V_{\text{in}}(t)$ and $V_{\text{out}}(t)$ be far less than the quantization step Δ, Equation 2.5 can be obtained.

$$V_{\text{in}}(t = 0.5T_{\text{s}}) - V_{\text{out}}(t = 0.5T_{\text{s}}) \ll \Delta \Rightarrow e^{0.5T_{\text{s}}/\tau}V_{\text{in}}(t = 0.5T_{\text{s}}) \ll \Delta \tag{2.5}$$

Considering the worst case when $V_{\text{in}}(t) = V_{\text{FS}} = 2^N\Delta$, the requirement for switch turned-on resistance can be obtained, as shown in Equation 2.6.

$$R_{\text{on}} = \frac{1}{2f_{\text{s}}C_{\text{s}}\ln(2^N)} \tag{2.6}$$

Here f_{s} represents the sampling frequency. The values of R_{on} and C_{s} determine the tracking bandwidth of S/H circuit, which further determines how promptly the output of T/H can follow its input. Typically, the tracking mode bandwidth should be many times greater than the maximum signal bandwidth. Insufficient tracking bandwidth will case tracking error, as shown in Figure 2.12.

2.2.3. Clock Jitter

The operation of T/H circuit is controlled by a sampling clock that dictates the instant of switch turned-on and turned-off. Ideally, the T/H sampling clock edge should be at the fixed instant to carry out the uniform sampling. Due to the physical position, temperature, clock length and noise, the actual sampling clock may be different from the designed clock.

The errors of a clock can be divided as clock skew and clock jitter. The fixed clock skew will not degrade the single-channel ADC performance since the sampling interval is

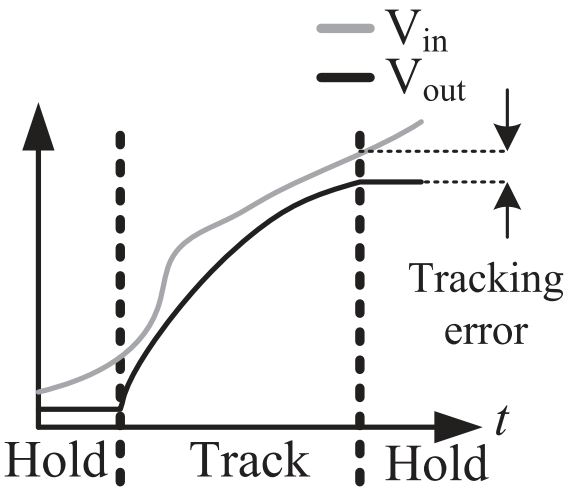

Figure 2.12. Tracking error caused by insufficient tracking bandwidth.

identical. But the non-uniform clock skew among time-interleaved T/H paths will cause signal significant errors. The sampling clock jitter causes the random variation of sampling instant Δt, as shown in Figure 2.13. Such sampling jitter will cause an error voltage to be added into the desired held value. The error is proportional to the product of derivative of the input signal at the sampling instant and the sampling edge deviation Δt [46].

Assuming the input is a sinusoidal signal, the sampled and held value due to the sampling clock jitter can be expressed in Equation 2.7 and Equation 2.8. Here t_0 represents the instant when the switch opens; A represents the input signal amplitude; ω represents the angular frequency.

$$V_{\text{out}}(t_0) = A\sin[\omega(t_0 + \Delta t)] = A\sin(\omega t_0)\cos(\omega \Delta t) + \cos(\omega t_0)\sin(\omega \Delta t) \tag{2.7}$$

For small value of Δt, the Equation 2.7 can be simplified as

$$V_{\text{out}}(t_0) \approx A\sin(\omega t_0) + \omega \Delta t A\cos(\omega t_0) \tag{2.8}$$

The error $\epsilon(t_0)$ caused by sampling clock jitter can be calculated by Equation .

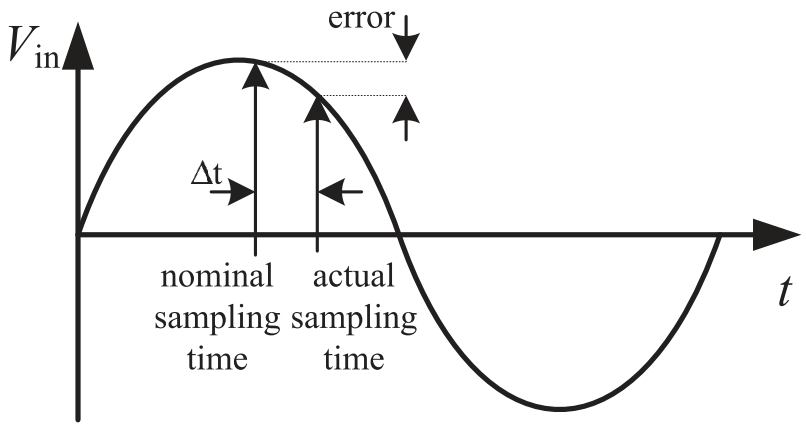

Figure 2.13. Error caused by sampling clock jitter.

$$\epsilon(t_0) = V_{\text{out}}(t_0) - A\sin(\omega t_0) \approx \omega \Delta t A\cos(\omega t_0) \tag{2.9}$$

Assuming the sampling instant t_0 is uniformly distributed in the input signal period, the noise power of the error signal can be obtain by Equation 2.10. Here T_{in} represents the period of the input sinusoidal signal; δt represents the standard deviation of clock jitter.

$$\overline{\epsilon^2(t)} = \overline{\Delta t^2}\frac{1}{T_{\text{in}}}\int_0^{T_{\text{in}}} [A\omega\cos(\omega t)]^2 \, dt = \frac{A^2\omega^2\delta_{\text{t}}^2}{2}. \tag{2.10}$$

Considering the case that the noise only comes from sampling clock jitter, the SNR can be obtained in Equation 2.11.

$$SNR = \frac{A^2/2}{(A^2\omega^2\delta_{\text{t}}^2/2)} = \frac{1}{\omega^2\delta_{\text{t}}^2} \tag{2.11}$$

2.2.4. Signal Dependent Sampling Instant

Since the falling of the actual sampling clock is not zero, the sampling instant also depends on the input signal. The switch turned-off happens at the instant when the voltage of clock

$\phi(t)$ equals the sum of input signal $V_{\text{in}}(t)$ and the threshold voltage of transistor V_{th}, as shown in Figure 2.14.

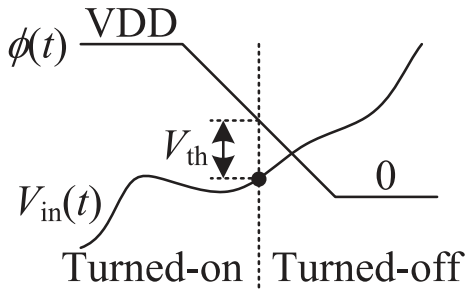

Figure 2.14. Signal dependent sampling instant.

When $V_{\text{in}}(t) = 0$, the switch is turned off every time $\phi(t) = V_{\text{th}}$ at the sampling clock falling edge; When $V_{\text{in}}(t) > 0$, the switch is turned off earlier than that in the case of $V_{\text{in}}(t) = 0$; When $V_{\text{in}}(t) < 0$, the switch is turned off latter than that in the case of $V_{\text{in}}(t) = 0$. Note that considering the transistor body effect, the threshold voltage of transistor also depends on input signal. Therefore, to mitigate the sampling instant variation, the sharp clock edge and small signal swing of $V_{\text{in}}(t)$ should be used in the design of ADC.

2.2.5. Clock Feedthrough and Charge Injection

At the instant the sampling switch turns off, the parasitic capacitor across NMOS gate and drain C_{gd} and the parasitic capacitor across NMOS gate and source C_{gs} will cause clock feedthrough. The charges that stored in the channel of NMOS transistor need to be released, resulting in charge injection. Both of clock feedthrough and charge injection will change the sampled voltage value at capacitor C_{s}.

A non-ideal T/H circuit with C_{gd}, C_{gs} and channel charge Q_{ch} noted is shown in Figure 2.15. The charge Q_{ch} stored in channel during the switch-on is given by Equation 2.12. Here C_{ox} represents gate oxide capacitance per unit area; W and L represent the width and length of the transistor, respectively.

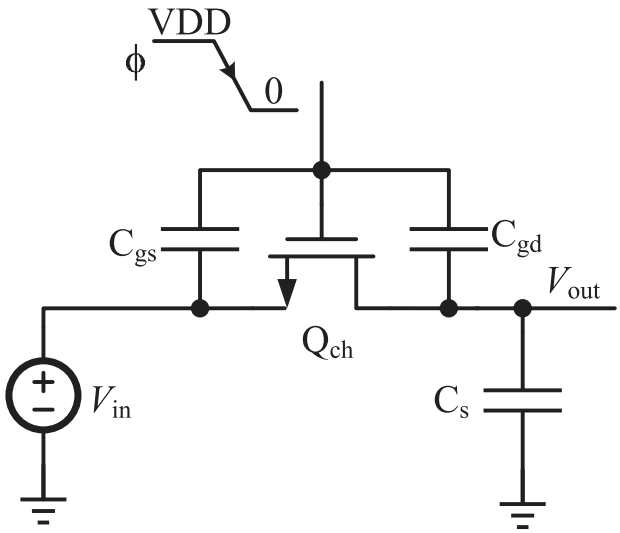

Figure 2.15. The T/H with non-idealities for the clock feedthrough and charge injection analysis.

$$Q_{\text{ch}} = C_{\text{ox}} W L \left(V_{\text{DD}} - V_{\text{in}} - V_{\text{th}}\right) \tag{2.12}$$

Considering the case that the switch is turned off by a sampling clock with sharp falling edge, the charge stored on C_{gd} during the switch was turned on will redistributed between C_{gd} and C_{s}. Such charge redistribution will cause the output of T/H changing a certain voltage. By using superposition principle, the voltage change ΔV is given by Equation 2.13.

$$\Delta V = -\frac{C_{\text{gd}}}{C_{\text{gd}} + C_{\text{s}}} V_{\text{DD}}, \text{for fast turn off case} \tag{2.13}$$

Considering the case that the switch is controled by a slow sampling clock, the charged stored on C_{gd} can be absorbed by the input source until the voltage of the sampling clock reaches $V_{\text{in}} + V_{\text{th}}$ the instant when switch is turned off. Thus only the amount of charges $(V_{\text{in}} + V_{\text{th}})C_{\text{gd}}$ will be redistributed between C_{gd} and C_{s}. The voltage change of T/H output is given by Equation 2.14.

$$\Delta V = -\frac{C_{\mathrm{gd}}}{C_{\mathrm{gd}} + C_{\mathrm{s}}} \left(V_{\mathrm{in}} + V_{\mathrm{th}}\right), \text{for slow turn off case} \tag{2.14}$$

For the switch fast turn-off case, the charges stored in the channel of transistor will be absorbed by both input source and output capacitors. Assuming the charges are equally absorbed by the input and output, the voltage change of T/H output is given by Equation 2.15. For the switch slow turn off case, the charge injection will not have impact on the output of T/H circuit, because the charges can be absorbed by the input source.

$$\Delta V = -\frac{C_{\mathrm{ox}} W L \left(V_{\mathrm{DD}} - V_{\mathrm{th}} - V_{\mathrm{in}}\right)}{2\left(C_{\mathrm{gd}} + C_{\mathrm{s}}\right)} \tag{2.15}$$

Considering the clock feedthrough and charge injection effect by combining Equation 2.13, 2.14, 2.15 together, the actual transfer function of T/H can be obtained, as shown in Equation 2.16 and Equation 2.17. For fast switch turn-off case:

$$V_{\mathrm{out}} = \left[1 + \frac{C_{\mathrm{ox}} W L}{2\left(C_{\mathrm{gd}} + C_{\mathrm{s}}\right)}\right] V_{\mathrm{in}} - \left[\frac{C_{\mathrm{gd}}}{C_{\mathrm{gd}} + C_{\mathrm{s}}} V_{\mathrm{DD}} + \frac{C_{\mathrm{ox}} W L}{2\left(C_{\mathrm{gd}} + C_{\mathrm{s}}\right)} \left(V_{\mathrm{DD}} - V_{\mathrm{th}}\right)\right] \tag{2.16}$$

For slow switch turn-off case:

$$V_{\mathrm{out}} = \left(1 - \frac{C_{\mathrm{gd}}}{C_{\mathrm{gd}} + C_{\mathrm{s}}}\right) V_{\mathrm{in}} - \frac{C_{\mathrm{gd}}}{C_{\mathrm{gd}} + C_{\mathrm{s}}} V_{\mathrm{th}} \tag{2.17}$$

Therefore, the clock feedthrough and charge injection will cause the gain error and offset error for the ADC.

2.2.6. Switch Off-mode Feedthrough

Besides clock feedthrough, the input signal feedthrough during the switch is turned off, will also have impact on the T/H output, as shown in Figure 2.16. During the T/H works in hold mode, the gate of sampling switch is connected to ground through a turn-on switch with turn-on resistance R_{on}. The substrate of the sampling switch is also connected to ground

through the substrate resistor. The parasitic capacitors C_{gs}, C_{gd}, C_{sb} and C_{db} constitute high-pass feedthrough paths past an open switch. To cancel the switch off-mode feedthrough, the scheme in Figure 2.17 was used in [53], [43]. Differential inputs are used in Figure 2.17, thus the positive path sampling switch off-mode feedthrough can be canceled by the negative path dummy switch feedthrough. For the negative path, sampling switch off-mode feedthrough can be canceled by the positive path dummy switch feedthrough.

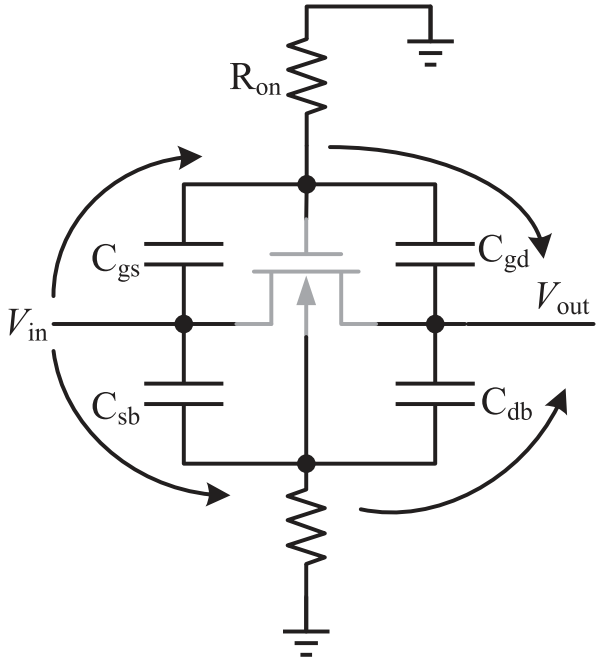

Figure 2.16. Switch off-mode feedthrough.

2.2.7. Track-mode Nonlinearity

When the T/H circuit works in the track mode, the turn-on resistance of the transistor is given by Equation 2.18. Here μ represents the mobility of carriers.

$$R_{on} = \frac{1}{\mu C_{ox} W/L \, (V_{DD} - V_{th} - V_{in})} \tag{2.18}$$

The switch turn-on resistance depends on the input signal. In track mode, if the input signal was slow, the T/H output could track the input well, however, when the input voltage

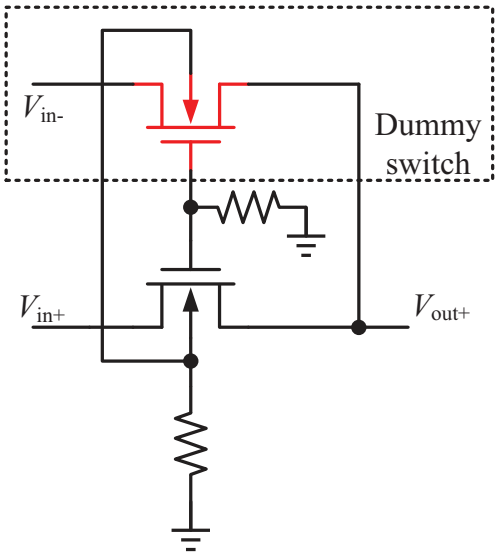

Figure 2.17. The scheme with dummy switch to cancel the switch off-mode feedthrough.

is high, the output will get distorted due to the increase of R_{on}. The signal-dependent R_{on} causes the signal-dependent track-mode bandwidth. The track-mode bandwidth should be sufficiently large to compress the distortions caused by the signal-dependent R_{on}.

2.2.8. Droop

Another non-ideal effect for T/H is the hold-mode droop. Although in the hold mode the sampling switch is turned off, due to the off-switch leakage, transistor junction diodes leakage and gate leakage, the held voltage value will gradually decrease, as shown in Figure 2.18.

2.3. ADC Performance Metrics

In order to set the criteria for estimating the performance of the ADCs, there are many specifications utilized, which can be classified as static specifications and dynamic specifications. The static specifications include differential nonlinearity (DNL) and integral nonlinearity (INL). The dynamic specifications include signal-to-noise ratio (SNR), signal-to-noise and distortion ratio (SNDR or SINAD), spurious free dynamic range (SFDR), effective num-

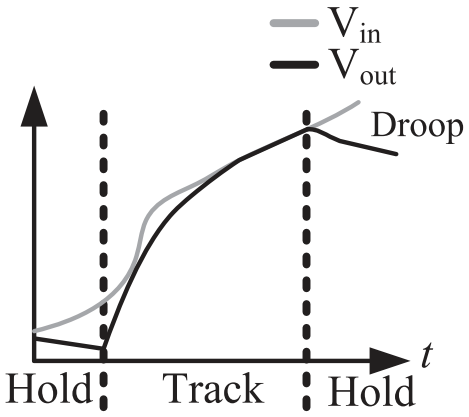

Figure 2.18. Droop impact on the transfer curve of T/H circuit.

ber of bits (ENOB). Depending on the applications, the emphasis on these specifications will vary. For example, image processing cares more about DNL, INL, SNDR, ENOB, where DNL is relative with the sharp-edge detection. However, the specifications of SFDR, SNDR are more of concern, in a wideband digital receiver, because the linear dynamic range determines the detection of low-level signals in a strong interference environment.

2.3.1. Static Specifications

INL and DNL are the most important specifications to illustrate the static linearity of an ADC. The definitions of INL and DNL of an ADC can be illustrated in the transfer curve, as shown in Figure 2.19. INL is also called as relative accuracy and defined as the deviation of the output code a converter from the straight line drawn through zero and full scale. For example, let $\widetilde{X}_{\mathrm{a,m}}$ be the corresponding analog input value of code m; and let the ideal corresponding analog input of code m be $X_{\mathrm{a,m}}$. The INL of an ADC output m can be written as [20, 47]

$$INL_{\mathrm{m}} = \widetilde{X}_{\mathrm{a,m}} - X_{\mathrm{a,m}}. \tag{2.19}$$

The INL should not deviate more than $\pm 1/2$ LSB to ensure the monotonic property of an ADC. A monotonic ADC means that there is no missing code in its transfer curve [52].

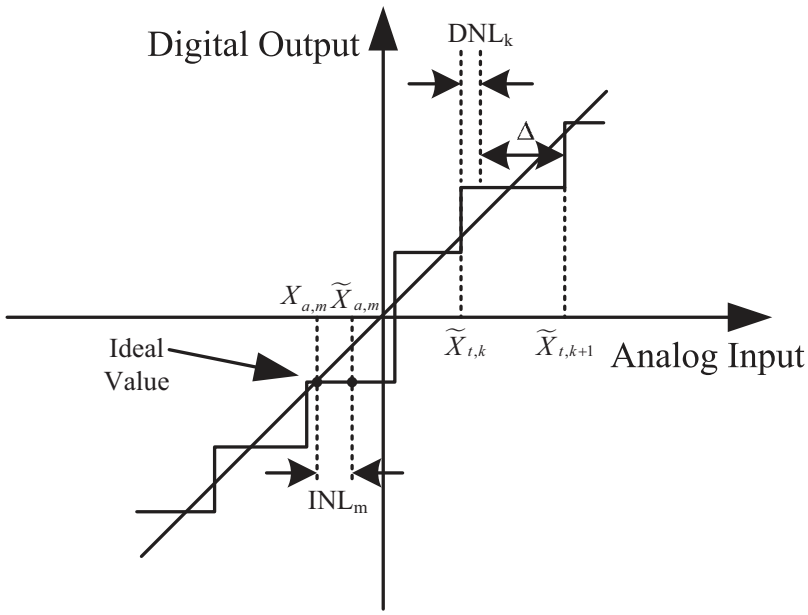

Figure 2.19. Transfer curve of an ADC.

The DNL is defined as the difference between two adjacent analog outputs minus the ideal step size Δ. The DNL implies the amount of deviation that the step size of a non-ideal data converter different from that of an ideal ADC. The DNL of an ADC output can be written as

$$DNL_{\mathrm{k}} = \widetilde{X}_{\mathrm{a,k}} - \widetilde{X}_{\mathrm{a,k+1}} - \Delta. \tag{2.20}$$

The relation between INL and DNL is given by

$$INL_{\mathrm{m}} = \sum_{i=1}^{m} DNL_{\mathrm{i}}. \tag{2.21}$$

2.3.2. Dynamic Specifications

Since the impact of some non-ideal factor is proportional to the frequency of input signal, i.e. clock jitter, finite track-mode bandwidth of S/H circuit, the static specifications cannot

characterize the performance of the ADC adequately. Dynamic testing can show both static and dynamic errors.

The definition of signal-to-noise ratio (SNR) is defined as the ratio of signal power to total noise power, as shown in equation 2.22. The total noise power includes the power of all frequency components except the DC signal, input signal and its harmonics (usually 2nd to 7th order harmonics are considered). Both quantization noise and electronic noise will affect the SNR

$$SNR = \frac{Signal\ Power}{Total\ Noise\ Power}. \tag{2.22}$$

The ideal ADC is a deterministic device, which means the input signal completely determines the digital conversion result and the quantization error e_{q}. However, if the input signal of ADC stays within the input range and changes by sufficiently large amounts from sample to sample, then the quantization error e_{q} can be assumed to be a white noise [35]. Assuming the quantization error e_{q} is uniformly distributed, the power of the quantization noise is given by

$$\bar{e_{\mathrm{q}}^2} = \frac{\Delta^2}{12}. \tag{2.23}$$

Assuming the noise only contributed by the quantization error, and the amplitude of the input single-tone sinusoidal signal is $V_{\mathrm{FS}}/2$, the SNR is given by

$$SNR = 10\log_{10}\left(\frac{V_{\mathrm{FS}}^2}{8}\right) / \left(\frac{\Delta^2}{12}\right) = (6.02N + 1.76)\ \mathrm{dB}. \tag{2.24}$$

Here N is the number of bits of ADC. Note that to randomize the quantization error, the input signal frequency should satisfy the equation 2.25, otherwise the quantization error is highly deterministic and periodic.

$$f_{\mathrm{in}} = \frac{P}{N_{\mathrm{pt}}} f_{\mathrm{s}}. \tag{2.25}$$

Here N_{pt} is the number of fast Fourier transform points; P is an integer number that makes N_{pt} and P mutually prime; f_{in} and f_{s} are the input frequency and sampling frequency,

respectively.

The nonlinearities of an ADC cause the appearance of harmonic distortions in the spectrum. The total harmonic distortion (THD) describes the performance degradation due to harmonic distortions. The definition of THD is given by

$$THD = \frac{\sqrt{\sum_{k=2}^{N_{\mathrm{H}}+1} A_{\mathrm{k}}^2}}{A_1}. \tag{2.26}$$

where NH represents the number of harmonics to be considered; A1 and Ak represent the fundamental and the k-th order harmonic, respectively [48].

The signal-to-noise and distortion ratio (SNDR or SINAD) is defined as the ratio of signal power to the noise and distortion power, as shown in equation 2.27. The noise and distortion power includes all frequency components except DC and input signal frequency components.

$$SNDR = \frac{Signal\ Power}{Noise\ and\ Distortion\ Power}. \tag{2.27}$$

The spurious free dynamic range is defined as the ratio of the signal power to the largest spurious power, as shown in equation 2.28. The largest spur is often but not necessarily a harmonic of the input tone, for example the spurs caused by the inter-channel mismatches of a time-interleaved ADC may not be the harmonics.

$$SFDR = \frac{Signal\ Power}{Largest\ Spurious\ Power}. \tag{2.28}$$

Since the theoretical value of SNR is only depends on the number of ADC bits, as shown in equation 2.29, a simple reverse operation can be performed to estimate the effective resolution of a real ADC by:

$$ENOB = \frac{SNDR(\mathrm{dB}) - 1.76\mathrm{dB}}{6.02\mathrm{dB}}. \tag{2.29}$$

In order to establish measures to compare the performance of different ADCs, the figure of merit (FOM) is utilized to combine several performance metrics one single number for evaluating the ADC. The author in [13] defines the product of sampling rate and number of effective quantization levels as FOM1 shown in equation 2.30.

$$FOM1 = f_s \cdot 2^{ENOB}. \tag{2.30}$$

Another useful figure of merit is shown in equation 2.31, which can represent the power efficiency energy per conversion [16].

$$FOM2 = \frac{Power\ Consumption}{f_s \cdot 2^{ENOB}}. \tag{2.31}$$

Because the frequency of input signal will affect the SNDR of ADC, twice the signal bandwidth is commonly used to replace the sampling frequency f_s.

2.4. Design Challenges

To realize a long-haul 100 Gb/s optical transport network, a coherent receiver is required with certain modulation scheme, such as, DP-4QAM (dual polarization 4 quadrature amplitude modulation), DP-16QAM, DP-64QAM and DP-256QAM [36]. Figure 2.20 shows the constellations of 4QAM, 16QAM, 64QAM and 256QAM. After demodulation, PAM2, PAM4, PAM8 and PAM16 signals can be obtained as I and Q signals in Figure 2.22 from 4QAM, 16QAM, 64QAM and 256QAM. An example of the configuration of a 112 Gb/s DP-QPSK digital coherent receiver is shown in Figure 2.21.

The digital coherent receiver needs four ADC channels since there are two optical polarizations and each needs two ADCs to digitize the I and Q signals. Take the DP-QPSK for example: to achieve 100 Gbit/s line rate, at least 112 Gb/s is required to allow for forward error correction (FEC) overhead [4]. the incoming optical signal should have a data rate of 56 Gbit/s for its vertical polarization and horizontal polarization. By splitting the input optical signal through PBS (polarization beam splitter) and mixing with a local oscillator

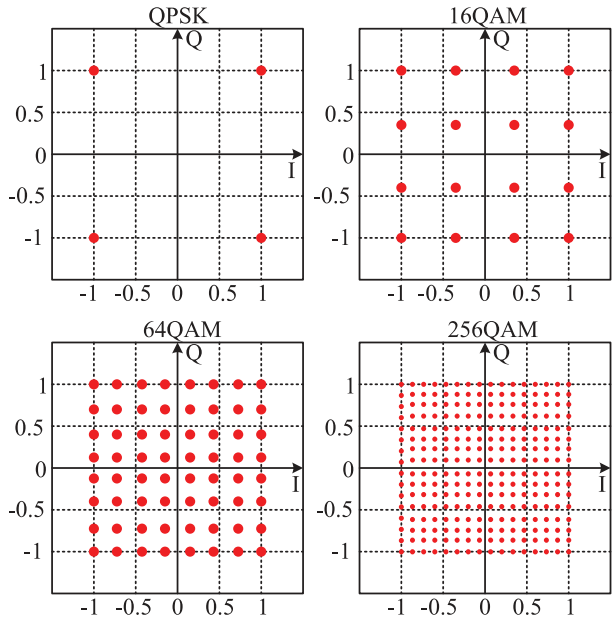

Figure 2.20. Constellation of 4QAM, 16QAM, 64QAM and 256QAM.

signal from BS (beam splitter), the PAM2 (also known as BPSK) signals can be obtained as I and Q signals. Since each QAM symbol contains 2 bits, the I and Q signals should have a baud rate (or symbol rate/modulation rate) of 28 Gbaud/s. Then the optical signals of I and Q are converted into electrical signals through photodetectors, TIAs (transimpedance amplifiers), AC coupling for ADC to digitize. To overcome aliasing issues, the sampling rate of ADC is assumed to be twice the bit rate, which is 56 GS/s. Since the first notch of the spectrum of a 28 Gbaud/s PAM signal is at 28 GHz, the bandwidth of the ADC should be larger than 28 GHz without losing too much high frequency information. Similarly, the ADC bandwidth requirements for the 112 Gb/s DP-16QAM, DP-64QAM and DP-256QAM are 14 GHz, 9.25 GHz and 7 GHz, respectively. The ADC bandwidth requirements for the 224 Gb/s DP-QPSK, DP-16QAM, DP-64QAM and DP-256QAM are 56 GHz, 28 GHz, 18.5 GHz and 14 GHz, respectively.

Figure 2.22 shows the two-stage T/H circuit with a sub-channel buffer. For the ADCs work in 100/200/400 Gb/s optical communication system, the input signal frequency can be tens of Giga Hertz (Hz). However, the bandwidth of the sub-channel buffers cannot be that

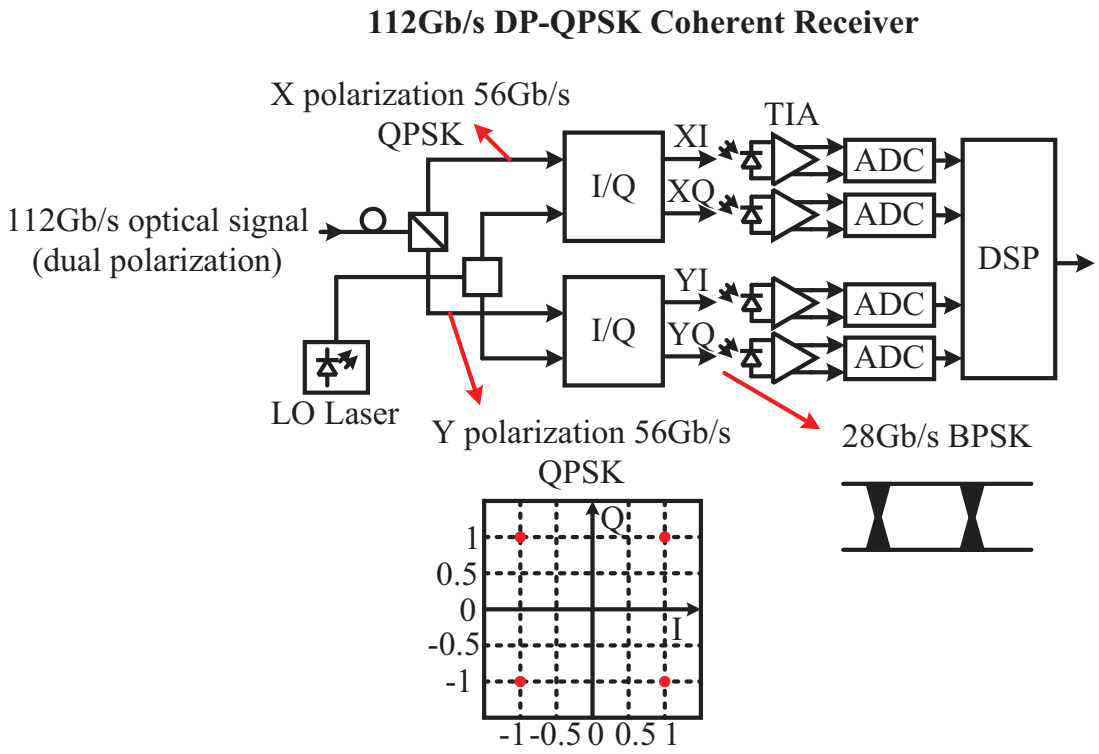

Figure 2.21. Configuration of a 112 Gb/s DP-QPSK digital coherent receiver.

high especially considering the load due to the long signal routings to single-channel ADCs. For a continuously working sub-channel buffer, if it does not have enough bandwidth to track the input signal during the track phase, then in the hold phase, the settling error in the track mode will be coupled to the node of sampling capacitor through the parasitic capacitance between the input and the output of the sub-channel buffer, resulting in degradation of the linearity.

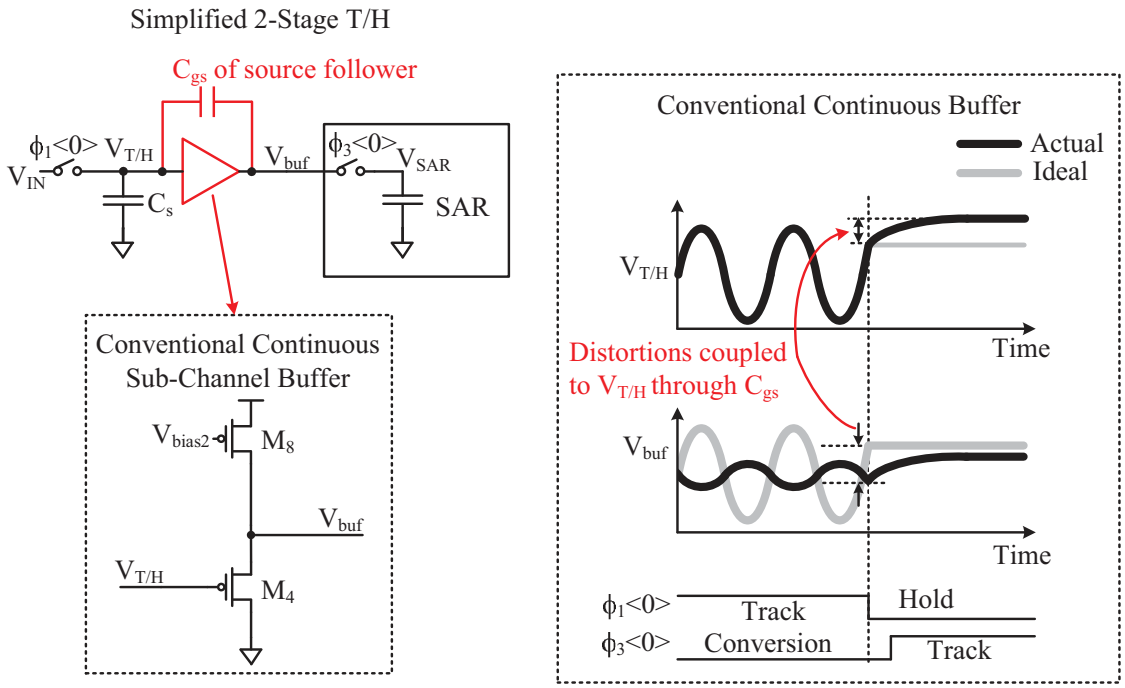

Figure 2.22. Two-stage T/H circuit and waveforms when sampling a high-speed input signal with limited buffer bandwidth.

As transistor operation voltages scales, a problem plaguing the T/H circuits is not enough voltage headroom to turn on the T/H switch, resulting in nonlinearity, and limiting the signal swing that can be rendered to sub-channel ADC. This is because the turned-on resistance is inversely proportional to the gate-source voltage of the switch. Thus for a certain break-down voltage of gate-to-source, there is a tradeoff between linearity and signal-to-noise ratio

(SNR). The turned-on resistance can be expressed as:

$$R_{\text{on,NOMS}} = \frac{L}{\mu C_{\text{ox}}\left(V_{\text{GS}} - V_{\text{TH}}\right)} = \frac{L}{\mu C_{\text{ox}}\left(V_{\text{DD}} - V_{\text{IN}} - V_{\text{TH}}\right)} \tag{2.32}$$

where μ is the mobility of charge carrier, C_{ox} is the unit gate oxide capacitance, W is the width of the switch, L is the length of the switch, V_{GS} is the gate-to-source voltage, V_{TH} is the threshold voltage, V_{DD} is supply voltage and V_{IN} is the input signal voltage. Figure

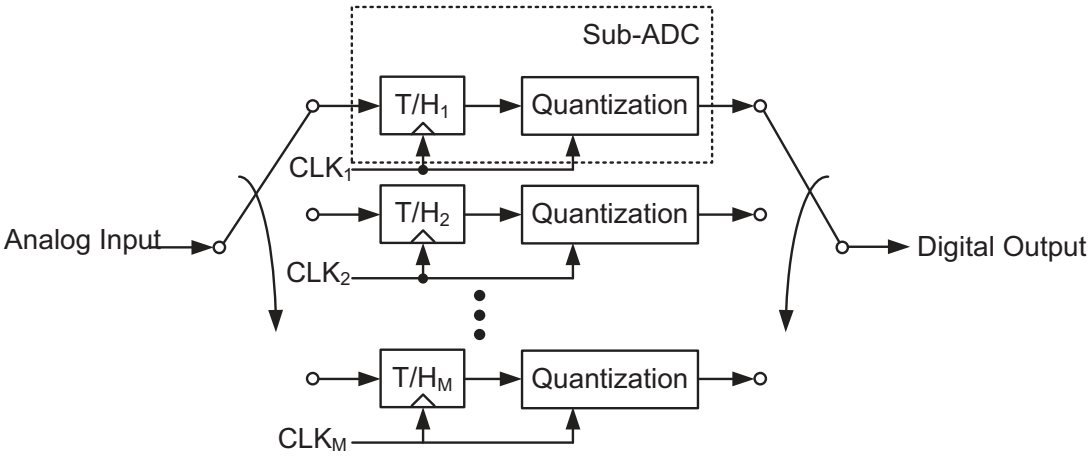

Figure 2.23. Conceptual diagram of a time-interleaved ADC with M channels.

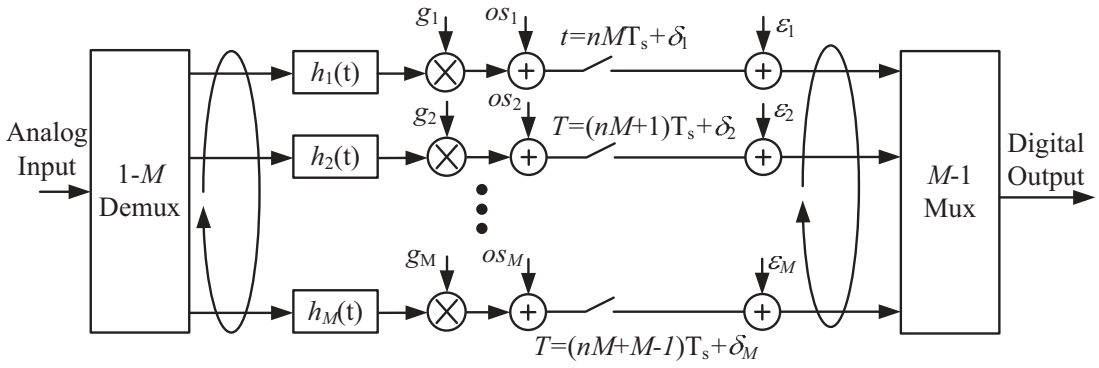

Figure 2.24. Time-interleaved ADC model with inter-channel mismatches.

2.23 shows a time-interleaved ADC system, where the M represents the number of channel

ADCs in the time-interleaved ADC; CLK_1 to CLK_M with phase shift of T_s from each other, represent the clock signal for each channel ADC. The output of T/H in each channel is updated at the falling edge of the clock. The individual speed of each channel is M/T_s, which is M times slower than the speed of overall throughput $f_s = 1/T_s$.

One problem in time-interleaved ADC that must be solved is the inter-channel mismatches. Typical mismatch errors include offset, gain, bandwidth mismatches, and sampling clock skew. Figure 2.24 shows a typical model of an M-way time-interleaved ADC. Block $h_1(t)$ to $h_M(t)$ model the independent frequency responses of T/H. The offset and gain of each channel are modeled by the term os_1 to os_M and g_1 to g_M, respectively. Finally, δ_1 to δ_M and ϵ_1 to ϵ_M model the sampling time errors and quantization errors, respectively.

In the next section, the details of the ADC design will be introduced, which include our proposed methods to solve the non-ideal factors, such as bandwidth limitations, clock feedthrough, charge injection, switch off-mode feedthrough, track-mode nonlinearity and so on.

Chapter 3

64-WAY TIME-INTERLEAVED ADC

3.1. Introduction

Digital coherent receivers are becoming increasingly attractive as they can compensate fiber optic impairments in DSP instead of using costly optical signal-processing hardware for long-haul optical communications [7]. Moreover, as the industry moves from 40 Gb/s wavelength division multiplexing transmission system towards 100 Gb/s and beyond system development, the optical dispersion compensators have reached their limits. However, the digital coherent receiver can offer high-accuracy and flexible compensation of fiber channel distortions [41]. Finally, the digital coherent technology enables a variety of spectrally efficient modulation formats such as dual polarization quadrature phase shift keying (DP-QPSK), dual polarization quadrature amplitude modulation (DP-QAM) to cope with the increasingly rapid growth of communications traffic [33].

The digital coherent receiver needs four analog-to-digital converter (ADC) channels since there are two optical polarizations and each needs two ADCs to digitize an I/Q signals. To achieve 100 Gb/s net line rate, a coherent receiver of at least 112 Gb/s is required to allow for forward error correction (FEC) overhead [4]. In the 112 Gb/s DP-QPSK modulation format, a baud rate of 28 Gbaud/s is used since each symbol contains 4 bits. Since commercial systems will also contain polarization-mode dispersion (PMD) and chromatic dispersion (CD) compensation, which necessitates over-sampling, 56 GS/s ADCs are needed for receiving 28 Gbaud/s pulse-amplitude modulation (PAM) signal [36]. Higher order QAM modulation formats allow to increase the data rate without increasing the symbol rate, thus reducing the requirements of ADC sampling rate and bandwidth. However, the necessary ADC resolution increases approximately by 1 bit if the number of constellation points is multiplied by 4 [37].

Table 3.1. Analog-to-digital converter requirements for polarization multiplexed 448 Gb/s transmission [4, 36]

Modulation Format	ADC BW	Baud Rate	Sampling Rate	ENOB
DP-QPSK	112 GHz	112 Gbaud/s	224 GS/s	3.8 b
DP-16QAM	56 GHz	56 Gbaud/s	112 GS/s	4.9 b
DP-64QAM	37 GHz	37 Gbaud/s	74 GS/s	5.7 b
DP-256QAM	28 GHz	28 Gbaud/s	56 GS/s	7 b

Table 3.2. Analog-to-digital converter requirements for polarization multiplexed 112 Gb/s transmission

Modulation Format	ADC BW	Baud Rate	Sampling Rate	ENOB
DP-QPSK	28 GHz	28 Gbaud/s	56 GS/s	3.8 b
DP-16QAM	14 GHz	14 Gbaud/s	28 GS/s	4.9 b
DP-64QAM	9.25 GHz	9.25 Gbaud/s	18.5 GS/s	5.7 b
DP-256QAM	7 GHz	7 Gbaud/s	14 GS/s	7 b

Table 3.3. Analog-to-digital converter requirements for polarization multiplexed 224 Gb/s transmission

Modulation Format	ADC BW	Baud Rate	Sampling Rate	ENOB
DP-QPSK	56 GHz	56 Gbaud/s	112 GS/s	3.8 b
DP-16QAM	28 GHz	28 Gbaud/s	56 GS/s	4.9 b
DP-64QAM	18.5 GHz	18.5 Gbaud/s	37 GS/s	5.7 b
DP-256QAM	14 GHz	14 Gbaud/s	28 GS/s	7 b

To realize a 448 Gb/s coherent receiver, several stringent requirements are imposed on the sampling rate, bandwidth (BW) and effective number of bits (ENOB) of the front-end ADCs as summarized in Table 3.1 [4, 36], where ENOB=(SNDR-1.76dB)/6.02dB. By referring to the ADC requirements of 448 Gb/s coherent receiver in [4] and 100 Gb/s coherent receiver in [37], Table 3.2 and 3.3 summarize the ADC requirements for the 112/224 Gb/s coherent receivers obtained by proportionally adjusting the BW and sampling rate according to the baud rate.

To realize 224 Gb/s coherent receivers, the DP-16QAM modulation format requires 56 GS/s ADCs with 28 GHz BW and at least 4.9 b ENOB. Considering a FIR filter can equalize amplitude degradation caused by analog BW, among published ADCs [32], only one work in 14-nm FinFET technology can meet the ENOB and sampling rate requirements of 224 Gb/s DP-16QAM coherent receivers [23]. Another four works can meet the ENOB, BW and sampling rate requirements of 112 Gb/s DP-16QAM modulation format [5, 12, 24, 26]. This paper presents a 56 GS/s ADC in standard 28 nm CMOS with 5.7 b ENOB up to 17.5 GHz, 5.2 b ENOB up to 27.1 GHz and a BW of 31.5 GHz fulfilling the requirements of 224 Gb/s DP-16QAM.

In this thesis, the implementation and measurement results of a 56 GS/s 8-bit time-interleaved ADC that uses ENOB and BW enhancement techniques [49] is described. As the supply voltages scale down in nanometer technologies, one common problem that plagues ADC design is that there is not enough voltage headroom to fully turn on the NMOS T/H switches, which limits the signal swing and affects the SNR of ADC channels. On the other hand, large signal swing would cause large variations in the on-resistance of the switch, resulting in nonlinearity. To achieve both large signal swing and good linearity, we propose a parametric T/H amplifier technique. This technique can amplify the sampled signalfed into the ADC channels, hence, SNR of the ADC channels limited by comparator noise can be improved. Furthermore, a switched sub-channel buffer is proposed to improve linearity. Such buffer can be disabled in track mode and only enabled to drive the ADC channels in hold mode. Therefore, during tracking, the amplitude and phase errors due to the not-

enough bandwidth of the sub-channel buffer can be avoided. Moreover, to achieve high BW, multiple BW enhancing techniques are utilized. Finally, a foreground all-digital calibration is introduced to correct the intra-channel capacitor mismatch and inter-channel offset, gain, sampling clock skew and bandwidth mismatches. The advantage of such calibration is that all the mismatches are corrected in digital domain and leave fast original architectures intact and compact. For example, the additional tuning circuit of sampling capacitance for bandwidth mismatch calibration in analog domain will degrade the bandwidth.

3.2. ADC ARCHITECTURE

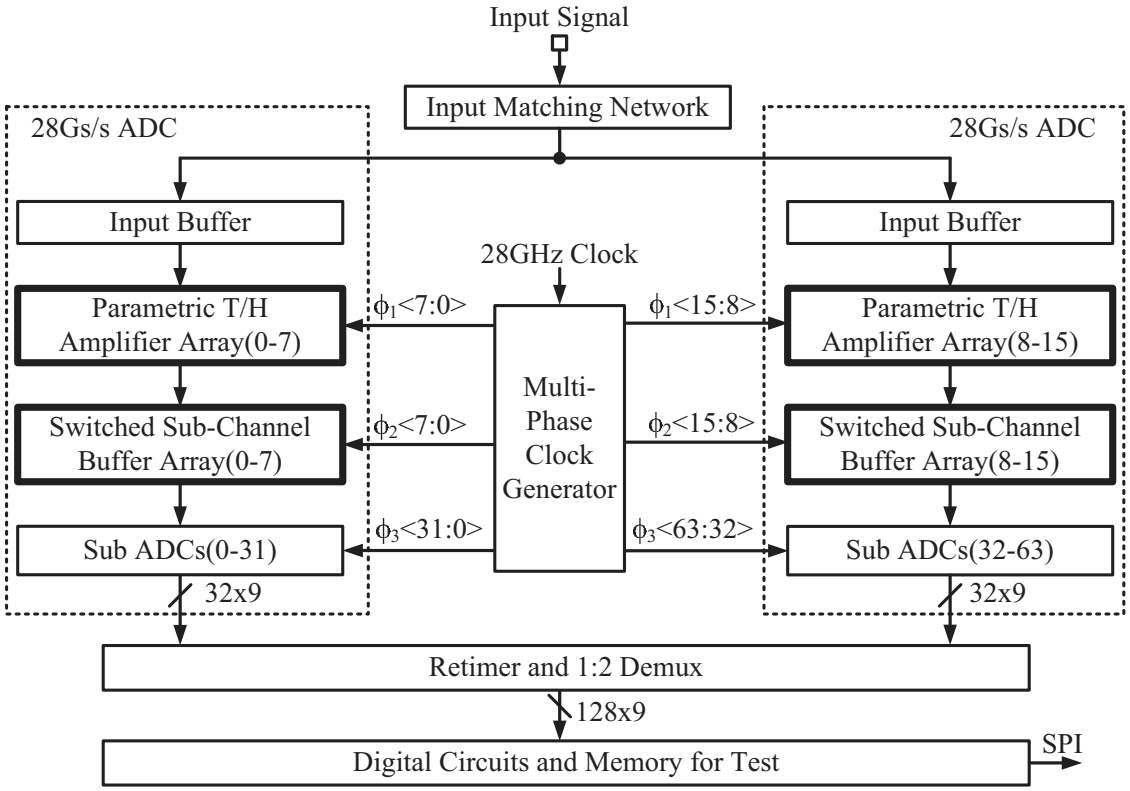

Figure 3.1. Architecture of the 56GS/s ADC.

Figure 3.1 and 3.2 depicts the top-level architecture of the 56 GS/s ADC and its clock timing diagram. The differential input is terminated by an input matching network that feeds into two 28 GS/s ADCs operated in a time-interleaved fashion. Each 28 GS/s ADC

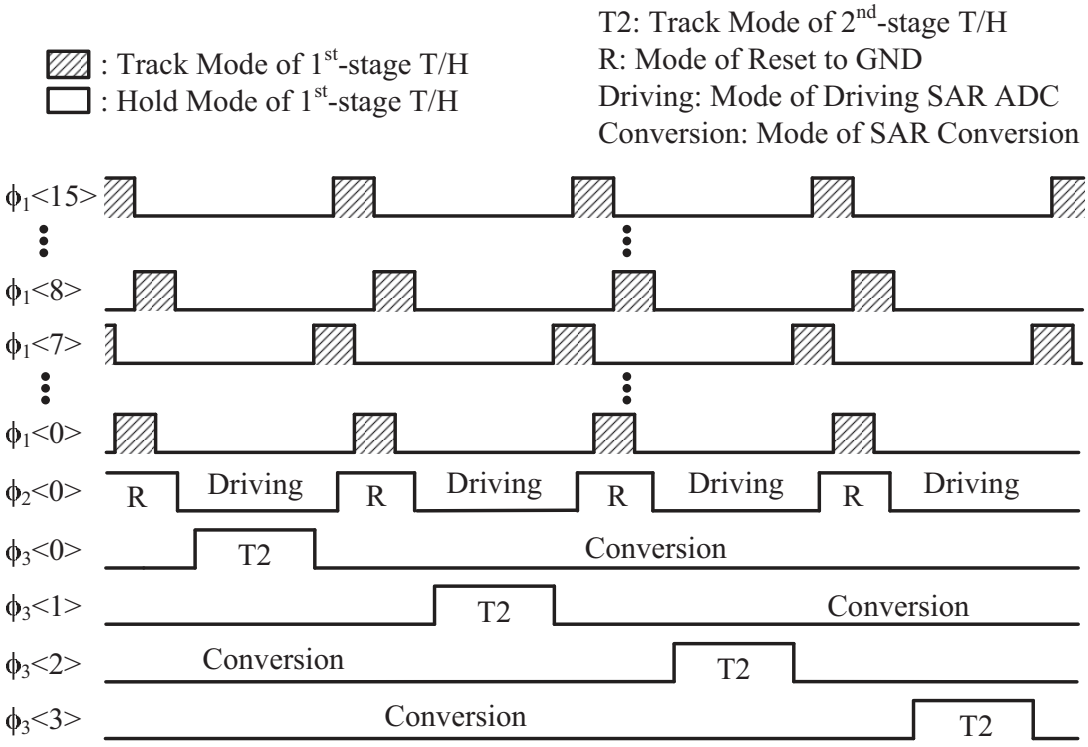

Figure 3.2. clock timing diagram of the 56GS/s ADC.

consists of two time-interleaved stages driven by an identical input buffer and 32 SAR ADC channels. During tracking, the two input buffers protect the input signal of one 28 GS/s ADC from the clock feedthrough coming from the other 28 GS/s ADC. In each 28 GS/s ADC, the first stage is an 8-way time-interleaver, where the input is sampled and held using 8-phase, non-overlapping 3.5 GHz clocks. The second stage is a 4-way time-interleaver, where each of the sampled signals are buffered by sub-channel buffers and then further sampled and held using four-phase 875 MHz clocks and converted to digital values using four instances of the 875 MS/s SAR ADC. The output of the 64 instances of SAR ADCs are retimed to a single 875 MHz clock and demuxed down to 128×9 bit digital data which is captured by the digital circuits and stored by the 16k×9 bit on-chip memory.

Similar to the ADCs with a high degree of interleaving [8,17,19,44], this work leverages a two-level hierarchical sampling architecture. Compared with the ADCs typically consisting of a broadband input buffer that directly drives all of the parallel ADC channels, the hierarchical sampling approach can reduce the number of low-jitter clocks and save the power consumption of distributing the clocks, because only the sampling clocks for the first stage time-interleaver is jitter-critical [11]. In addition, since the sub-channel buffer isolates capacitive loading of the sub-ADC seen at the first stage T/H input, the sum of the capacitances for the T/H switches in track mode can be minimized yet still meet the requirement of kT/C noise to maximize the ADC bandwidth [19].

3.3. Analog ENOB and BW enhancement techniques

The boot-strapped switch, CMOS switch and NMOS switch are the three most commonly used T/H switches. For the boot-strapped switch, the on-resistance R_{on} of the MOS switch can be expressed as

$$R_{\text{on}} = 1/\left[\mu C_{\text{ox}} \frac{W}{L} \left(\frac{C_{\text{boot}} V_{\text{DD}} - C_{\text{G}} V_{\text{IN}}}{C_{\text{boot}} + C_{\text{G}}} - V_{\text{tn}}\right)\right] \tag{3.1}$$

where μ is the electron mobility, C_{ox} is the gate oxide capacitance per unit area, W and L are the device width and effective channel length, respectively, V_{DD} is the supply voltage, V_{IN} is the input voltage, C_G represents the total gate parasitic capacitance of T/H switch, C_{boot} is the capacitance used to establish a constant voltage V_{DD} between the gate and the source terminals of the sampling switch, and V_{tn} is the threshold voltage. To achieve good linearity, C_{boot} should be much larger than C_G to make the impact of the input voltage V_{IN} on R_{on} negligible. The signal swing is no longer limited by the low supply voltage in the bootstrap T/H circuit voltage. However, compared with other T/H switches, the boot-strapped switches have a higher capacitance attached to one side of the switch because of the circuitry connected for a constant gate-to-source voltage. In addition, the bootstrap T/H circuit has many internal nodes drawing charges from the input node, which slows down the boot-strap response time [56].

Since the NMOS device exhibits an on-resistance that decreases as the input voltage decreases and the PMOS device exhibits an on-resistance that decreases as the input voltage increases, the CMOS switches can be employed to linearize the switch conductance. However, the threshold voltages do not scale accordingly as the supply voltage scales in the advanced technologies. A problem arises: because V_{DD} is comparable to the sum of the two threshold voltages of NMOS and PMOS devices, there is a substantial drop in the conductance when V_{IN} approaches $V_{DD}/2$ [1]. The analog input bandwidth of the front-end T/H circuits in high-speed ADCs for optical communications is very critical, because the sampling capacitor has to follow several Giga baud/s or even tens of Giga baud/s PAM input signals for the 100 Gb/ and beyond transmission. The analog bandwidth of T/H with NMOS switch depends on the sampling capacitance and the on-resistance of the switch. The total parasitic capacitance C_s and on-resistance R_{on} are linked with the technology transition frequency f_T [22]. Thus, the T/H with NMOS switch can achieve a very high bandwidth, which is limited by f_T. In standard CMOS technologies, the threshold voltage of NMOS transistors does not scale with the supply voltage, and it becomes a large portion of the supply voltage leading to the problems that when the input voltage is high, $V_{GS,min}$ is too low to fully turn on the switch

to obtain a small on-resistance to track the input. When the input voltage is low, the on-resistance is small. Owing to the limited gate overdrive voltage and large signal swing, the large variation of on-resistance causes distortions. As a result, the available signal swing is limited for the following ADC channels. To overcome this problem, the ADC in [44] uses the thick oxide 2.5 V NMOS device as the T/H switch to enable a higher V_{DD} than the supply voltage of thin oxide device but at the sacrifice of lowing the switching speed. The ADC in [7] employs an active amplifier to amplify the sampled signal and improve the signal-to-noise ratio (SNR) of the following ADC channels.

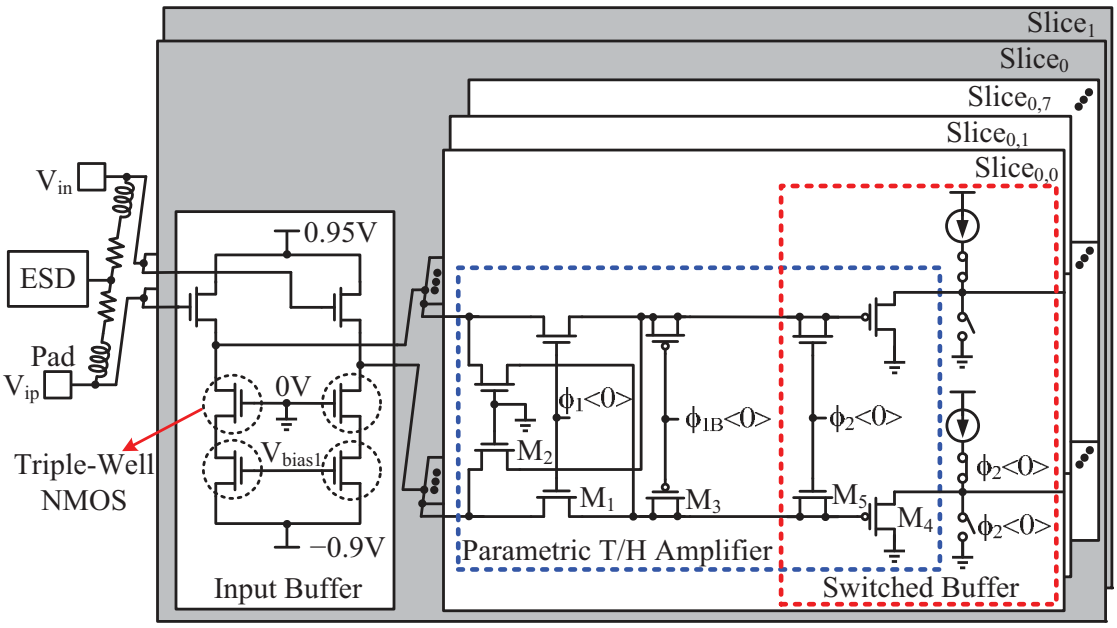

Figure 3.3. Schematic details of the front-end circuits.

In this work, a parametric T/H amplifier is proposed that can amplify the sampled signal and improve the SNR of the following ADC channels. A parametric amplifier is a circuit in which the amplification is achieved by the use of variable (time-dependent) parameters or circuit elements [40]. The gain of the parametric T/H amplifier stems from varying the passive capacitance without using active transistors, thus presenting much lower noise than using active amplifiers. Figure 3.3 and Table 3.4 show the schematic details of the T/H amplifier and the working regions of its transistors. The total sampling capacitance

Table 3.4. Working regions of parametric T/H amplifier transistors

C_S (Device Width)	Track		Hold	
	C_S (fF)	Region	C_S (fF)	Region
$C_{d,M1}$(13.5 μm)	11.1	Linear	8.5	Cutoff
$C_{d,M2}$(13.5 μm)	8.5	Cutoff	8.5	Cutoff
$2C_{d,M3}$(14 μm)	10.5	Weak-Inversion	9.3	Cutoff
$C_{g,M4}$(62 μm)	34.6	Cutoff	23.8	Saturation
$2C_{d,M5}$(9 μm)	14.0	Linear	9.2	Cutoff
$C_{MetalRouting}$	22.1	-	22.1	-
Total C_S (fF)	100.8		81.4	
Power Gain	1.9 dB			

of the T/H circuit comprises the parasitic capacitances of M_1-M_5 and the metal routing. The total sampling capacitance decreases when the T/H circuit goes from track mode to hold mode, while the total charge on the sampling capacitor remains constant, resulting in the corresponding voltage gain. M_1 is the sampling switch; M_2, which is constantly off, is for the signal feedthrough compensation; M_3 is for clock feedthrough compensation. M_4 is the source-follower buffer driving the sub ADC channels; and M_5 is added to maintain a constant common-mode voltage level for M_4. Except for M_2 and the metal routing, which maintain the same parasitic capacitance, all other transistors (M_1, M_3, M_4 and M_5) present a smaller parasitic capacitance in hold mode than in track mode. Specifically, M_3 employs a PMOS transistor because the PMOS capacitance decreases when transiting from the weak inversion region in track mode to the cut-off region in hold mode. Benefiting from the 24 % increase in output voltage (1.9 dB power gain) of the parametric T/H amplifier, the improved SNDR, together with the further SNDR improvement coming from the switched buffer, is significant, considering that there is only a small difference in the ENOB between DP-16QAM and DP-64QAM (4.9 b vs. 5.7 b, equivalent to a 4.8 dB SNDR improvement).

For the design consideration of NMOS switch M_1, the low threshold voltage (LVT) device has a desirable low on-resistance, but not high enough off-resistance, resulting in charge leakage from the sampling capacitor and distortions. High threshold voltage (HVT) device has a favorable high off-resistance presenting good isolation performance in hold mode. However, compared with LVT and regular threshold voltage (RVT) devices, in track mode, the HVT device has larger on-resistance and larger variation of signal dependent on-resistance, which degrades analog input bandwidth and causes distortions. Weighing the tradeoff between on-resistance in track mode and off-resistance in hold, RVT device is employed as the T/H switch.

When a NMOS switch transitions from on to off, the channel charge injection and clock feedthrough introduce an error in the voltage sampled on the sampling capacitor C_S, as shown in Figure 3.4 and 3.5. For a slow turn-off, the channel charge is absorbed by the input source. For a fast turn-off, a fraction of the channel charge pQ_{CH} is injected to the sampling capacitor C_S, where p is the fraction factor dependent on the impedance seen at each terminal of NMOS switch to ground and transition time. The following expression for the voltage error ΔV_{chinj} caused by charge injection can be found [42]:

$$\Delta V_{chinj} = \begin{cases} 0, \text{slow off} \\ -p\dfrac{C_{ox}WL(V_{DD} - V_{tn} - V_{IN})}{C_{GS} + C_S}, \text{fast off.} \end{cases} \tag{3.2}$$

For a fast turn-off switch, due to the clock feed through, the charge coupled to the sampling node is $V_{DD}C_{GD}$. For a slow turn-off switch, the sampling moment is at the time when the voltage of clock ϕ equals $V_{IN} + V_{tn}$. Thus the charge coupled to the sampling node is $(V_{IN} + V_{tn})C_{GD}$. Due to the clock feed through, the voltage error ΔV_{fth} can be written as

$$\Delta V_{fth} = \begin{cases} -\dfrac{C_{GD}(V_{IN} + V_{tn})}{C_{GS} + C_S} & \text{, slow off} \\ -\dfrac{V_{GD}V_{DD}}{C_{GS} + C_S} & \text{, fast off.} \end{cases} \tag{3.3}$$

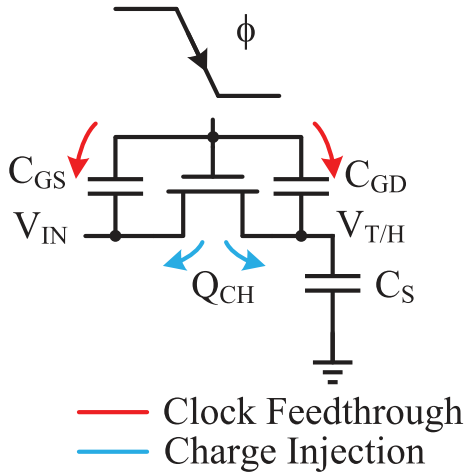

Figure 3.4. Clock feedthrough and charge injection in a T/H circuit with NMOS switch.

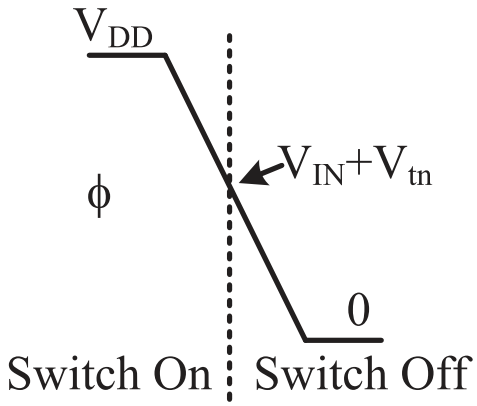

Figure 3.5. Clock waveform showing the sampling moment.

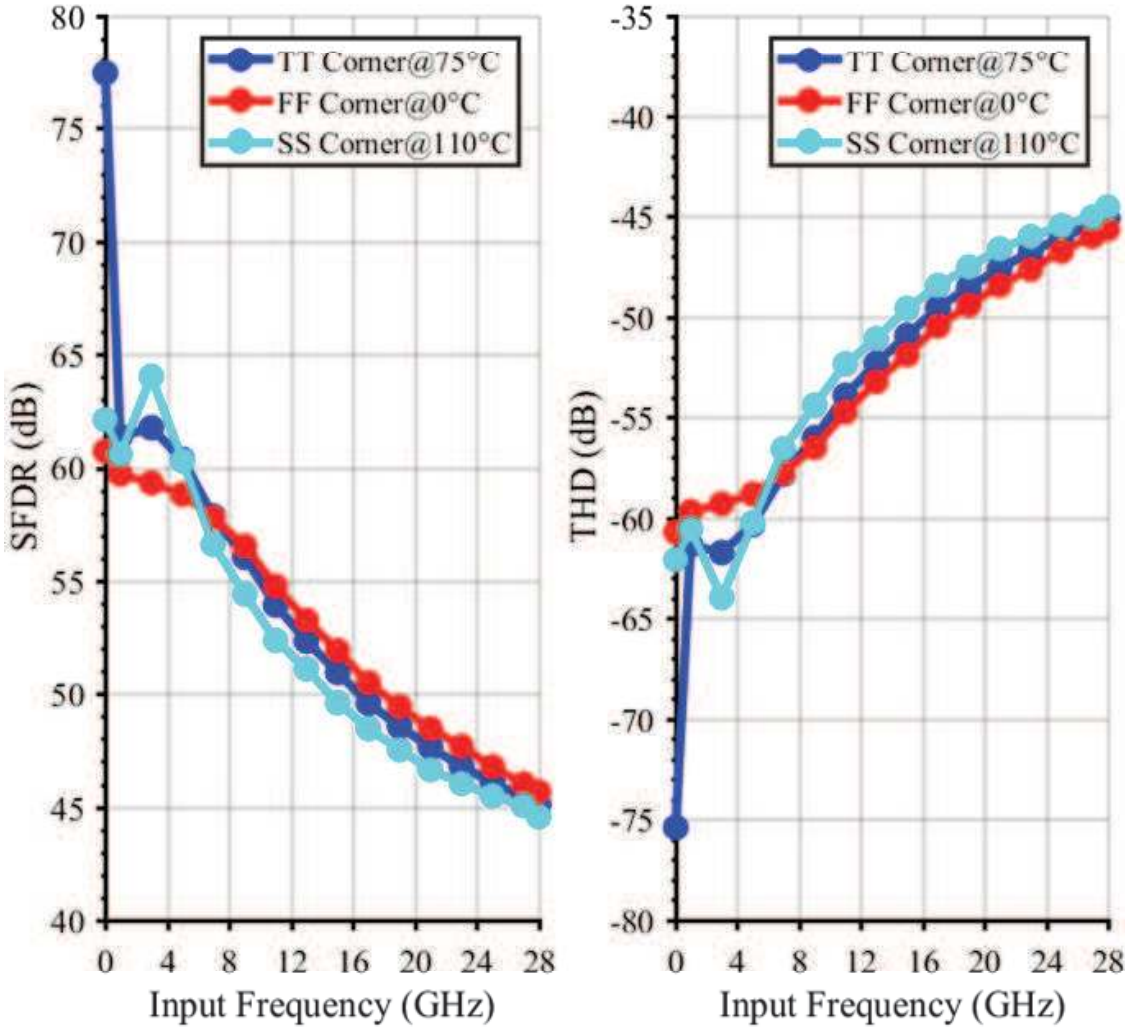

Figure 3.6. Simulated SFDR and THD vs. input frequency for the parametric T/H amplifier with 500 mV_{pp} across different corners.

A well known method to compensate the charge injection and clock feed through of the NMOS switch is to add a half sized dummy switch, driven by the inversed clock ϕ_B to the circuit. But in our T/H circuit, a PMOS device is used to compensate for the clock feed through. One concern is whether the voltage errors caused by the imperfect compensation of the charge injection and clock feedthrough would degrade the ADC performance. By neglecting the body effect and assuming V_{tn} constant in (3.2) and (3.3). Therefore the $\Delta V_{chinj} + \Delta V_{fth}$ manifests itself as a constant offset error and a gain error in the input/output characteristic. Since the constant offset does not affect the ADC linearity, it does not need calibration for most applications. In addition, the input gain error imposes no real problem to the overall linearity of the converter [31]. The purpose of the M_3 in the T/H circuit is to compensate the undesired drop of the sampled voltage caused by clock feed through of M_1 and keeps the PN junction of drain and bulk of M_1 inversely biased. Otherwise the sampled charges on C_S would leak away.

Other concerns with the parametric T/H amplifier are the linearity degradation caused by the body effect of the switch and the signal dependent parasitic capacitance. Fig. 3.6 shows the simulated plot of SFDR and THD vs. input frequency for the parametric T/H amplifier with a input swing of 500 mV_{pp}. The simulation result shows that the SFDR >44.6 dB and THD <44.56 dB up to 28 GHz. The distortions including the nonlinearity contributed by the signal dependent on-resistance and parasitic sampling capacitance, shows the performance of the parametric T/H amplifier is good enough for an ADC with 8 bit resolution. The nonlinearity is dominated by the 3rd-order harmonic distortion.

Sub-channel buffers are essential components in a hierarchical sampling architecture to enable the sampled signal having the ability to drive the following ADC channels. Figure 3.7 shows the schematic of a simplified 2-stage T/H. In a conventional sub-channel buffer, the output V_{buf} keeps tracking the input signal $V_{T/H}$ in both track mode and hold mode. However, in a 112/224 Gb/s coherent receiver, where the input frequency is up to tens of GHz, it is nearly impossible for a sub-channel buffer to achieve enough bandwidth to track the input signal. This creates a problem in a conventional continuous working sub-channel

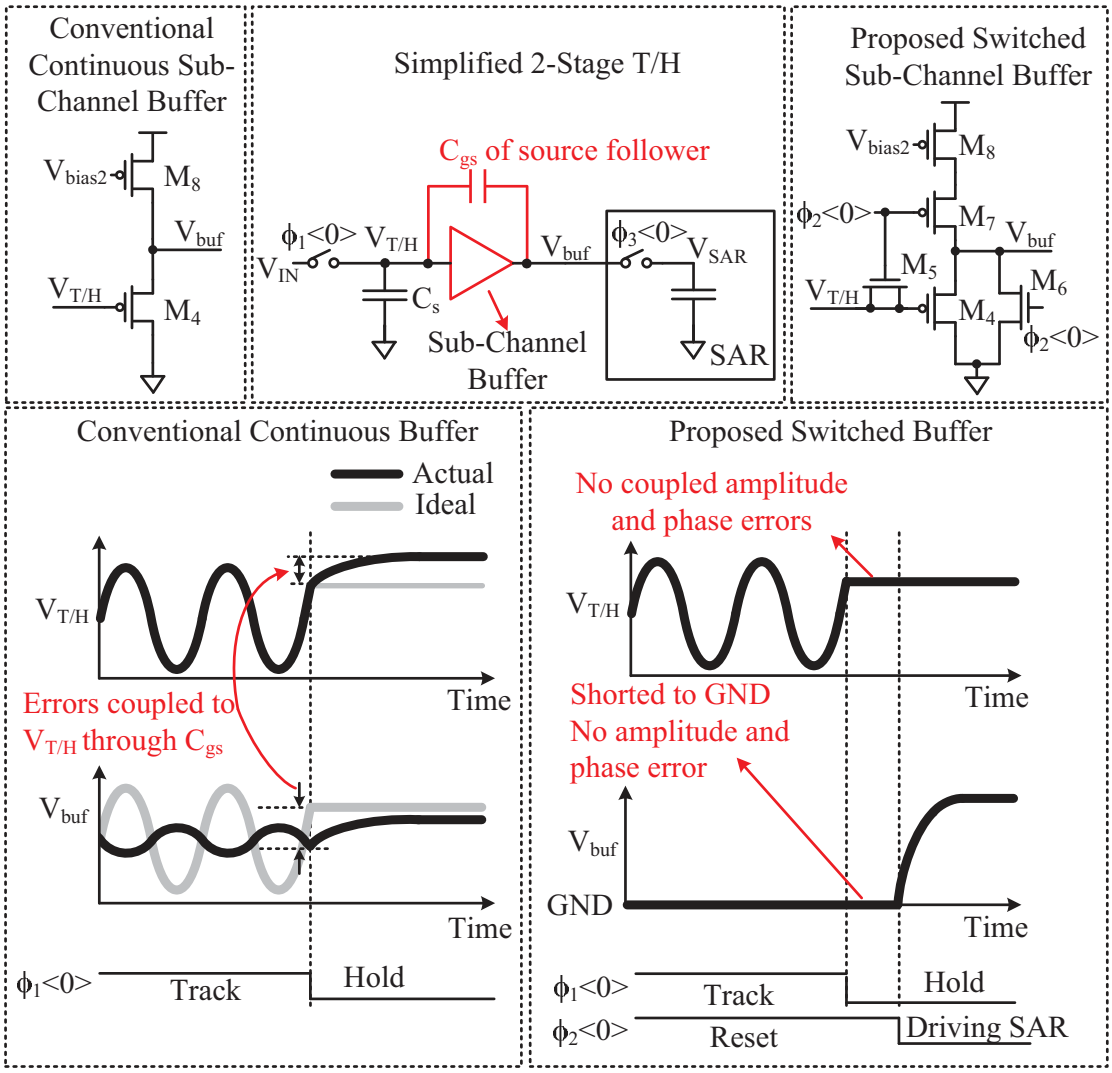

Figure 3.7. Schematic of a simplified 2-stage T/H and comparison of a conventional continuous working sub-channel buffer and a switched sub-channel buffer.

buffer, as shown in the $V_{\rm buf}$ and $V_{\rm T/H}$ waveforms of a conventional sub-channel buffer in Figure 3.7 during tracking, the buffer output $V_{\rm buf}$ cannot follow the input signal $V_{\rm T/H}$, which creates amplitude and phase errors. Let $v_{\rm T/H}$ and $v_{\rm buf}$ be the small signal input and output of the conventional source-follower buffer. Assuming the $g_{\rm m}r_{\rm o,M8}>>1$, the transfer function of the source follower is given by [18]

$$\frac{v_{\rm buf}(s)}{v_{\rm T/H}(s)} = \left(1 + s\frac{C_{\rm gs}}{g_{\rm m}}\right) / \left(1 + s\frac{C_{\rm gs} + C_{\rm L}}{g_{\rm m}}\right) \tag{3.4}$$

where $r_{\rm o,M8}$ is the output resistance of $\rm M_8$, $C_{\rm gs}$ is the gate-source capacitance of $\rm M_4$, and $C_{\rm L}$ is the total load capacitance of source follower including the bulk-source capacitance of $\rm M_4$ and bulk-drain capacitance of $\rm M_8$. Because $v_{\rm buf}$ cannot follow the input signal $v_{\rm T/H}$, the transconductance $g_{\rm m}$ of $\rm M_4$ is signal dependent at high input frequency. Therefore, the obtained $v_{\rm buf}$ from the transfer function (3.4) contains nonlinear distortions. Let $v_{\rm T/H0}$ and $v_{\rm buf0}$ be the voltage of $v_{\rm T/H}(t)$ and $v_{\rm buf}(t)$ at the sampling moment. At the sampling moment, the total charge Q stored on the sampling node can be written as

$$Q = \left(v_{\rm T/H0} + V_0\right) C_{\rm S} + \left(V_{\rm gs0} + v_{\rm T/H0} - v_{\rm buf0}\right) C_{\rm gs} \tag{3.5}$$

where V_0 and $V_{\rm gs0}$ are the DC voltages of $V_{\rm T/H}$ and $V_{\rm gs}$ of $\rm M_4$, respectively, $C_{\rm S}$ is the sampling capacitance and $v_{\rm buf0}$ contains harmonic distortions of input signal.

After tracking, the buffer output $V_{\rm buf}$ would try to settle to its final value where $V_{\rm T/H}V_{\rm buf} = V_{\rm gs0}$. Let $V_{\rm T/H1}$ and $V_{\rm buf1}$ be the final value of $V_{\rm T/H}$ and $V_{\rm buf}$ after the settling process, therefore the total charge Q stored on the sampling node can be expressed as

$$Q = V_{\rm T/H1}C_{\rm S} + V_{\rm gs0}C_{\rm gs}. \tag{3.6}$$

Since the total charge Q stored on the sampling node remains constant, the final $V_{\mathrm{T/H}}$ and V_{buf} after the charge redistribution can be calculated from (3.5)(3.6) and written as

$$V_{\mathrm{T/H1}} = v_{\mathrm{T/H0}} + V_0 + \frac{C_{\mathrm{gs}}}{C_{\mathrm{S}}}(v_{\mathrm{T/H0}} - v_{\mathrm{buf0}}) \tag{3.7}$$

$$V_{\mathrm{buf1}} = v_{\mathrm{T/H0}} + V_0 - V_{\mathrm{gs0}} + \frac{C_{\mathrm{gs}}}{C_{\mathrm{S}}}(v_{\mathrm{T/H0}} - v_{\mathrm{buf0}}) \tag{3.8}$$

Observing from equations (3.7)(3.8), during the settling process, charge redistribution between the sampling capacitor C_{S} and C_{gs} of the source follower causes distortion in $V_{\mathrm{T/H}}$ and the buffer output V_{buf} [29]. One way to reduce the harmonic distortions introduced by v_{buf0} is to make $C_{\mathrm{S}}>>C_{\mathrm{gs}}$, however the ADC analog input bandwidth will be greatly reduced. Another way is to minimize $v_{\mathrm{T/H0}} - v_{\mathrm{buf0}}$ by having enough bandwidth for the sub-channel buffer, however a large number of power will be dissipated and a large size of source follower will have a larger C_{gd}, which will increase the total sampling capacitance and reduce the ADC analog input bandwidth. Though the analysis is based on a conventional continuous working source follower based sub-channel buffer, the above analysis can also be applied to other kind of continuous working sub-channel buffers.

A switched buffer is proposed in this work to tackle the problem of harmonic distortions. The conceptual idea is that V_{buf} is reset to GND during tracking and is only enabled to drive the SAR ADC in hold mode. As shown in the proposed switched sub-channel buffer in Fig. 3.7, in track mode, the buffer is shut down by M_7, cutting off the circuit DC current, and M_6 shorts the outputs of the buffer to GND. At the sampling moment, the total charge Q stored on the sampling node can be written as

$$Q = (v_{\mathrm{T/H0}} + V_0)(C_{\mathrm{S}} + C_{\mathrm{gs}}) \tag{3.9}$$

where $v_{\mathrm{T/H0}}$, V_0, C_{S} and C_{gs} are defined the same as in (3.5). C_{S} includes all parasitic capacitance on the gate of M_4 except C_{gs}. In hold mode, M_7 is turned-on to enable the current of M_8 to flow into M_4. M_6 is turned-off to enable the outputs of the buffer driving

the SAR ADC. In hold mode, the equation for the total charge Q stored on the sampling node is the same as (3.6). The final $V_{\mathrm{T/H1}}$ and V_{buf1} after the charge redistribution can be calculated from (3.6)(3.9) and written as

$$V_{\mathrm{T/H1}} = v_{\mathrm{T/H0}} + V_0 + \frac{C_{\mathrm{gs}}}{C_{\mathrm{S}}}(v_{\mathrm{T/H0}} + V_0 - V_{\mathrm{gs0}}) \tag{3.10}$$

$$V_{\mathrm{buf1}} = v_{\mathrm{T/H0}} + V_0 - V_{\mathrm{gs0}} + \frac{C_{\mathrm{gs}}}{C_{\mathrm{S}}}(v_{\mathrm{T/H0}} + V_0 - V_{\mathrm{gs0}}) \tag{3.11}$$

When entering hold mode, the signal V_{buf} goes from GND to the driving voltage. This increase in the voltage would be coupled to the node of the sampling capacitor, increasing the common-mode voltage of the buffer output closer to the power supply as shown in the last term of (3.10). To mitigate this, M5 is added to cancel the increase in the common-mode voltage using its falling-edge clock feedthrough. Compared with the conventional continuous working sub-channel buffer, (3.10)(3.11) demonstrates that there is no harmonic distortions introduced by the proposed switched sub-channel buffer.

Multiple BW enhancing techniques are employed in the front-end circuits, including using parasitic capacitance for sampling and using inductive peaking at the differential input to compensate for the input parasitic capacitance. Moreover, the input buffers, having dual supply voltages +0.95 V/0.9 V, are employed to drive the load presented by the following T/H circuits. The outputs of the input buffers are biased at approximately 0.1 V to make the on-resistance of the T/H circuits small. Additionally, ESD-diodes are added at the common-mode node instead of directly connected to the differential input nodes to avoid additional input parasitic capacitance.

Negative power supply is required by the input buffer for the current sink. Triple-well NMOS transistors are used with their body nodes isolated from the substrate and connected to the negative supply voltage. A cross-section view of the triple-well NMOS is shown in Figure 3.8. The NMOS transistors of the input buffer are stacking to divide the voltage across several devices in series known as the totem-pole HV protection technique [3].

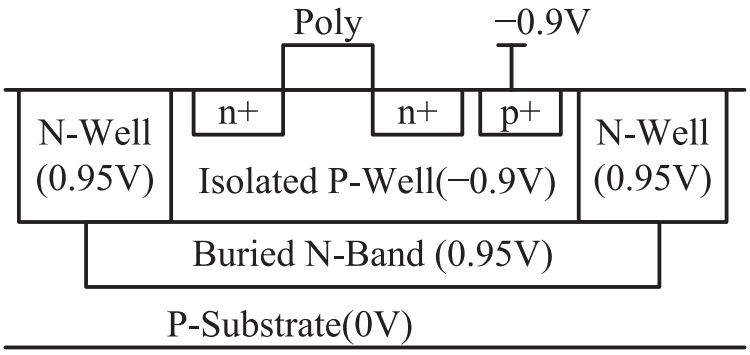

Figure 3.8. A cross-section view of triple-well NMOS device.

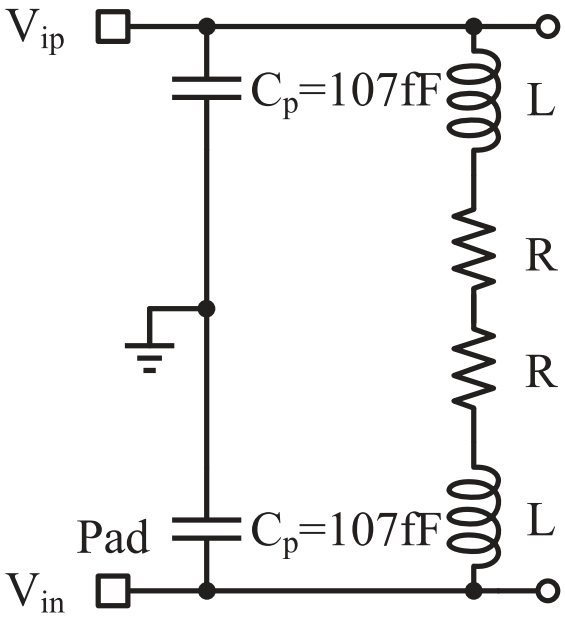

Figure 3.9. Input matching network model.

Peaking techniques are widely used in enhancing the bandwidth of broadband circuits and they can be grouped into different categories, such as shunt peaking, series peaking, shunt-series peaking , T-coil peaking and bridged T-coil peaking [45]. For simplicity, this work employs shunt peaking to deal with parasitic capacitances at the ADC input nodes similar to [50]. For high-speed ADCs, the input is often terminated with an input matching network to reduce signal reflections. Figure 3.9 shows an input matching network model of the ADC. The input pad and input buffers contribute to 107 fF parasitic capacitance at the input node. The reflection coefficient Γ_{L}(which is the same as S11) can be given by [27]

$$\Gamma_{\mathrm{L}} = \frac{Z_{\mathrm{L}} - Z_0}{Z_{\mathrm{L}} + Z_0} \tag{3.12}$$

where Z_0=50Ω is the characteristic impedance of the transmission line and Z_{L} is the load impedance.

$$Z_{\mathrm{L}} = \frac{sL + R}{sC_{\mathrm{p}}} \tag{3.13}$$

The design is targeting the S11 at < -15 dB at 24 GHz and < -10 dB at 32 GHz. By

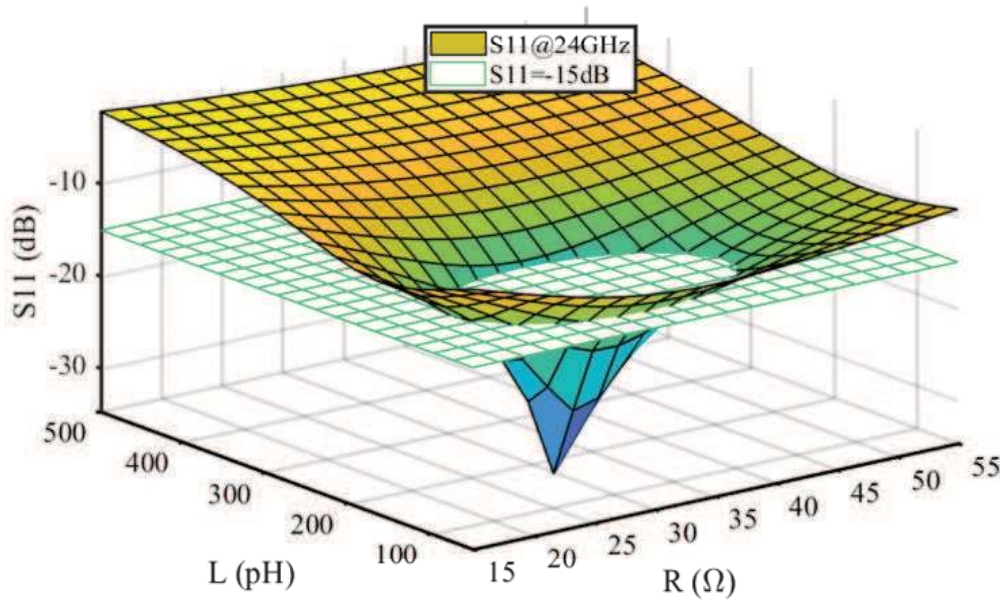

Figure 3.10. S11 of the input matching network model by sweeping L and R at 24 GHz.

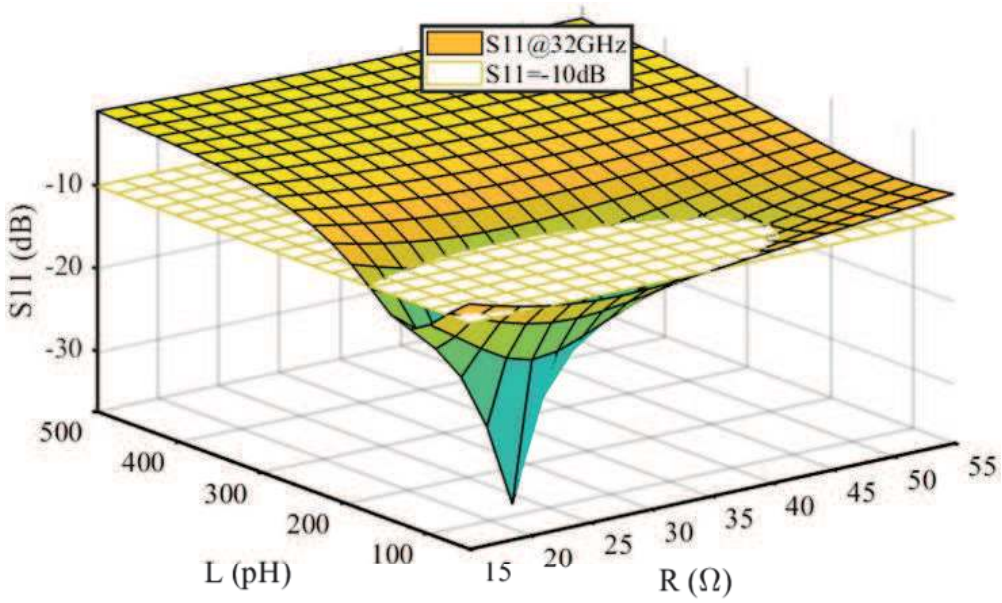

Figure 3.11. S11 of the input matching network model by sweeping L and R at 32 GHz.

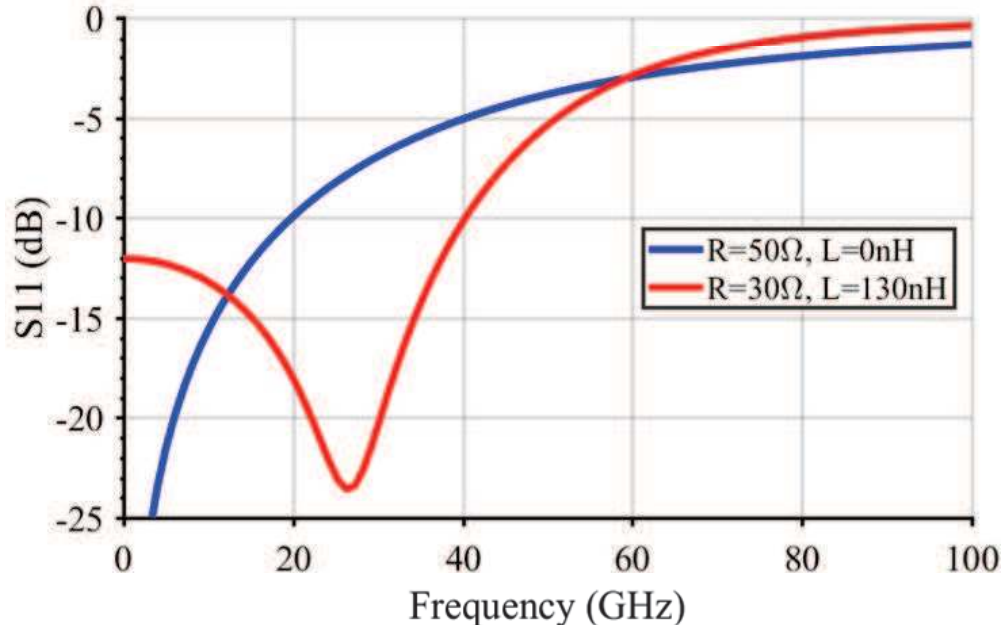

Figure 3.12. S11 vs. input frequency of the input matching network model when $R = 50\ \Omega$, $L = 0$ nH and $R = 30\ \Omega$, $L = 130$ nH.

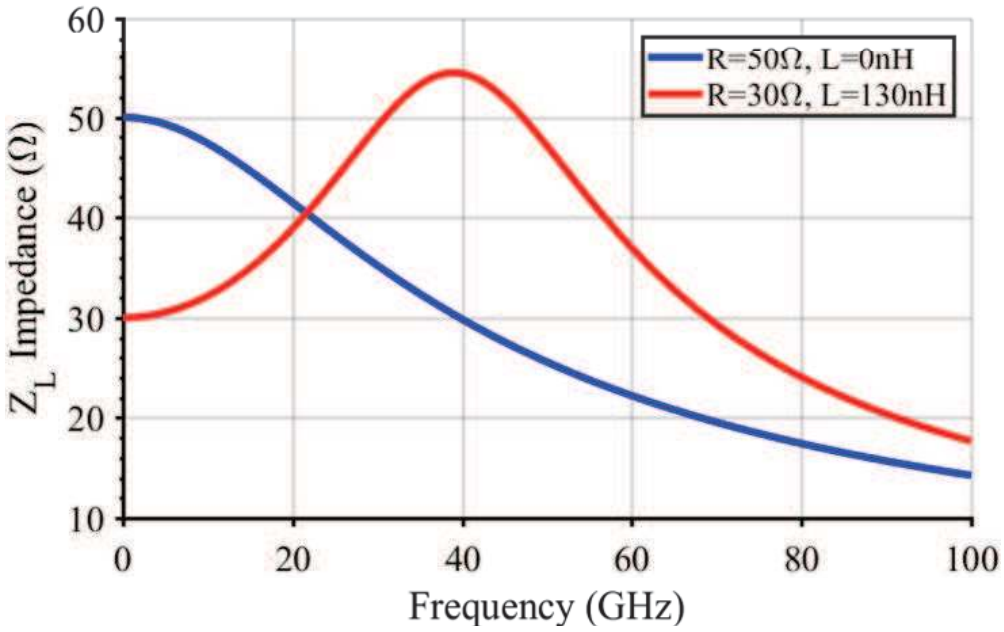

Figure 3.13. Z_{L} impedance vs. input frequency of the input matching network model when $R = 50\ \Omega$, $L = 0$ nH and $R = 30\ \Omega$, $L = 130$ nH.

sweeping the L and R at 24 GHz and 32 GHz, the obtained S11 plot are shown in Figure 3.10 and 3.11. At 24 GHz, a minimum S11 is achieved when $R = 30\ \Omega$ and $L = 160$ nH. At 32 GHz, a minimum S11 is achieved when $R = 25\ \Omega$ and $L = 130$ nH. To achieve a small S11 at both the 24 GHz and 32 GHz, we chose $R = 30\ \Omega$ and $L = 130$ nH. Such values can also ensure the S11 robust under certain range of the R and L process variations. Figure 3.12 and 3.13 shows the plot of S11 and Z_{L} vs. input frequency for $R = 30\ \Omega$, $L = 130$ nH and $R = 50\ \Omega$, $L = 0$ nH. We can intuitively see the S11 performance at the low frequencies is sacrificed yet still < -10 dB for the S11 improvement at high frequencies, and the Z_{L} impedance is approaching $50\ \Omega$ as the input frequency is close to 32 GHz.

To minimize the inter-channel mismatch, the layout of the 3.5 GS/s T/H is symmetric and instantiated for all the T/H circuits; Moreover, balanced paths are used to distribute the signal to the T/H. For the consideration of the crosstalk shielding, the following rules are followed in the layout design: First, noise sensitive circuits are placed in the triple N-well to isolate the substrate noise; Second, power mesh is inserted between the high speed signal

routing on top-level metals and the transistor circuits on bottom-level substrate. Therefore, th e signal coupling is isolated and the IR drop of the power supply is reduced; Third, the power or ground routing is added around the signal and clock routing to avoid the signal cross-talk on the same metal layer; Finally, a high-resistance substrate ring is place around the ADC to isolate the substrate noise.

3.4. Clock Generation Circuit

One essential part of the ADC is the 14 GHz clock generation. The 4-phase 14 GHz sampling clocks are derived from a 28 GHz clock by dividing by 2 using CML circuit and converted to CMOS levels. Because the input signal is sampled by the clock edge of the 4-phase 14 GHz clocks, their jitter performance and timing skew play a key role in the overall ADC performance. The timing-skew error is calibrated in the CML clock buffers. The 4-phase 14 GHz clocks also feed to the sub-clock generation block to generate the 3.5 GHz clocks and 0.875 GHz clocks.

In the 14 GHz clock generation block of Figure 3.14, the 28 GHz differential sine-wave clock signals feed to the clock generation circuit through DC blocker. By dividing the 28 GHz CML clock by 2, the 4-phase 14 GHz CML clocks $CML < 3{:}0 >$ are obtained. The following CML clock buffers drive the CML-to-CMOS conversion circuit and also isolate the output (4-phase 14 GHz clocks) from the frequency divider, so that the delay of each 14 GHz clock can be tuned separately. The digitally controlled capacitor banks are used at the output of 14 GHz CML clock buffers for the calibration of clock timing skew errors. The delay of each 14 GHz clock is fine tuned with steps of resolution of 25 fs steps. The tuning range of 14 GHz clock delay is about 1.6 ps, which can cover the timing skew errors caused by PVT mismatches. The differential amplifiers and 3-stage inverters convert the CML differential signal to CMOS signals. To eliminate the error caused by the input offset of the differential amplifiers, the output of the differential amplifier is ac-coupled to a self-biased inverter.

Figure 3.15 shows the schematic details of the CML clock buffer with digital controled capacitor bank. The schematic of the 28 GHz CML clock divider is shown in Figure 3.16.

The sampling clock CKTH< 15:0 > is generated from the 50% duty cycle 14 GHz clock CK14G<3:0> and the 25% duty cycle 3.5 GHz CK3p5G< 15:0 >, as shown in Figure 3.17. Figure 3.18 shows the schematic to generate the 25% duty cycle 3.5 GHz CK3p5G< 15:0 >. To specify the sequence of the generated clock, a reset signal $RST < 0 >$ is used. TSPC (True Single Phase Clocking) flip flop circuit is used in the clock divider circuit of Figure 3.18, which is shown in Figure 3.19.

3.5. Error Model for Time-Interleaved ADC

The aim of this section is to analyze the nonidealities which affect the performance of the time-interleaved ADC and create a discrete-time behavioral model of the ADC with mismatch errors that can be simulated at fast speed in the MATLAB SIMULINK environment. Afterwards, the obtained SIMULINK results with mismatch errors can be further used to verify the effectiveness of a calibration method, which is introduced in the following sections. The most significant nonidealities are modeled and building blocks for modeling intra-channel capacitor mismatch, inter-channel offset, gain, sampling clock skew and bandwidth mismatches, sampling jitter and kT/C noise are proposed.

Figure 3.20 shows the block diagram of an 8-bit SAR ADC j-th channel with 1 bit for redundancy in [54]. At the beginning of each conversion cycle, the 9 raw bits $b_{\mathrm{i,j}}[n]$ of the n-th conversion result are all set to zero, where i is from 8 to 0 denoting the conversion phase from MSB to LSB. The successive approximation (SA) loop consisting of the comparator, SAR logic and capacitive DAC keep subtracting the combining weights from the input signal and obtains a residue voltage $V_{\mathrm{RES,i,j}}[n]$ as the comparator input. For each bit conversion, the expressions of $V_{\mathrm{RES,i,j}}[n]$ and $b_{i,j}[n]$ are given by

$$V_{\mathrm{RES,i,j}}[n] = V_{\mathrm{RES,i+1,j}}[n] - b_{\mathrm{i,j}}[n](1+\epsilon_{\mathrm{i,j}})w_{\mathrm{i}}\Delta, \tag{3.14}$$

$$b_{\mathrm{i,j}}[n] = \begin{cases} -1, V_{\mathrm{RES,i+1,j}}[n] \leq 0 \\ 1, V_{\mathrm{RES,i+1,j}}[n] > 0. \end{cases} \tag{3.15}$$

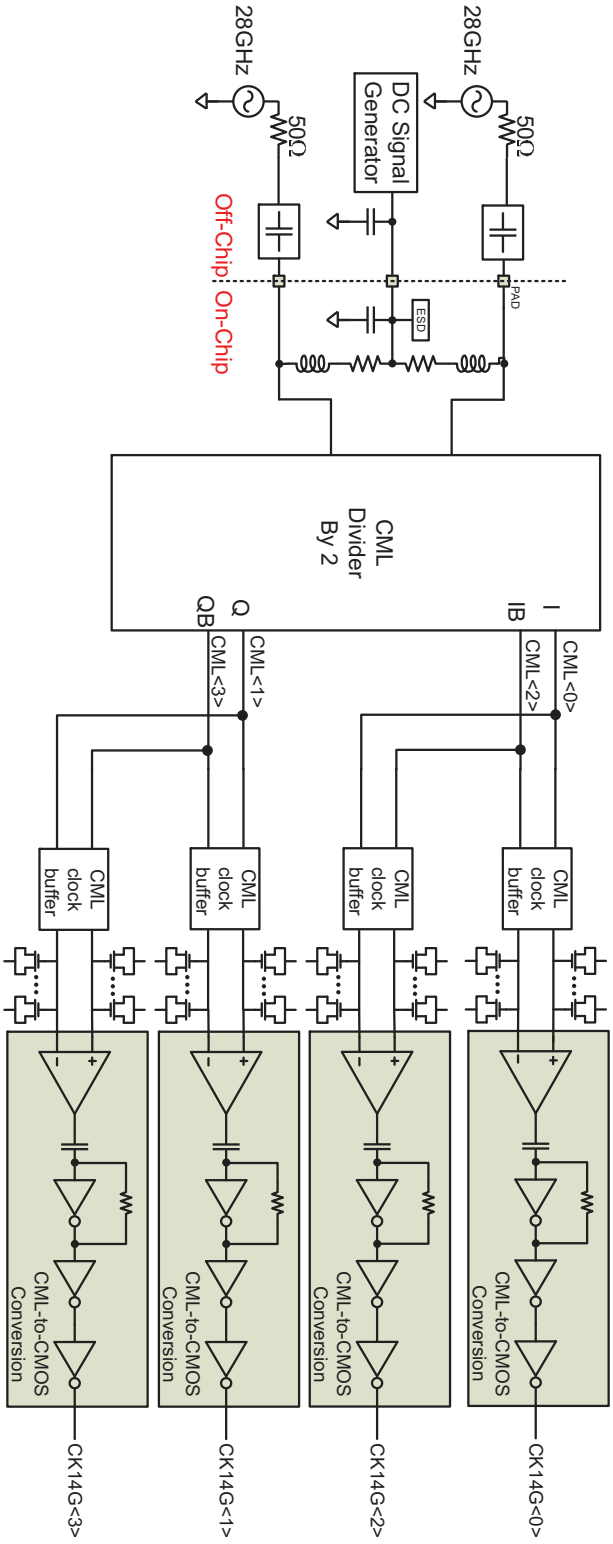

Figure 3.14. Block diagram of 14 GHz clock generation.

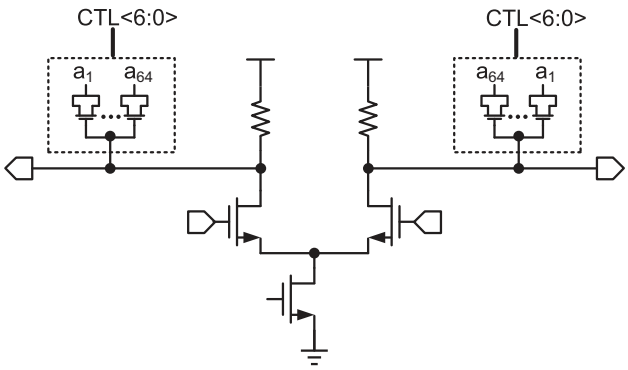

Figure 3.15. Schematic details of the CML clock buffer with digital controled capacitor bank.

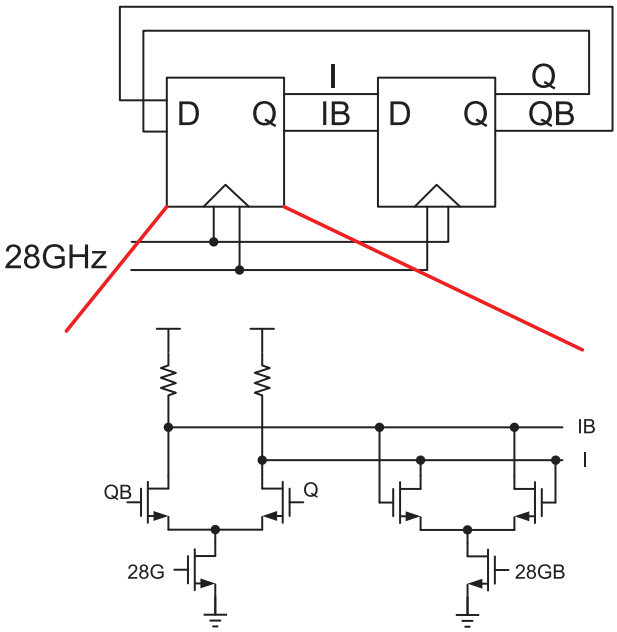

Figure 3.16. Schematic of 28 GHz CML clock divider.

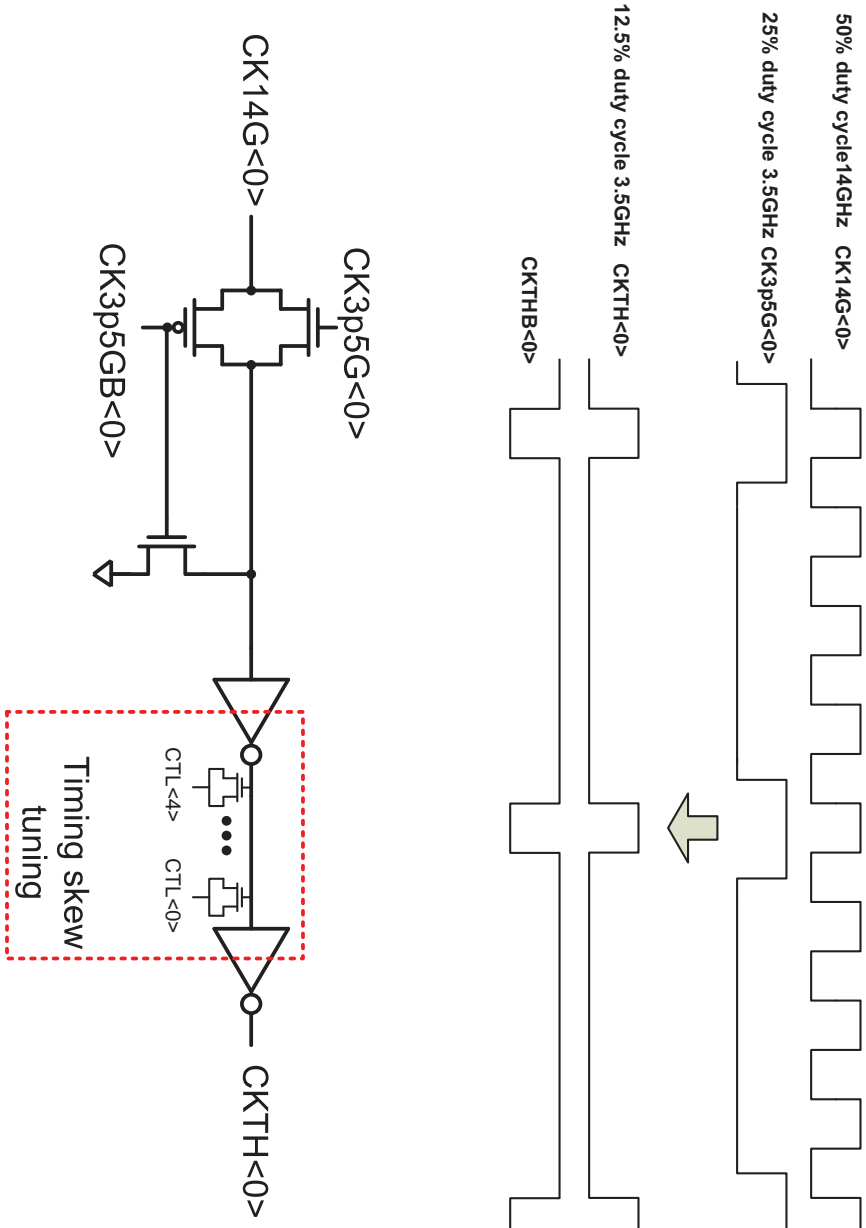

Figure 3.17. Schematic to generate the sampling clock.

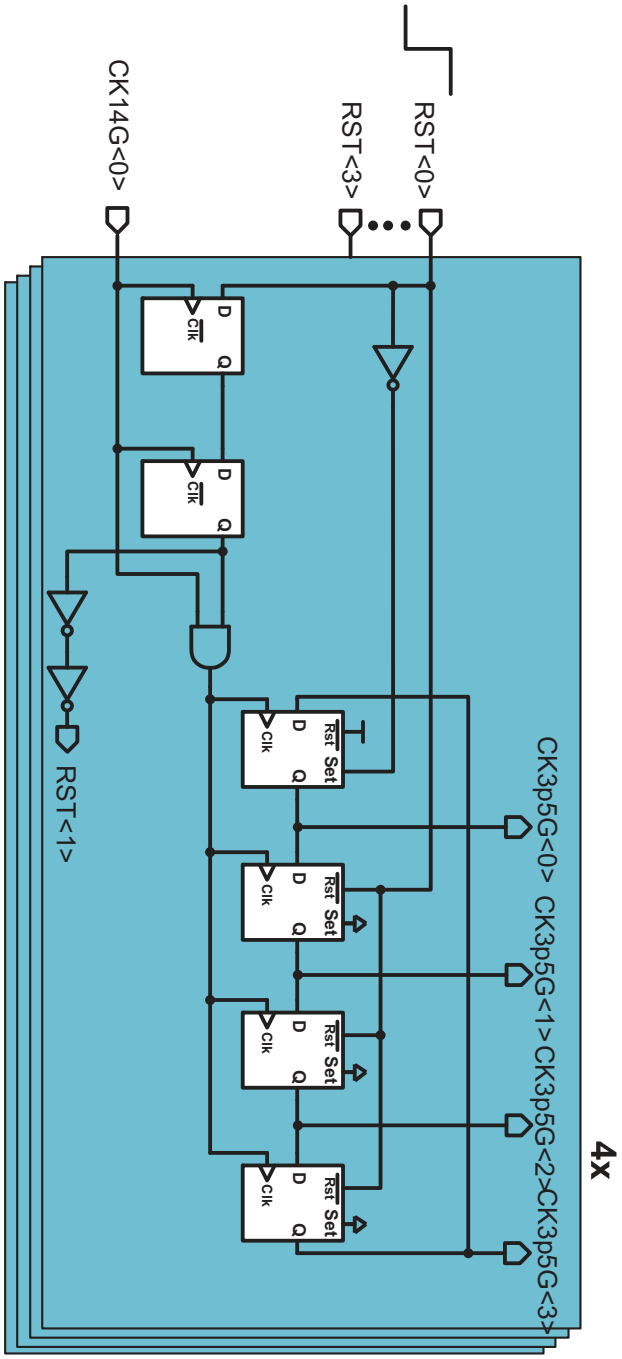

Figure 3.18. Schematic to generate the 25% duty cycle 3.5 GHz CK3p5G< 15:0 >.

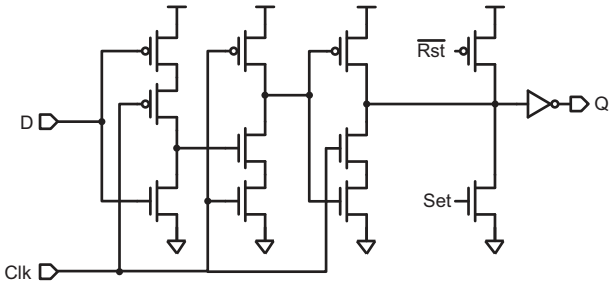

Figure 3.19. Schematic of TSPC flip flop.

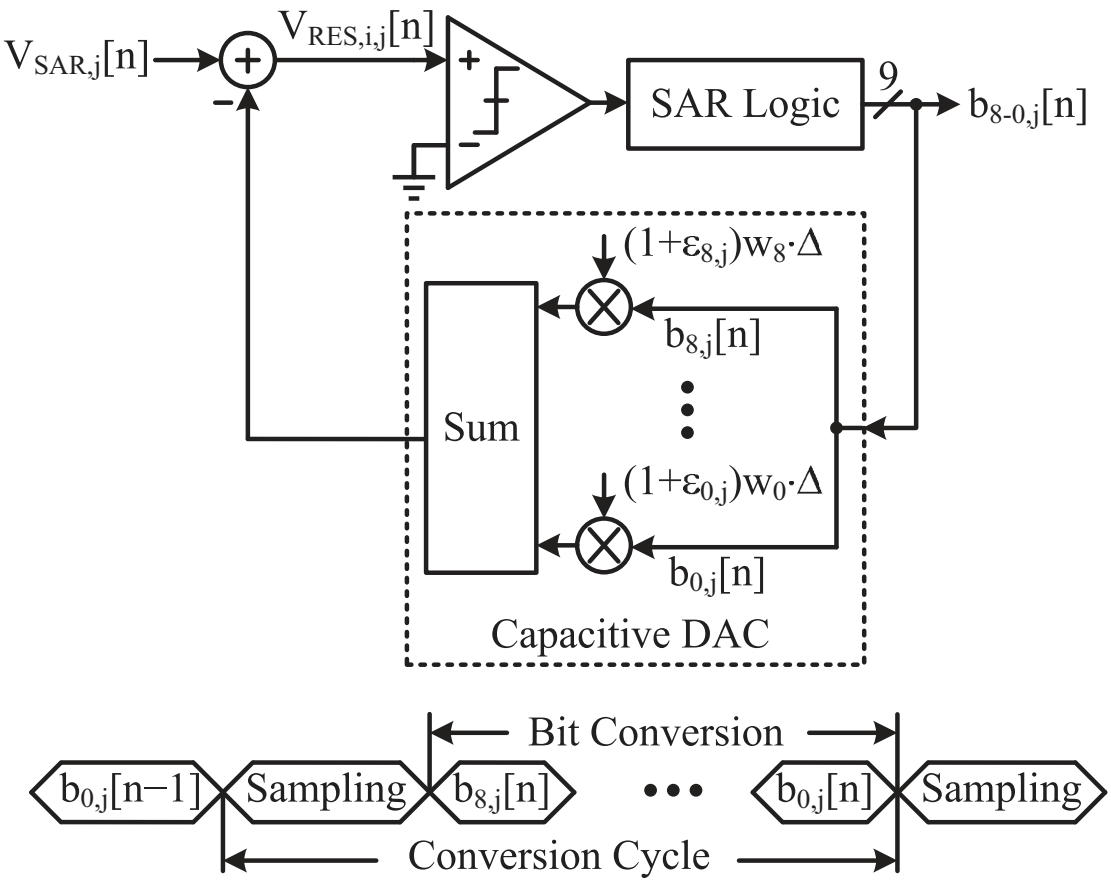

Figure 3.20. Block diagram of an 8-bit SAR ADC with 1 bit for redundancy.

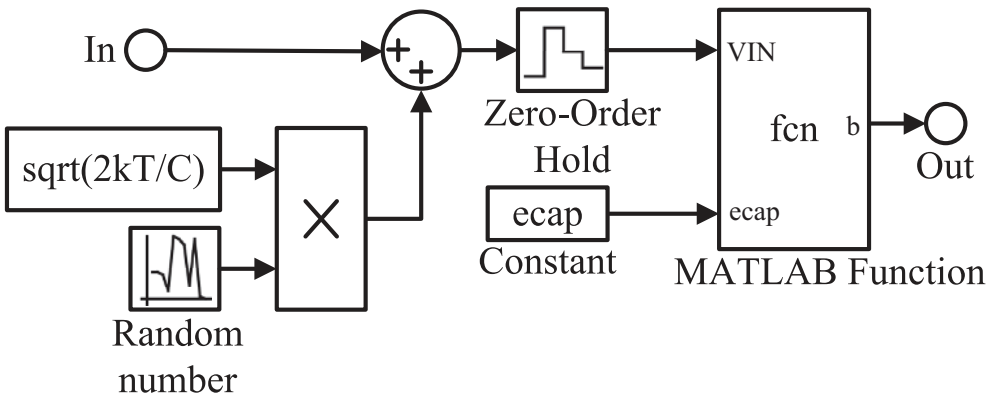

Figure 3.21. Model of an 8-bit SAR ADC.

where w_{i} is ideal capacitor weight and equals to 64, 32, 16, 8, 5, 3, 2, 1 and 0.5 for i from 8 to 0, $\epsilon_{\mathrm{i,j}}$ is a nonideal factor of the j-th channel resulting from capacitor mismatch and Δ is the quantization step. For the 1st bit conversion, $V_{\mathrm{RES,9,j}}[n] = V_{\mathrm{SAR,j}}[n]$, which is the input voltage of the SAR ADC. (3.14) and (3.15) are the transfer function between the input voltage and the raw conversion bits. Therefore, the input voltage can be reconstructed by computing the inverse transfer function with combining weights, i.e. analog-to-digital conversion with the calibration for capacitor mismatch.

The equations (3.14) and (3.15) can also be used to model the intra-channel capacitor mismatch effect at the behavioral level as shown in Fig. 3.21. The input signal In is a discrete-time signal coming from the front-end interleaver. The random numbers with Gaussian distribution, zero mean and unity standard deviation are multiplied with square root of $2\mathrm{k}T/C$ to mimic the $\mathrm{k}T/C$ noise on the differential signals. After addition of the $\mathrm{k}T/C$ noise, the signal is sampled with a sampling period of T_{S}=1/(875 MHz) by a zero-order hold. An vector of *ecap* represents the nonideal factor $\epsilon_{\mathrm{i,j}}$ for j-th ADC channel capacitor mismatch, where i is from 8 down to 0. The equations of (3.14) and (3.15) are implemented in the MATLAB function (available in SIMULINK) in the model, and the $b_{\mathrm{i,j}}[n]$ are obtained as outputs.

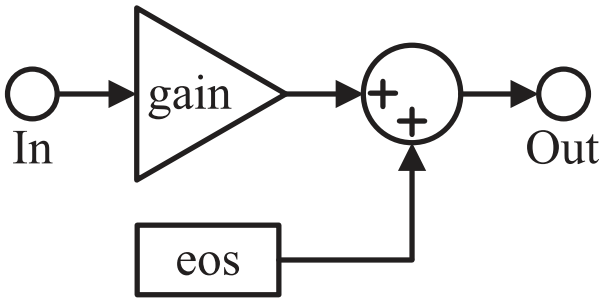

Figure 3.22. Model of inter-channel offset and gain mismatches.

Time-interleaving provides an effective means for ADC to achieve M times faster conversion rate than a single channel ADC, where M is the number of ADC channels. However, one inherent drawback of time-interleaving is channel mismatch, which has largely limited the performance and must be addressed.

Typical mismatch errors include offset, gain, sampling clock skew and bandwidth mismatches. Among various mismatch errors, inter-channel offset mismatch is the simplest form of error. It produces a periodic error term added in the digital output. In a single-tone test, the offset mismatch causes spurs located at $k \times f_S/M$ in the output spectrum, where f_S is ADC sampling rate and k is from 1 to M. Compared with the offset mismatch, the gain mismatch error is proportional to the input amplitude. In a single-tone test, the gain mismatch causes spurs located at $\pm f_{in} + k \times f_S/M$, where f_{in} is the input frequency [25]. Considering the offset and gain mismatches in ADC channels, the input signal $V_{SAR,j}$ of each SAR ADC can be written as

$$V_{SAR,j} = g_j V_{buf,j} + o_j \tag{3.16}$$

where g_j is the gain, and o_j is the offset for ADC channel j. The effect of the offset and gain mismatches can be simulated at the behavioral level shown in Figure 3.22, where *gain* represents the gain mismatch for g_j with Gaussian distribution, and *eos* represents the offset mismatch for o_j with Gaussian distribution.

There are two kinds of timing errors in a time-interleaved ADC, the sampling clock skew and clock jitter. The effect of clock skew and clock jitter is proportional to the input frequency. For a sinusoidal input signal, the largest timing error occurs at the input zero crossing points. The total timing error $\epsilon_{\mathrm{t,j}}$ for channel j can be written as

$$\epsilon_{\mathrm{t,j}} = \epsilon_{\mathrm{skew,j}} + \epsilon_{\mathrm{jitter}} \tag{3.17}$$

where $\epsilon_{\mathrm{skew,j}}$ represents the constant sampling clock skew error for channel j and $\epsilon_{\mathrm{jitter}}$ represents the clock jitter error. The sampling clock timing errors can also be seen as the phase error of the input signal sampled by an ideal clock. Therefore, the sampled signal $V_{\mathrm{T/H,j}}[n]$ with the sampling clock timing error $\epsilon_{\mathrm{t,j}}$ can be modeled using an non-integer delay interpolation filter

$$V_{\mathrm{T/H,j}}[n] = \sum_{i=-\infty}^{\infty} V_{\mathrm{INT/H}}[n] \frac{\pi \sin(n - k - \epsilon_{\mathrm{t,j}}/T_{\mathrm{step}})}{\pi(n - k - \epsilon_{\mathrm{t,j}}/T_{\mathrm{step}})} \tag{3.18}$$

where $V_{\mathrm{INT/H}}[n]$ is the n-th T/H input signal in discrete-time domain with a sampling period of T_{step} [30, 34].

Figure 3.23 shows a behavioral mode for the simulation of the effect of timing errors where *eskew* represents the sampling clock skew $\epsilon_{\mathrm{skew,j}}$, and *jrms* represents the root mean square (RMS) value for the clock jitter. The zero-order hold performs the ideal T/H operation at the sampling rate of 3.5 GHz. The noninteger delay interpolation filter with 201 taps is implemented in the MATLAB function. To reduce the error between the modeled noninteger delay filter with finite number of taps and the actual T/H circuit with timing errors, the simulation step of the discrete-time model is chosen to be $T_{\mathrm{step}} = T_{\mathrm{S}}/2$, where the T_{S} is the sampling period of the time-interleaved ADC. Figure 3.24 and 3.25 show the errors between the sampled signals of the 8-bit ADC in the modeled T/H circuit and the actual T/H circuit when $T_{\mathrm{step}} = T_{\mathrm{S}}$ and $T_{\mathrm{step}} = T_{\mathrm{S}}/2$, respectively. Of course, a filter with a larger number of taps and smaller simulation step can be more accurate for modeling the behavior of the sampling clock skew. However, extreme accuracy is not important, because the purpose of

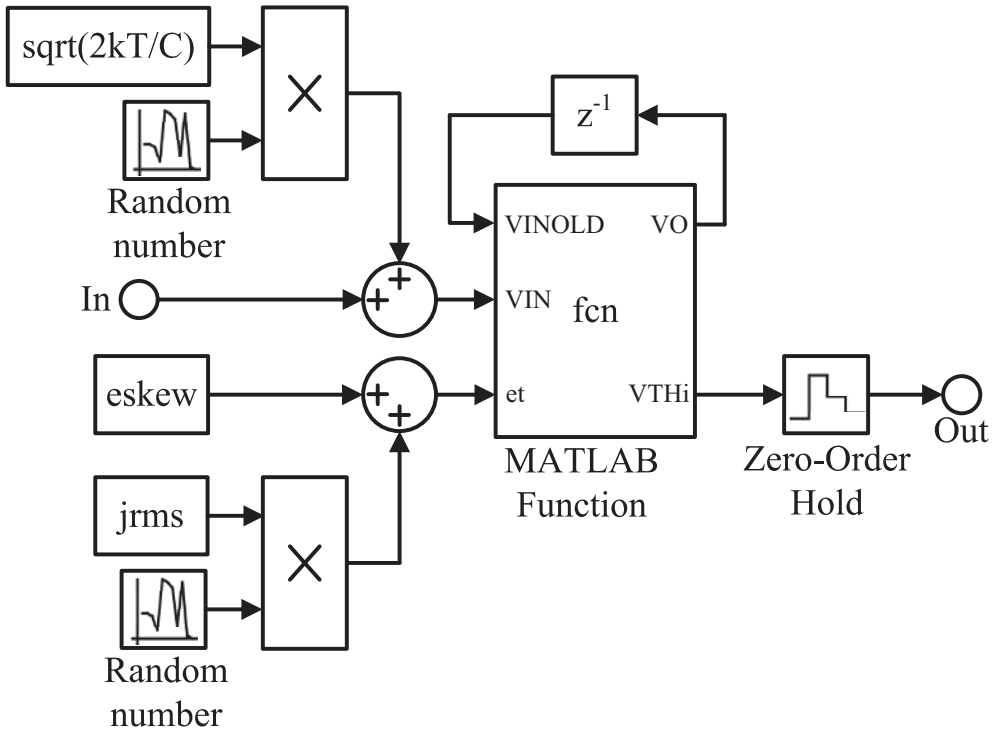

Figure 3.23. Model of inter-channel sampling clock skew mismatch with clock jitter by a 201-tap noninterger delay interpolation filter.

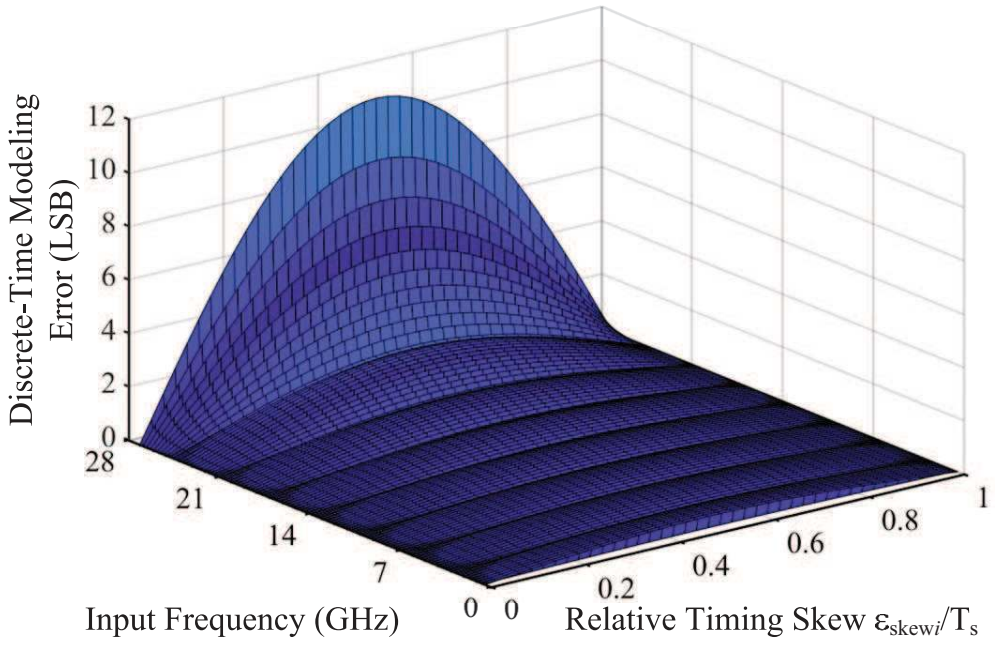

Figure 3.24. Discrete-time modeling error when simulation step $T_{\text{step}} = T_{\text{S}}$.

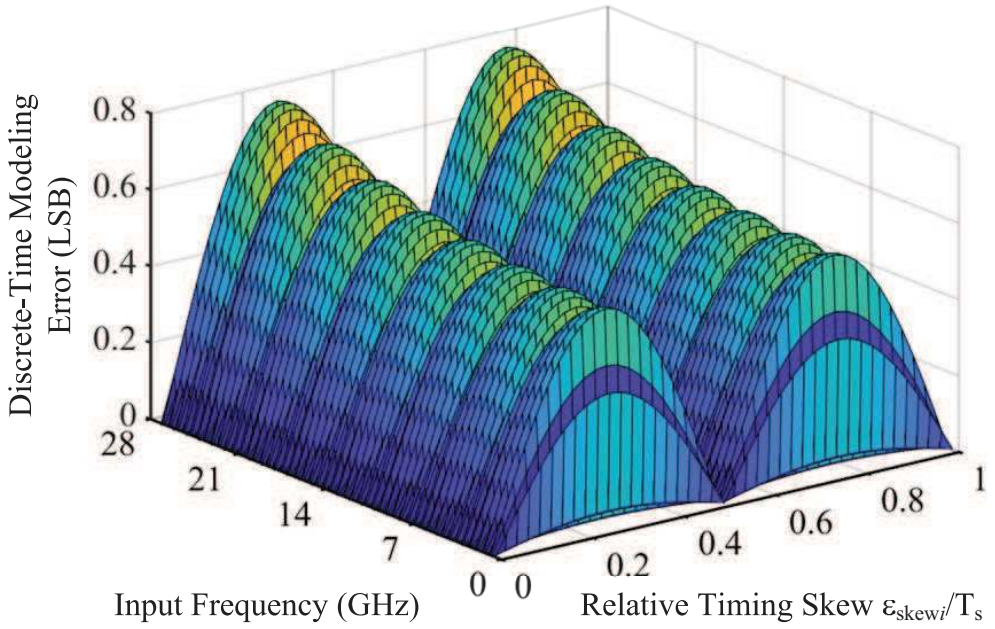

Figure 3.25. Discrete-time modeling error when simulation step $T_{\text{step}} = T_{\text{S}}/2$.

such behavioral model is to show the effects of mismatches and verify the effectiveness of the calibration scheme proposed in the following sections, and a filter with a large number of taps and small simulation step can slower down the behavioral simulation speed. A 201-tap noninterger delay Interpolation filter is used in our behavioral model to make the modeling error of the sampling clock jitter less than 1 LSB. A delayed feedback loop is used as a memory to store the input signal vector with 201 samples for the 201-tap interpolation filter. In each sampling period, a newest input V_{IN} together with its previous 200 samples stored in $VINOLD$ will constitute the vector VO, where VO and $VINOLD$ are the signal vectors with 201 elements.

Due to the process variation, the front-end input buffers and T/H circuits in track mode may exhibit different voltage transfer functions and result in inter-channel bandwidth mismatch. For a high-speed input signal, the inter-channel bandwidth mismatch causes phase mismatch and amplitude mismatch.

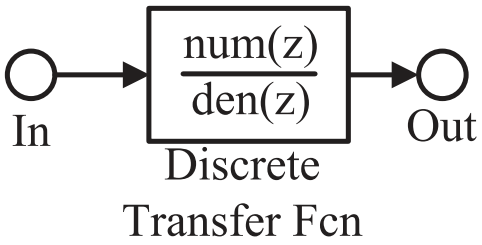

Figure 3.26. Model of inter-channel bandwidth mismatch.

Figure 3.26 shows the model for inter-channel bandwidth mismatch by using the Discrete Transfer Fcn (available in SIMULINK). Given a continuous-time transfer function $H(s)$, the corresponding discrete-time transfer function $H(z)$ can be obtained by continuous-to-discrete-mapping ($c2d$, function in MATLAB). The $num(z)$ and $den(z)$ represent the numerator and denominator of $H(z)$, respectively.

3.6. Digital Domain Error Compensation

Based on the model established in the previous section, we now describe the digital domain correction mechanism for the intra-channel capacitor mismatch and inter-channel offset, gain, sampling clock skew and bandwidth mismatches.

Compensation techniques for the capacitor mismatch in SAR ADCs have been described in numerous publications [6, 28]. The conceptual idea of analog-to-digital conversion with capacitor mismatch calibration is to use the raw converted outputs with combining weights to reconstruct the analog input signal and can be expressed as

$$V_{\mathrm{SAR,j}}[n] = \sum_{i=0}^{8} b_{\mathrm{i,j}}[n] w_{\mathrm{i,j}} \Delta + \epsilon_{\mathrm{q}} \tag{3.19}$$

where $\epsilon_{\mathrm{q}} = V_{\mathrm{RES,0,j}}[n]$ viewed as the quantization noise, $w_{\mathrm{i,j}} = (1 + \epsilon_{\mathrm{i,j}}) w_{\mathrm{i}}$ is the actual bit weight of each raw bit $b_{\mathrm{i,j}}[n]$ in j-th channel and i is from 0 to 8.

In the previous section, the inter-channel offset, gain, sampling clock skew and bandwidth mismatches are all mapped to discrete-time domain. Figure 3.27 shows a discrete-time model for time-interleaved ADC with inter-channel mismatches, where $s[n]$ is ADC input vector, $B_{0,0-1}(z)$ model the responses of input buffers with a sampling period of T_{S}, $B_{1,0-15}(z)$ model the T/H responses during tracking, P_{0-15} model the sampling clock skew, g_{0-63} model the channel gain, os_{0-63} model the channel offset, and $r_{0-63}[n]$ are the signal vector received by single channel ADC at a sampling rate of $64T_{\mathrm{S}}$. By defining $s_{\mathrm{j}}[n] = s[64n - j]$, where the channel number j is from 0 to 63, an equivalent multiple-input, multiple-output (MIMO) model can be obtained as shown in Figure 3.28, where $h_{\mathrm{i,j}}[n]$ denotes the channel impulse response between the j-th transmit node and the i-th receive node. Suppose the signal transmitted from the j-th transmit node is $s_{\mathrm{j}}[n]$. Then the signal received at the i-th receive node is expressed as

$$\begin{aligned} r_{\mathrm{i}}[n] &= \sum_{j=0}^{63} h_{\mathrm{i,j}}[n] * s_{\mathrm{j}}[n] + os_{\mathrm{i}} \\ &= \sum_{j=0}^{63} \sum_{k=-\infty}^{\infty} h_{\mathrm{i,j}}[k] s_{\mathrm{j}}[n-k] + os_{\mathrm{i}}. \end{aligned} \tag{3.20}$$

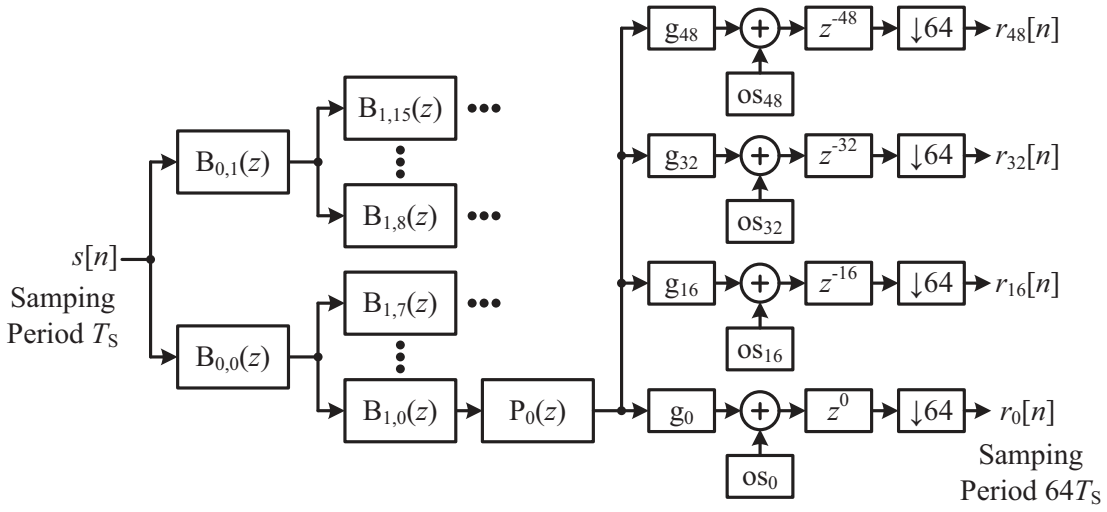

Figure 3.27. Block diagram of discrete-time model the time-interleaved ADC with inter-channel mismatches.

Given the discrete-time MIMO model of the time-interleaved ADC, the compensation of inter-channel mismatches can be formulated as the equalization problem of a MIMO channel [30]. The simplest equalization technique is to use the finite-duration impulse response (FIR) filters for the MIMO channel. The received signal is passed through a bank of 64 FIR filters, where each filter spans K samples. The filter coefficients are denoted as $a_{\mathrm{i,j}}[k]$, $k \in [0, K-1]$. The outputs of the FIR filters from the 64 receive nodes can be used to form estimates of the transmitted signal $s_{\mathrm{j}}[n]$, which can be written by [38]

$$s_{\mathrm{est,j}}[n] = \sum_{i=0}^{63} \sum_{k=0}^{K-1} a_{\mathrm{i,j}}[k](r_{\mathrm{i}}[n-k] - os_{\mathrm{i}} \tag{3.21}$$

where $s_{\mathrm{est,j}}[n]$ denotes the estimate of $s_{\mathrm{j}}[n]$. Considering the j-th transmitted signal $s_{\mathrm{j}}[n]$ has the most impact on the received signal $r_{\mathrm{j}}[n]$ and the received signals span around $r_{\mathrm{j}}[n]$ and little impact on the received signal that is far away from $r_{\mathrm{j}}[n]$, we choose $2L+1$ samples around $r_{\mathrm{j}}[n]$ (L precursors and L postcursors) to reconstruct the transmitted signal $s_{\mathrm{j}}[n]$.

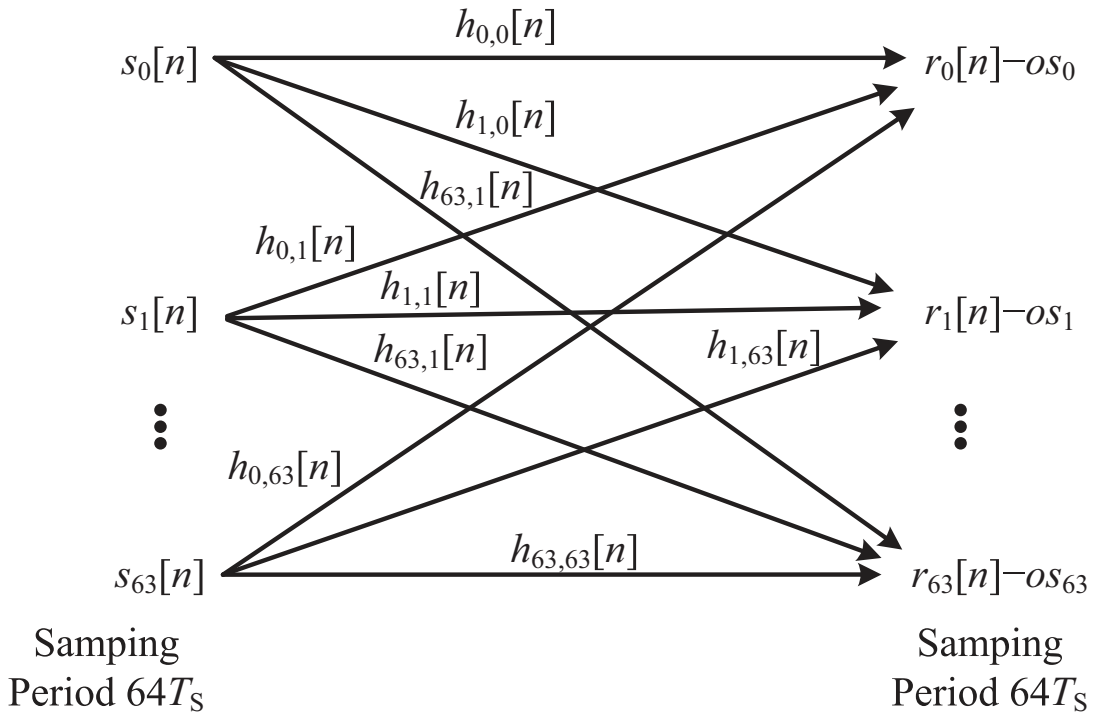

Figure 3.28. Equivalent discrete-time MIMO model of the time-interleaved ADC with inter-channel mismatches.

Therefore, from (3.21), the $s_{\mathrm{est,j}}[n]$ can be simplified and expressed by the new FIR filters as

$$\begin{aligned} s_{\mathrm{est,j}}[n] &= \sum_{k=-L}^{L} C_{\mathrm{k,j}} \left(r[64n-j-k] - os_{(\mathrm{j+k})\bmod 64} \right) \\ &= \sum_{k=-L}^{L} C_{\mathrm{k,j}} r[64n-j-k] + os_{\mathrm{est,j}} \end{aligned} \tag{3.22}$$

$$os_{\mathrm{est,j}} = \sum_{k=-L}^{L} C_{\mathrm{k,j}} \left(-os_{(\mathrm{j+k})\bmod 64} \right) \tag{3.23}$$

where $r_{\mathrm{j}}[n] = r[64n-j]$, $j \in [0, 63]$, $C_{\mathrm{j}}[k]$ denotes the new filter coefficients for channel j, $k \in [L, L]$, and *mod* represents the modulo operation. The above analysis summarizes equations (3.19) and (3.22) for the calibration of the intra-channel capacitor mismatch and inter-channel offset, gain, sampling clock skew and bandwidth mismatches. The next section will describe the proposed method to obtain the calibration parameters of $w_{\mathrm{i,j}}$, $C_{\mathrm{j}}[k]$, and $os_{\mathrm{est,j}}$, where $i \in [0, 8]$, $j \in [0, 63]$, $k \in [-L, L]$.

3.7. Digital Foreground Calibration Technique

ADC calibration techniques can be categorized into foreground calibration and background calibration. The background calibration can track variations caused by the changing ambient conditions during converter operation. One factor that determines whether a background calibration is a must depends on how large the ADC working condition may change and the resolution requirement. If the ADC working condition is stable and the ADC resolution is not high, then the foreground calibration is acceptable such as the foreground calibration schemes in [8, 17, 19, 23, 24].

The intra-channel capacitor mismatch and inter-channel offset, gain and sampling clock skew mismatches are calibrated in numerous published ADCs. However, only a few ADCs can compensate the inter-channel bandwidth mismatch by using FIR equalizers [12, 17, 26]. Those ADCs use pseudo-random data as input, and their background calibrations compare each conversion result with the most possible transmitted data symbol and compute the

mean square error (MSE). The coefficients of the FIR equalizers can be adjusted adaptively to minimize the MSE.

In this paper, we propose a foreground calibration that use sinusoidal tones as training signals to obtain the coefficients of the FIR equalizers. The advantage is that it is easier to generate the high-speed pure sinusoidal signal in practice with low distortions than the high-speed pseudo-random data with comparable accuracy. The inherent error in the actual pseudo-random data can result in some residual uncompensated inter-channel mismatch errors.

In general, the conventional foreground calibration approach was to inject a known low speed signal as the training signal to obtain the parameters for the error compensation [8,17,19,23,24]. Therefore, only the static errors can be calibrated. However, in our proposed foreground calibration, the FIR equalizers using the training signals from low frequency to Nyquist frequency, can compensate the frequency dependent dynamic mismatch errors.

Figure 3.29 shows the foreground calibration scheme for the intra-channel capacitor mismatch and the inter-channel offset, gain, sampling clock skew and bandwidth mismatches. The conversion results of 64 ADC channels are demuxed by 2 and the entire ADC outputs 128×9 bits for the demuxed 128 channels. The compensation of mismatch is based on the adjustment of the capacitor weights $w_{0-8,\mathrm{j}}$ and the coefficients $C_{\mathrm{k,j}}$, and $os_{\mathrm{est,j}}$ of 128 $(2L+1)$-tap FIR equalizers where $j \in [0, 127]$ and $m \in [-L, L]$. The weights and coefficients of FIR equalizers are calculated once by collecting the conversion results of the training frequencies from low frequency to Nyquist frequency and curve fitting. Afterwards, the weights and coefficients of FIR equalizers will freeze and the ADC begin the converter operation.

Figure 3.30 shows the flowchart of the estimation of the SAR ADC bit weights and the coefficients of FIR equalizers. For the estimate of the SAR ADC bit weights, there are two steps. In the first step, we set the initial values of the bit weights to be the values of the ideal case, where $w_{8,\mathrm{j}} = 64$, $w_{7,\mathrm{j}} = 32$, $w_{6,\mathrm{j}} = 16$, $w_{5,\mathrm{j}} = 8$, $w_{4,\mathrm{j}} = 5$, $w_{3,\mathrm{j}} = 3$, $w_{2,\mathrm{j}} = 2$, $w_{1,\mathrm{j}} = 1$, $w_{0,\mathrm{j}} = 0.5$. A low-frequency training input signal is fed into the ADC. Then based on the obtained uncalibrated results, we can use curve fitting ($lsqcurvefit$, function in MATLAB)

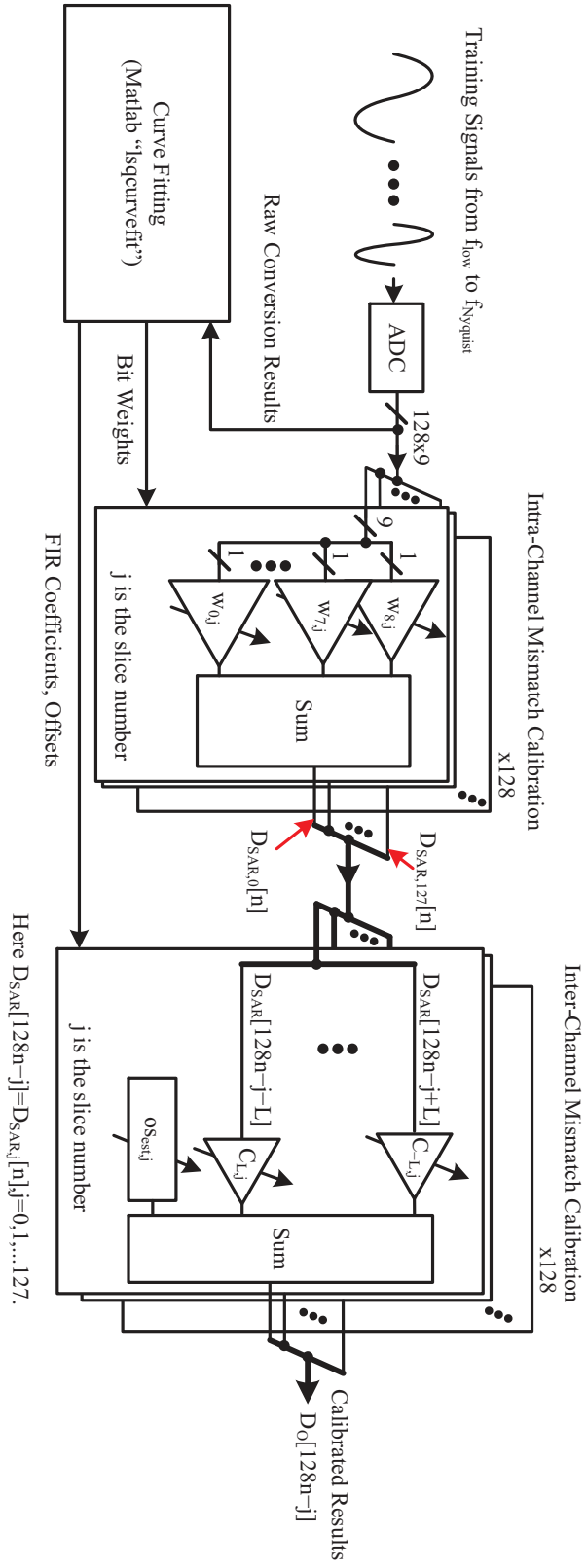

Figure 3.29. Foreground calibration scheme for the intra-channel capacitor mismatch and the inter-channel offset, gain, sampling clock skew and bandwidth mismatches.

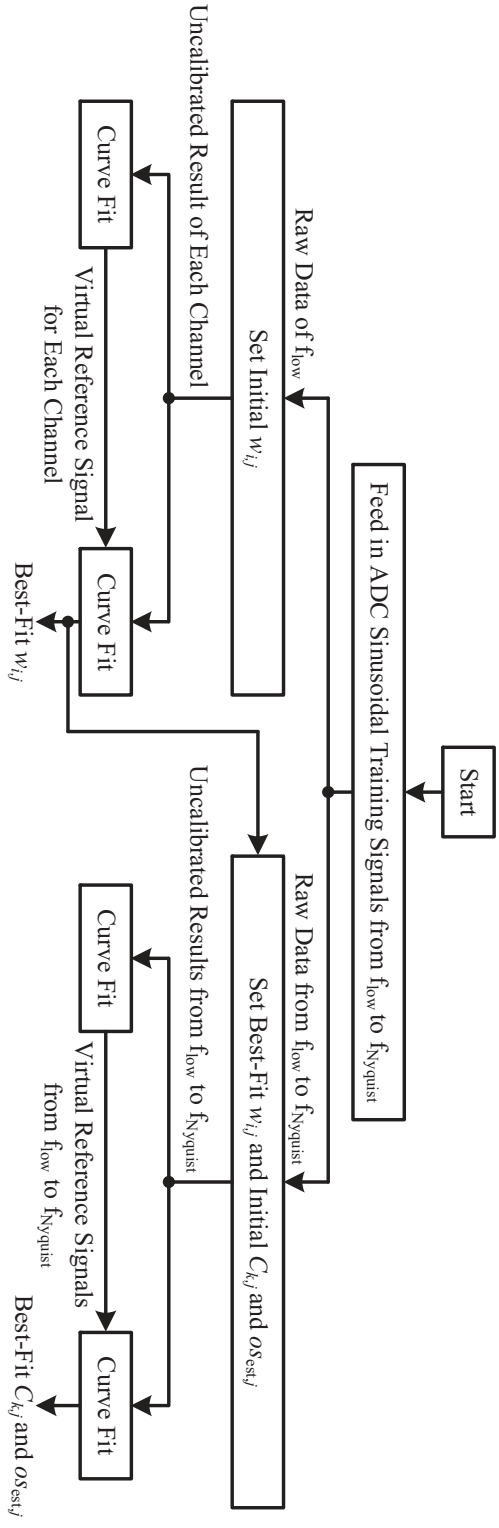

Figure 3.30. Flow chart of the foreground calibration.

to find out the values of the frequencies, amplitudes, phases and offsets of the training sinusoidal signals for each ADC channel. There are two inputs for the curve-fitting process. One is the target signal, which is a mathematical expression with unknown variables which we want to obtain. The other one is a known reference signal. The curve-fitting process can find out the values of the unknown variables that can minimize the MSE between the target signal and the reference signal. In this step, the expression of the target signal $V_{\mathrm{ref,j}}[n]$ is

$$V_{\mathrm{ref,j}}[n] = A_{\mathrm{j}}\cos\left(2\pi f_{\mathrm{j}} n T_{\mathrm{S}} + p_{\mathrm{j}}\right) + o_{\mathrm{j}} \tag{3.24}$$

where $V_{\mathrm{ref,j}}[n]$ represents the sine-fitted signal, A_{j}, f_{j}, pj, o_{j} denote the values of amplitude, frequency, phase and offset for the input training signal of j-th ADC channel, respectively. The obtained $V_{\mathrm{ref,j}}[n]$ is regards as a virtual reference signal.

In the second step, the curve-fitting process is executed again to estimate the bit weights $w_{\mathrm{i,j}}$, $i \in [0, 8]$, $j \in [0, 127]$. The $V_{\mathrm{ref,j}}[n]$ obtained in the first step is used as the virtual reference signal. In this step, we choose the conversion results of a low-frequency training signal for curve fitting because intra-channel capacitor mismatch is a static error, which is independent on the input frequency.

For the estimation of the coefficients of FIR equalizers, there are also two steps. In the first step, we set the initial values of the coefficients of FIR equalizersto be the values of the ideal case, where $C_{\mathrm{k,j}} = 0$ in the case $k \neq 0$, $C_{\mathrm{k,j}} = 1$ in the case $k = 0$. The training input signals from low frequency to Nyquist frequency are fed into the ADC. Then based on the obtained conversion results, we can use curve fit to find out the values of the frequencies, amplitudes, phases and offsets of the training sinusoidal signals as the virtual reference signals for the estimate of the coefficients of FIR equalizers.

In the second step, the curve-fit process is done again to estimate the coefficients of $(2L + 1)$-taps FIR equalizers. The expression of the target signal is

$$D_{\mathrm{O}}[128n - j] = \sum_{k=-L}^{L} C_{\mathrm{k,j}} D_{\mathrm{SAR}}[128n - j - k] + os_{\mathrm{est,j}} \tag{3.25}$$

$$D_{\mathrm{SAR}}[128n-j]=\sum_{i=0}^{8} b_{\mathrm{i,j}}[n]w_{\mathrm{i,j}} \tag{3.26}$$

where $C_{\mathrm{k,j}}$ and $os_{\mathrm{est,j}}$ are the coefficients of the FIR equalizers, $k \in [-L, L]$,$j \in [0, 127]$. $D_{\mathrm{SAR}}[128n-j]$ and $D_{\mathrm{O}}[128n-j]$ are the n-th results of channel j after calibrating the intra-channel capacitor mismatch and inter-channel mismatches, respectively. In this step, the conversion results from low frequency training frequency to Nyquist frequency are used for curve fitting, so that the obtained coefficients can be valid for inter-channel mismatch calibration of the entire first Nyquist band.

Table 3.5. Setup for Behavioral Simulation.

Parameter	Value
Sample Rate	56 GS/s
Resolution	8 bits
Full-Scale Input Range	600 mV
3dB BW of Input Buffer	53 GHz
BW Mismatch of Input Buffer (Normal dist.)	δ=5%
3dB BW of 1st-Stage T/H	53 GHz
BW Mismatch of 1st-Stage T/H (Normal dist.)	δ=5%
Sampling Cap. in 1st-Stage T/H for kT/C Noise	100 fF
Sampling Clock Skew Mismatch (Normal dist.)	δ=5%T_{S}
Sampling Clock RMS Jitter	70 fs
Sampling Cap. in 2nd-Stage T/H for kT/C Noise	200 fF
Sub-ADC Gain Mismatch (Normal dist.)	δ=5%
Sub-ADC Offset Mismatch (Normal dist.)	δ=5%$\times 2^8\Delta$
Sub-ADC Capacitor Mismatch (Normal dist.)	δ=5%

A model of MATLAB SIMULINK is devised for a 56 GS/s, 8 bit, 64 way interleaved ADC array to verify the proposed TI-ADC calibration algorithms. Referring to the previous study on the intra-channel capacitor mismatch and inter-channel mismatch, we set 5% mismatch in the behavioral simulation for the worst-case scenario [30,55]. The key parameters and the mismatch statistics of the TI-ADC array used in the simulation are listed in Table 3.5.

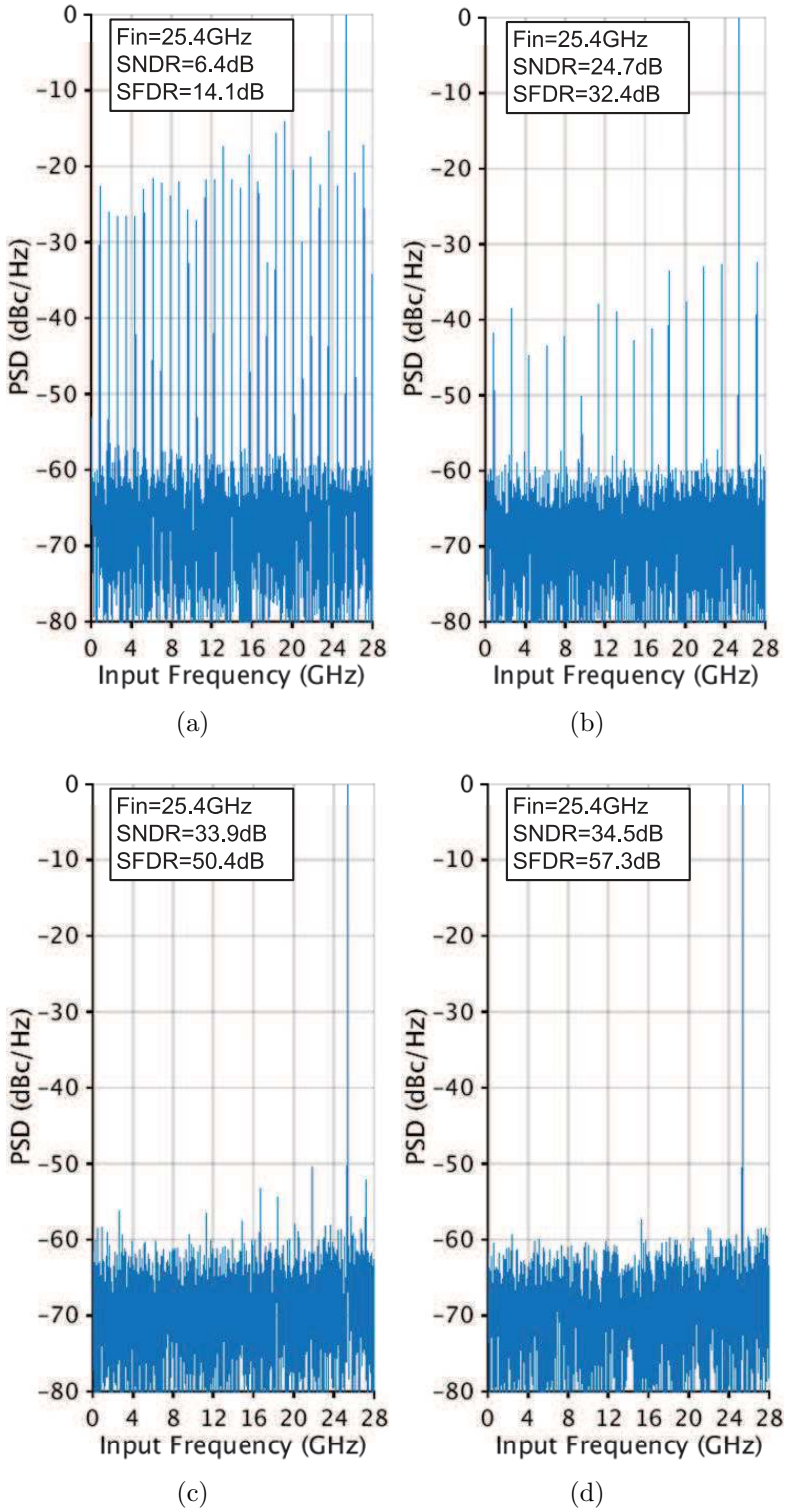

Figure 3.31. Simulated output spectra of the behavioral time-interleaved ADC model (a) before calibration, (b) after calibration with 3-taps FIR equalizers, (c) 9-taps FIR equalizers and (d) 15-taps FIR equalizers. Intra-channel capacitor mismatch calibration is also included.

Figure 3.31 shows the digital spectrum of the TI-ADC before calibration and after calibration with 3-taps FIR equalizers, 9-taps FIR equalizers and 15-taps FIR equalizers. Both of the intra-channel capacitor mismatch and inter-channel mismatches are calibrated. As the tap number of FIR equalizers increases, the power of the spurs caused by inter-channel mismatches after calibration can be compressed further. For a 15-tap FIR equalizer, the spurs caused by 5% Gaussion distributed mismatch after calibration can be smaller than -60 dB.

3.8. Measurement Results

The prototype ADC was fabricated in a standard 28 nm CMOS process. A micrograph of the $0.878mm^2$ chip is shown in Figure 3.32. The ADC was wire-bonded onto a chip-on-board carrier with short bonding wires for high speed input clocks and signals. The measured total power consumption is 702 mW, consisting of 291 mW for the interleaver, 181 mW for the clock generation, 209 mW for 64 SAR ADCs and 21 mW for the retimer and demux. The ADC was measured from a 0.95 V supply except for only a small portion of the circuit (input buffers) with a dual supply voltages of $+0.95$ V/-0.9 V.

Table 3.6. Test Equipment for the ADC Inputs and Clock Inputs.

Signal Generator for ADC Inputs	Keysight N5183B
Signal Generator for Clock Inputs	Keysignt E8257D
Balun	Marki BAL-0036
Phase Shifter	API Technology 6705K-5
Bias Tee	Marki BTN-0065

Figure 3.33 shows the test setup for the ADC inputs and clock inputs and the test equipment are summarized in Table 3.6. The test environment is shown in Figure 3.34. A Keysight N5183B with maximum output power of ∼21 dBm is used as the ADC input source. The ADC differential input range is 600 mV_{pp}. The fully diff. input is generated using a balun, and phase imbalance is tuned out by 2 tunable phase shifters. The losses of

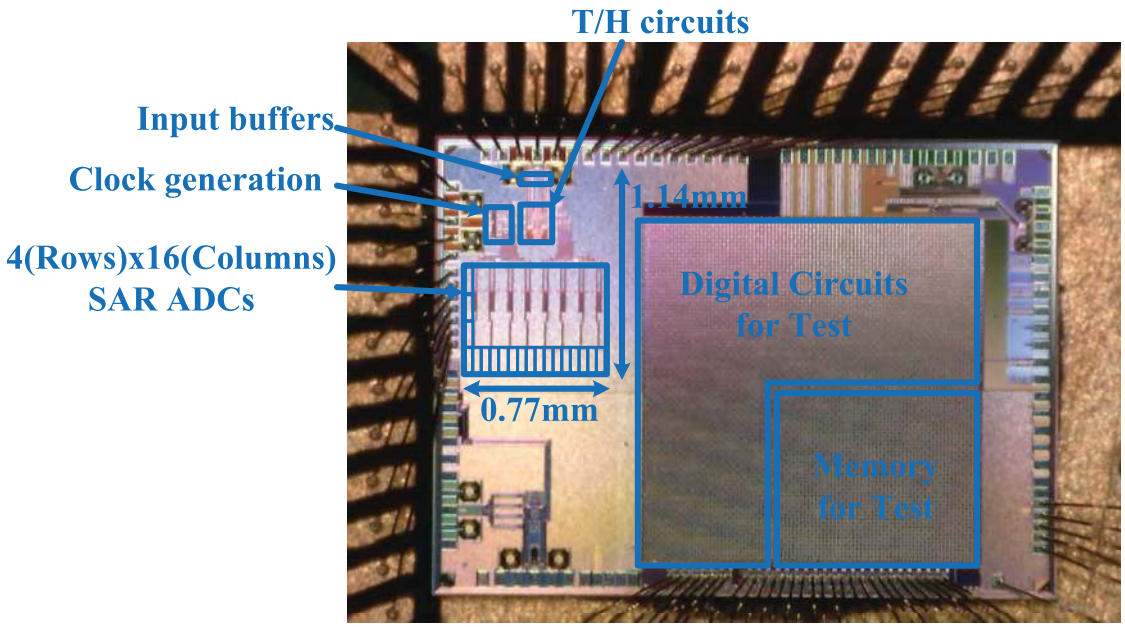

Figure 3.32. Die micrograph.

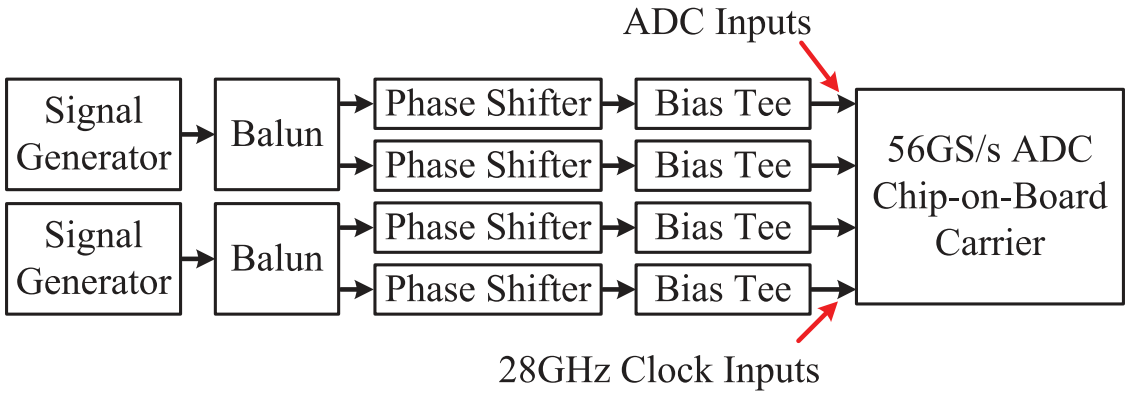

Figure 3.33. Test setup for the ADC inputs and clock inputs.

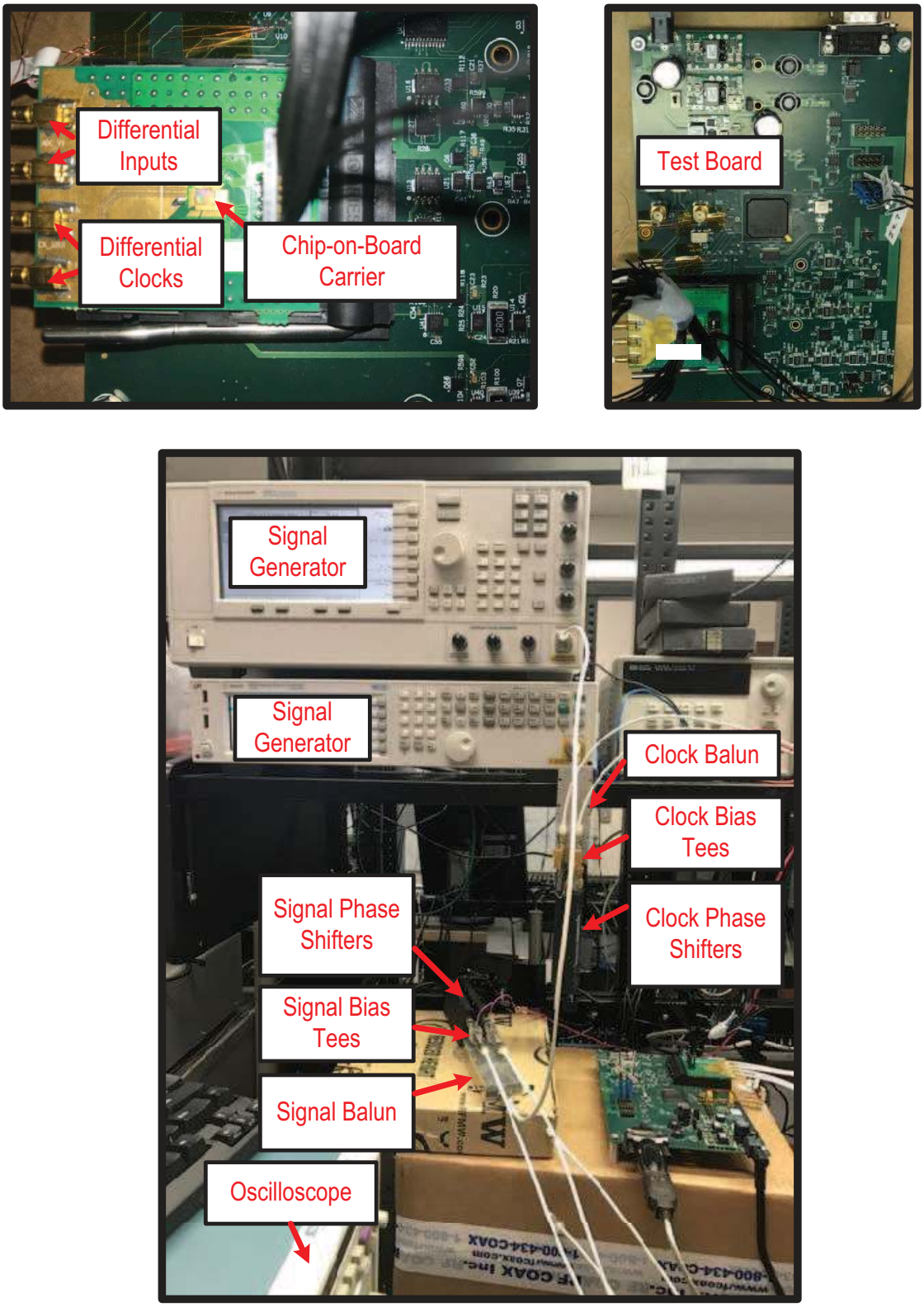

Figure 3.34. Test environment.

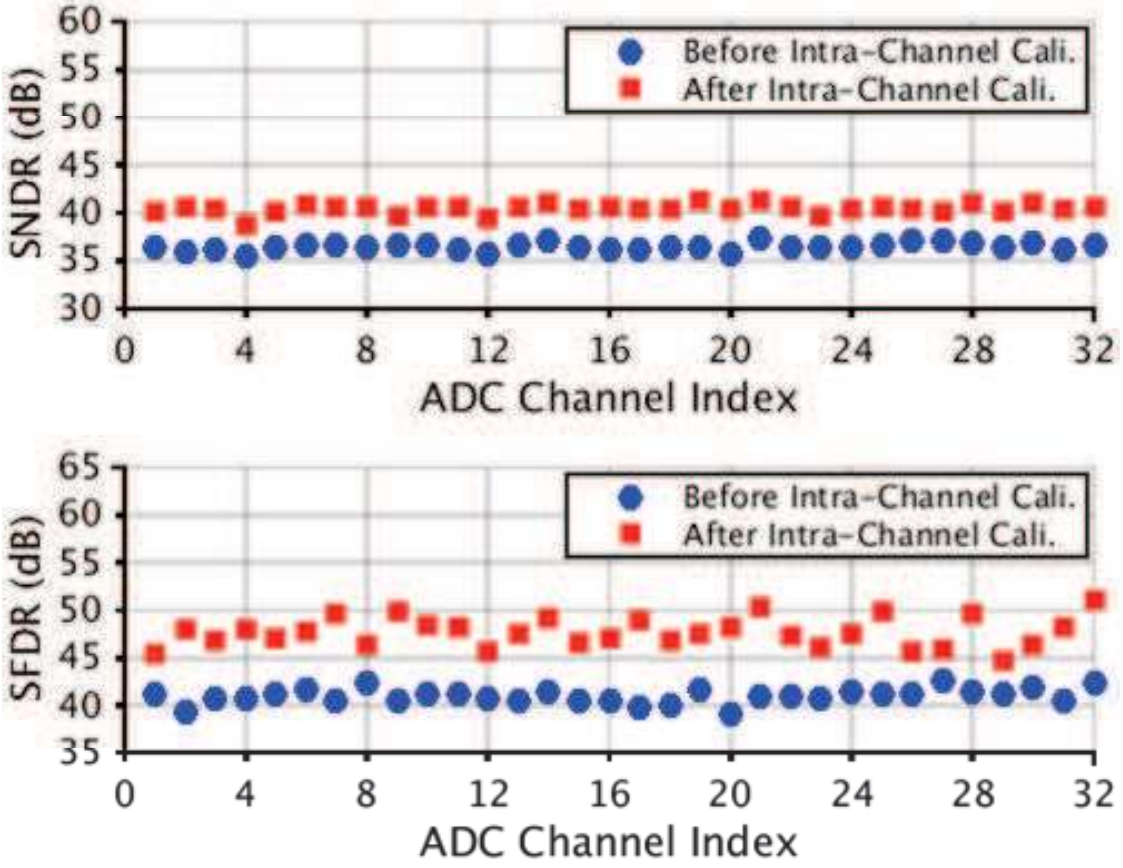

Figure 3.35. Measured SNDR and SFDR profile across the 32 ADC channels (f_S=0.875 GS/s, f_{in}=0.878 GHz).

balun, bias tee and cable are compensated at each test frequency. The 28 GHz clock inputs are provided by an external signal generator Keysight E8257D with $\sim$ 20 fs rms jitter. Note, however, that the jitter contributed by the on-chip sampling clock generation for the first-stage T/H circuits is $\sim$ 64 fs (based on worst case post-layout simulations). When a clock generations additive jitter J_{add} and the source jitter number J_{source} (which is typically given as an rms value), are provided, a root sum square value as shown in (3.27) can be used to calculate total jitter J_{tot}

$$J_{\text{tot}} = \sqrt{J_{\text{source}}^2 + J_{\text{add}}^2}. \tag{3.27}$$

Thus for the noise budget of 4.9-b ENOB at 28 GHz, the clock jitter contributes $\sim$ 19%.

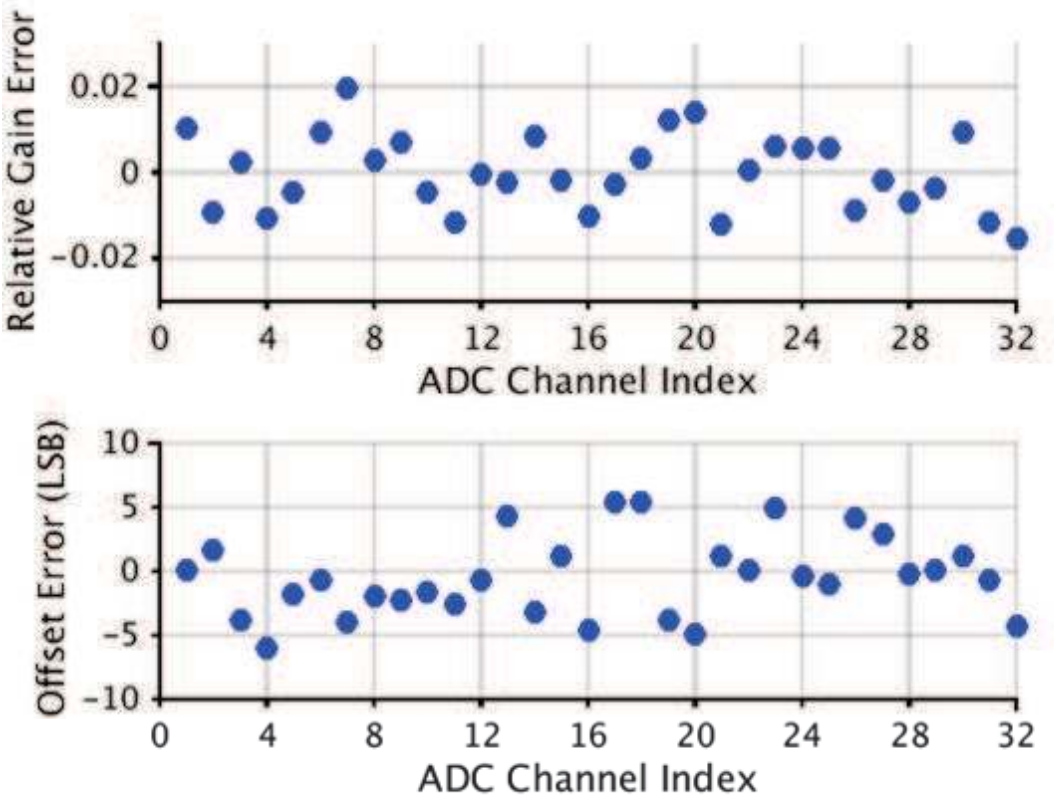

Figure 3.36. Gain mismatch and offset mismatch for 32 ADC channels. Gain and offset are estimated at 0.878 GHz input frequency.

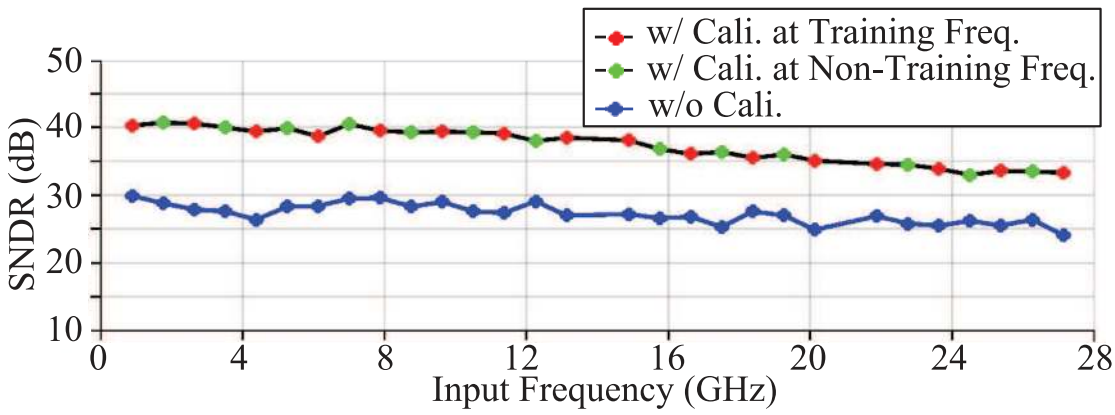

Figure 3.37. Measured SNDR vs. input sine frequency with and without calibration.

A one-time power-up calibration is performed off-chip to correct the intra-channel capacitor mismatch, and the inter-channel gain, offset, timing skew and BW mismatches. Then the signals of the training frequencies and non-training frequencies are fed into the ADC to evaluate the performance.

As a first step, an 878-MHz sine-wave input was used as the training signal to obtain the bit weights of each SAR ADC. The output power spectral density (PSD) of each ADC channel before and after the intra-channel capacitor mismatch calibration is measured. Due to an error in the digital/memory interface, the conversion results need to be decimated by two for estimating the performance. Figure 3.35 shows the variation of the SNDR and SFDR performance across 32 individual ADC channels. The SNDR and linearity improvement is nearly uniform among the interleaved ADC channels, demonstrating the benefit of correcting the intra-channel capacitor mismatch.

Next the inter-channel offset and gain mismatches are investigated. To estimate the mismatch value of offset and gain, we did an extra experiment that a 1-tap FIR equalizer was used to correct the gain error and offset error. Such 1-tap FIR equalizer cannot correct the inter-channel sampling clock skew and bandwidth mismatches, but it is an approach to investigate the mismatch values of offset and gain. By doing the curve fitting for the conversion results of the 878-MHz sine-wave input, the coefficients $C_{0,\mathrm{j}}$ and $os_{\mathrm{est,j}}$ of the

1-tap FIR equalizer of j-th ADC channel can be obtained. The $(1 - 1/C_{0,\mathrm{j}})$ and $-os_{\mathrm{est,j}}$ denotes the relative gain error and offset error of j-th ADC channel. Figure 3.36 provide details on the relative gain error and offset error. The gain and offset mismatches are caused by the mismatch of the input buffers, the mismatch of clock feedthrough, charge injection and sampling capacitance in the first-stage T/H circuits, the mismatch of sub-channel buffer and the mismatch of the reference voltage of ADC channels.

Table 3.7. Performance Comparison

	[24]	[5]	[26]	This work	
Technology	32 nm SOI	20 nm CMOS	28 nm CMOS	28 nm CMOS	
Resolution	8-bit	8-bit	8-bit	8-bit	
f_S(GS/s)	90	64	28	56	
SNDR@$f_{\mathrm{in,low}}$ (dB@GHz)	36@6	37.6@8	37@1	40.5@7	
SNDR@$f_{\mathrm{in,high}}$ (dB@GHz)	33@19.9	33.7@16	34@13.3	38.1@13.1	33@27.1
SFDR@$f_{\mathrm{in,high}}$ (dB@GHz)	41.4@19.9	NA	41.8@13.3	48.6@13.1	42@27.1
BW (GHz)	22	NA	18**	31.5	
Supporting Modulation Formats [4]	112 Gb/s DP-16QAM	112 Gb/s DP-16QAM	112 Gb/s DP-16QAM	112 Gb/s DP-QPSK 112 Gb/s DP-16QAM 112 Gb/s DP-64QAM 224 Gb/s DP-16QAM	
Power (mW)	667	950	165	702	
FOM@$f_{\mathrm{in,low}}$ (fJ/conv.step)	144	240	102	145	
FOM@$f_{\mathrm{in,high}}$ (fJ/conv.step)	203	375	140	344	
Area (mm^2)	0.45 (active)	1.77*	0.24 (active)	0.878 (active)	

* Estimation based on die photo

** Estimation based on [17]

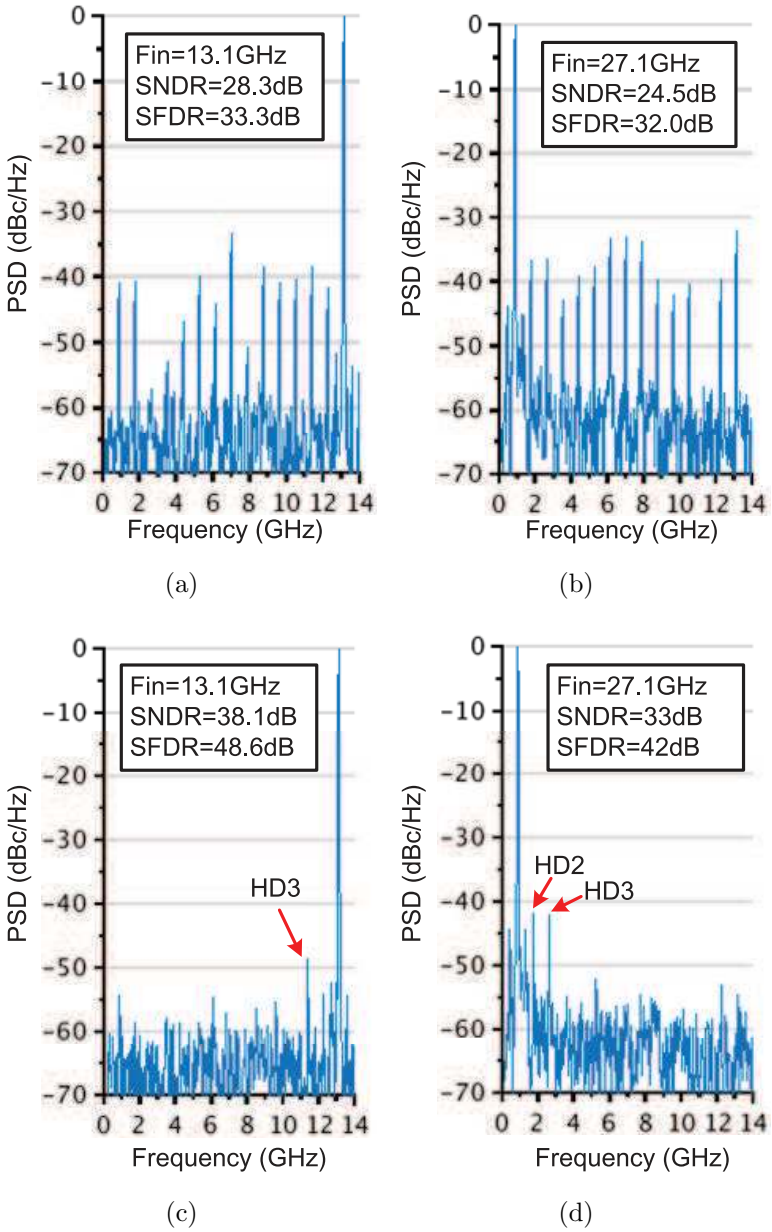

Figure 3.38. ADC output spectrum (a)(b) before calibration and (c)(d) after calibration.

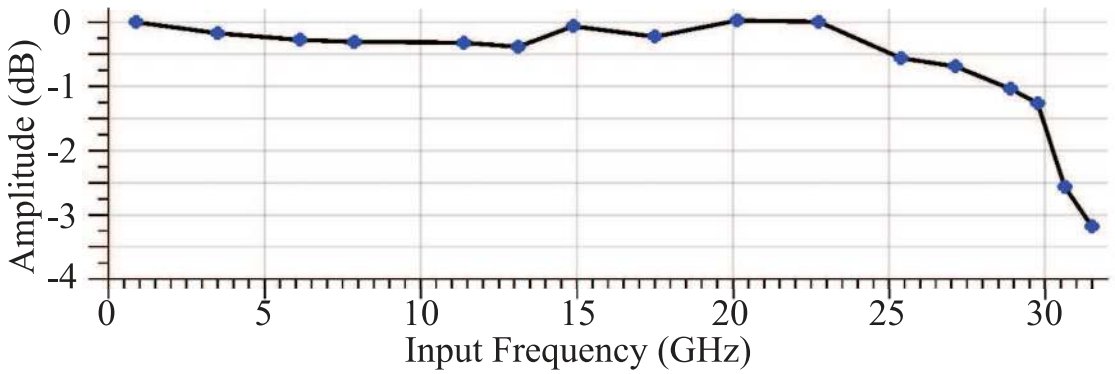

Figure 3.39. Measured single ADC channel output amplitude vs. input sine frequency.

We next characterized the ADC performance by using 15-taps FIR equalizers to correct all the inter-channel mismatches. In principle, the coefficients of FIR equalizers are calculated once by collecting the conversion results of the training frequencies from low frequency to Nyquist frequency and curve fitting. Then the signals of the training frequencies and non-training frequencies are fed into the ADC to evaluate the SNDR performance. But in practice, because the conversion results of the 56 GS/s ADC are decimated by two and the signal from 14 GHz to 28 GHz will fold back to the range from DC to 14 GHz in discrete-time domain, the coefficients of the FIR equalizers were computed twice for measuring the performance of signal frequency from DC to 14 GHz and from 14 GHz to 28 GHz, respectively. Figure 3.37 illustrates the measured SNDR vs. input frequency. Note that over 5.7-b ENOB and over 5.2-b ENOB are achieved up to 17.5 GHz and 27.1 GHz, respectively. In addition, the measured SNDR vs. input frequency demonstrates that the calibration works well at both the training frequencies and non-training frequencies. In Figure 3.38(a)(b), the output spectrum before calibration shows largest spurs related to the input frequency mixed with harmonics of 1/64th of the sampling clock frequency. After the calibration, the SFDR in Figure 3.38(c)(d) is limited by 2nd/3rd-order harmonic distortion and is 48.6 dB and 42 dB for Fin=13.1 GHz and Fin=27.1 GHz, respectively. In the spectrum, the tone of 27.1 GHz shows up as 0.9 GHz in Fig. 3.38 (b)(d). The measured BW of the ADC is 31.5 GHz, as shown in Figure 3.39, including the BW degradation due to input bonding wires and

insertion loss of traces of the chip-on-board carrier. Table 3.7 compares this work to state-of-the-art designs with similar applications. This ADC chip achieves the highest bandwidth and maintains the best SNDR up to Nyquist frequency under the same input frequency. Its FOM is similar to designs at 28-90 GS/s but achieves at least 1.4 times higher bandwidth. These advances make our ADC feasible to be applied in 224 Gb/s coherent receiver.

3.9. Conclusion

This section demonstrated the design of an ADC that can maintain the best SNDR up to Nyquist frequency and achieves the highest bandwidth (31.5 GHz) published to date compared with the previous reported 8 bit, >28 GS/s ADCs [32]. These results were enabled by the combination of the newly proposed parametric amplifier, the switched sub-channel buffer, the utilized multiple bandwidth enhancing techniques, and the foreground digital calibration. In addition, we introduced a set of models implemented in the MATLAB SIMULINK environment suitable for discrete-time domain behavioral simulations of the time-interleaved ADC. The proposed set of models takes into account at the behavioral level most of the non-idealities of the time-interleaved ADCs, such as inter-channel offset, gain, sampling clock skew and bandwidth mismatches, kT/C noise, sampling jitter, thus allowing us to obtain a good estimation of the calibration effectiveness of the intra-channel and inter-channel mismatches.

Chapter 4

64-WAY FRONT-END INTERLEAVER

4.1. Introduction

In order to have a insight of the performance of the front-end interleaver, the front-end interleaver alone is also designed and fabricated. This sections will introduce the design details and show the measured results of the front-end interleaver. Front-end track-and-hold amplifier (THA) is a core circuit in the time-interleaved ADC for the application of the high data rate optical communication system. The performance of T/H circuit affects the input bandwidth, signal-to-noise ratio and the distortion of the overall ADCs.

Traditional T/H circuits work well in low input frequencies. However, as the input frequency increases, the tradeoff between signal-swing-related linearity and signal-to-noise ratio is always encountered. This is because the variation of the signal-dependent resistance of T/H is much more severe for the input signal with large swing than that with small swing. On the other hand, given the constant power of thermal noise, a large signal swing is desired for better signal-to-noise ration. In addition, traditional hierarchical T/H amplifier uses output buffers to drive a bank of sub-channel ADCs. Because of the limited bandwidth of the sub-channel buffers, the settling errors of the outputs are generated in the track period. And then in the hold period those errors will be coupled to the inputs of the buffers through parasitic capacitors, resulting in harmonic distortions.

This section presents a 32-GHz-bandwidth and low distortion parametric track-and-hold amplifier in 28 nm CMOS. The parasitic capacitors are utilized as the sampling capacitor instead of an extra specific capacitor to achieve the highest input bandwidth. In addition, the T/H amplifier itself constitutes a parametric amplifier by having a bigger sampling capacitance in track period than that in hold period for amplifying the signal amplitude.

Therefore, the signal with small swing can be fed to the input of T/H amplifier for low distortion. After sampling, the signal is amplified to maintain the signal-to-noise ratio. In addition, a switched sub-channel buffer is proposed that can set the output of the buffer to ground in the track period to avoid the settling error in track phase and achieve low distortions.

4.2. Proposed Architecture

As shown in Figure 4.1, the proposed THA consists of input matching network MN, an input buffer Buf_{in}, the T/H core, output buffer Buf_{out}, and an additional driver stage Buf_{meas}. One of 16 output pairs of output buffers, SARIP$\langle 8 \rangle$ and SARIN$\langle 8 \rangle$ feeds to the final driver stage Buf_{meas} with 50 Ω output resistance for the purpose of measurement only. The driver stage Buf_{meas} is a common-source amplifier with source degeneration.

The input matching network MN uses two inductors that are in serial with terminal resistors to compensate the input parasitic capacitance for high bandwidth. However, the inductance is kept small, that is 130pH to avoid the amplitude overshoot at high frequencies and the additional group delay. By adding the ESD protection circuits for the differential input signals at input common node instead of input nodes, not only the ESD current can flows away through the terminal resistors and inductors, but also the bandwidth of MN will not be reduced by the parasitic capacitance of ESD circuits.

To increase the THA bandwidth, the source follower based input buffer Buf_{in} is also used to drive the T/H core. The dual supply voltages 0.95 V and -0.9 V are needed by Buf_{in} to make the output DC level can be as low as about 0.15V for the purpose of small turned-on resistance of T/H core. Transistors M_3-M_6 are triple-well NMOS devices, whose bulks are connected negative power supply and constitute the cascade current sinks. The T/H core is implemented with 0.95 V core MOS devices; transistors M_7-M_8 constitute the sampling switches; additional transistors M_9-M_{10} are introduced to signal feedthrough compensation; transistors M_{11}-M_{12} are used to compensate the clock feedthrough to avoid the sampled voltage below ground. To achieve highest signal bandwidth, the parasitic capacitors are

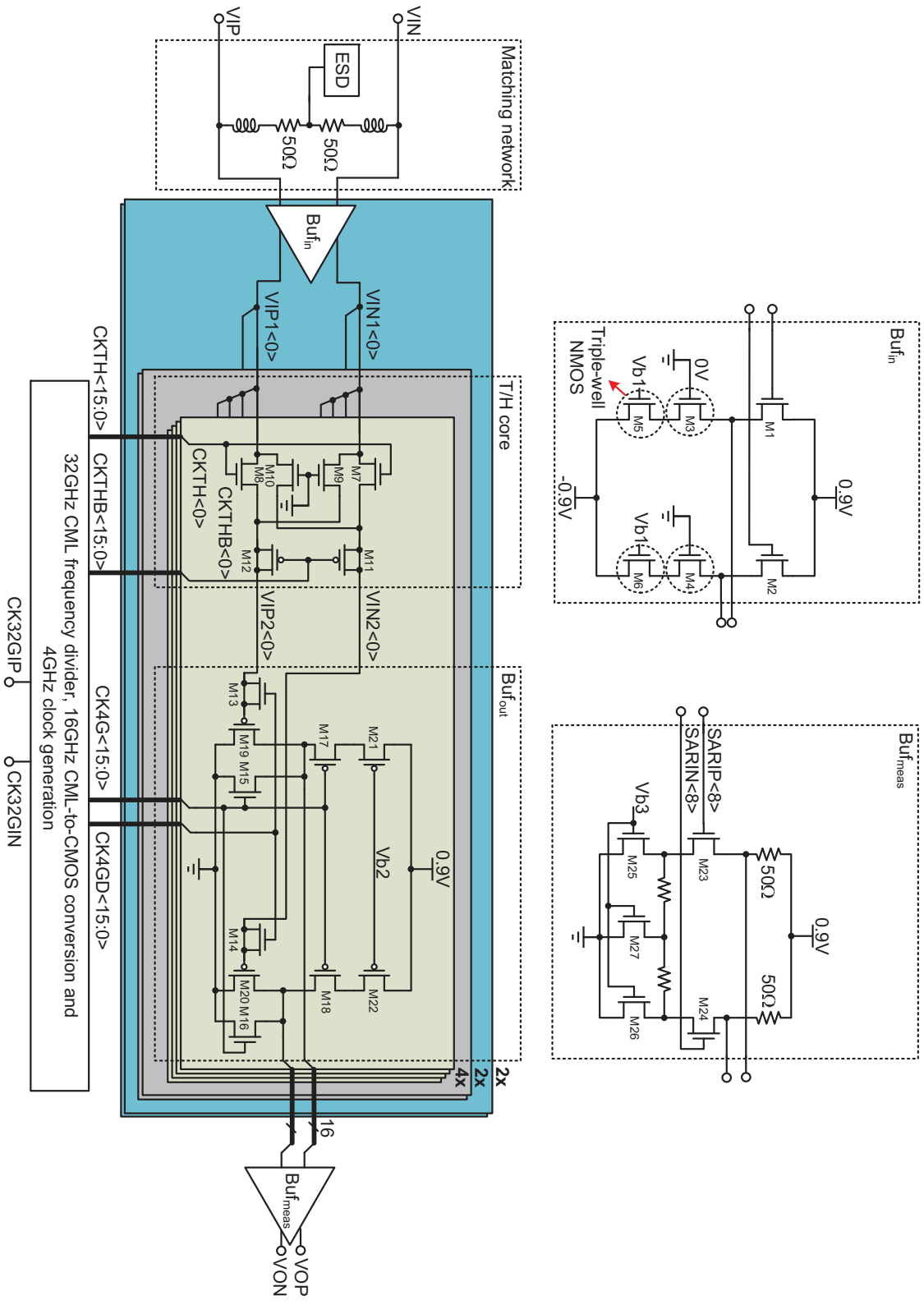

Figure 4.1. Schematic of the complete THA with matching network MN, input buffer Buf_{in}, T/H core, output buffer Buf_{out}, and measurement equipment driver stage Buf_{meas}.

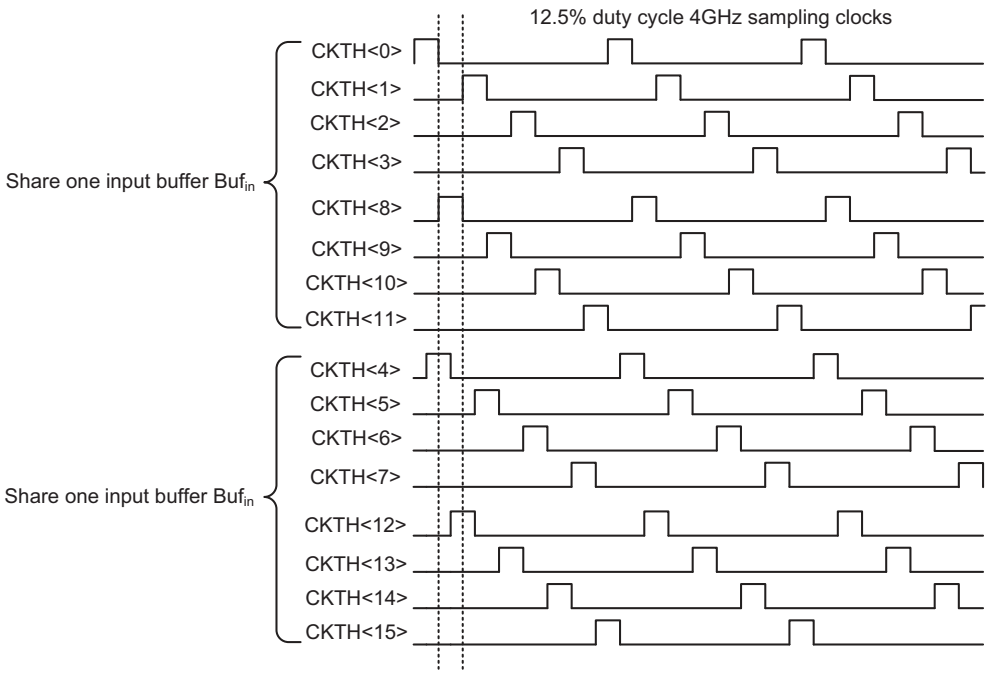

Figure 4.2. Diagram of sampling clocks.

used for sampling without specific extra sampling capacitor. The timing diagram of sampling clocks $CKTH\langle 15:0\rangle$ is shown in Figure 4.2, which is 12.5% duty cycle 4 GHz out of phase 22.5°. To ensure at anytime there is only one T/H core turned-on, driven by the input buffer Buf_{in} and avoid the interference of clock feedthrough among the T/H cores, the T/H cores are divided into two groups driven by two input buffers. 8×T/H cores with the sampling clock of $(2k) \times 22.5°$ share one input buffer; the other 8×T/H cores with the sampling clock of $(2k+1) \times 22.5°$ share another input buffer, where k is an integer number from 0 to 15.

Traditionally, continuous-time output buffers are used in the high-speed hierarchically time-interleaved ADC and always working in the track phase. For several tens of Giga Hz signal, because the bandwidth of the output buffers of THA cannot be that high, the settling errors of the output buffers exist and will be coupled to the sampling capacitor node through the input-output parasitic capacitors of output buffers, resulting harmonic distortions. A switched-output buffer Buf_{out} is proposed that can be reset in the track phase and enabled in the hold phase. The output buffer Buf_{out} is a PMOS source follower and basically composed

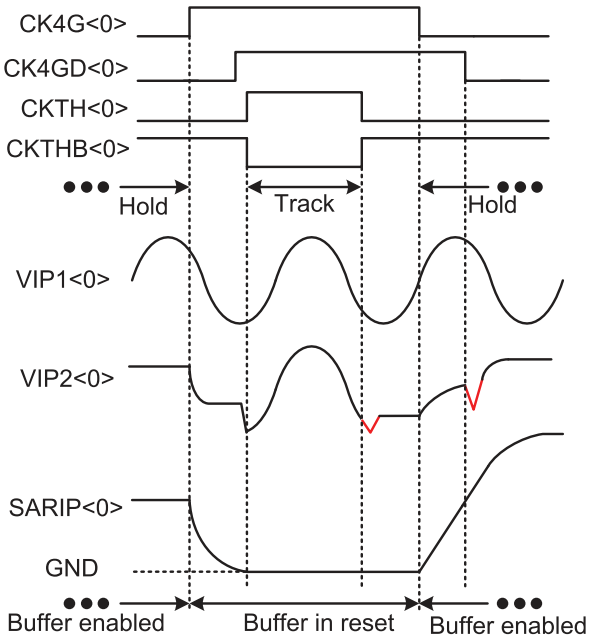

Figure 4.3. Diagram of signals in THA.

by M_{19}-M_{22}. In the track phase, the Buf_{out} is shut down by M_{17}-M_{18} cutting off the DC current and the outputs of Buf_{out} are shorted to ground by turning on switches M_{15}-M_{16}. In the hold phase, the Buf_{out} is enabled by turning on M17-M_{18} and off M_{15}-M_{16}. In track phase, the output buffers do not track the high-speed input signal and avoid the settling errors on the outputs. As a result, the linearity of THA is improved. M_{13}-M_{14} are used to compensate the undesired increase of the common-mode voltage that caused by the output voltage increase ground to the driving voltage in hold mode. Some intentional delay is added for this compensation to avoid the sampling voltage dropping below ground. The detailed signal diagram is shown in Figure 4.3.

Another innovation of the THA is that the T/H core circuit together with the input parasitic capacitance of Buf_{out} constitute a parametric amplifier. Nowadays, as the power supply voltage scales, a plaguing problem is that a trade-off always exists between signal-swing related signal-to-noise ratio and linearity. Typically, given a power supply voltage, a signal with large swing at the input of the T/H core circuit is desired for signal-to-noise ratio

Table 4.1. Working regions of parametric T/H amplifier transistors

C_S (Device Width)	Track		Hold	
	C_S (fF)	Region	C_S (fF)	Region
$C_{d,M7,8}$(13.5 μm)	11.1	Linear	8.5	Cutoff
$C_{d,M9,10}$(13.5 μm)	8.5	Cutoff	8.5	Cutoff
$2C_{d,M11,12}$(14 μm)	10.5	Weak-Inversion	9.3	Cutoff
$C_{g,M19,20}$(62 μm)	34.6	Cutoff	23.8	Saturation
$2C_{d,M13,14}$(9 μm)	14.0	Linear	9.2	Cutoff
$C_{MetalRouting}$	22.1	-	22.1	-
Total C_S (fF)	100.8		81.4	
Power Gain	1.9 dB			

consideration, but will result in poor linearity because of large variation of signal dependent turned-on resistance of T/H core circuit. To achieve both large swing and linearity, the signal can be amplified after sampling and then be quantized. A parametric amplifier is a circuit in which amplification is achieved by the use of variable parameters or circuit elements [21]. The advantage of a parametric amplifier is that it has much lower noise than an ordinary amplifier based on a gain device like transistor. This is because the gain of a parametric amplifier comes from varying the passive devices. In our work, the parasitic sampling capacitance is intentionally designed to make the sampling capacitance in track phase larger than that in hold phase. Because the sampled charge remains, the signal voltage of sampling capacitance can be amplified in the hold phase. Table 4.1 shows the schematic simulation results of parasitic sampling capacitors. In track phase, sampling capacitance $C_{s,track}$=100.8 fF; In hold phase, sampling capacitance $C_{s,hold}$=81.4 fF. Thus the gain of $C_{s,track}/C_{s,hold}$=1.9 dB can be obtained by the parametric amplifier.

4.3. Measurement Results

The proposed parametric THA with switched output buffer is fabricated in 28 nm CMOS process. Figure 4.4 shows the chip micrograph with an area of 0.28 mm^2 including clock generation blocks (CML frequency divider, CML buffer, CML-to-CMOS conversion, 4 GHz clock generation) and signal sampling blocks (input matching network, input buffer, T/H core and output buffer). The die is wire bonded to a chip-on-board carrier with very short bond wires to reduce the parasitic inductance. Figure 4.5 shows the test environment of the interleaver. The test equipments include 2 signal generators as the input clock source and input signal source, 2.92 mm 24 inch length cable with K connector and GPPO connector, balun, phase shifter, bias tee, chip-on-board carrier 33 GHz-BW 100 GS/s oscilloscope, and test board.

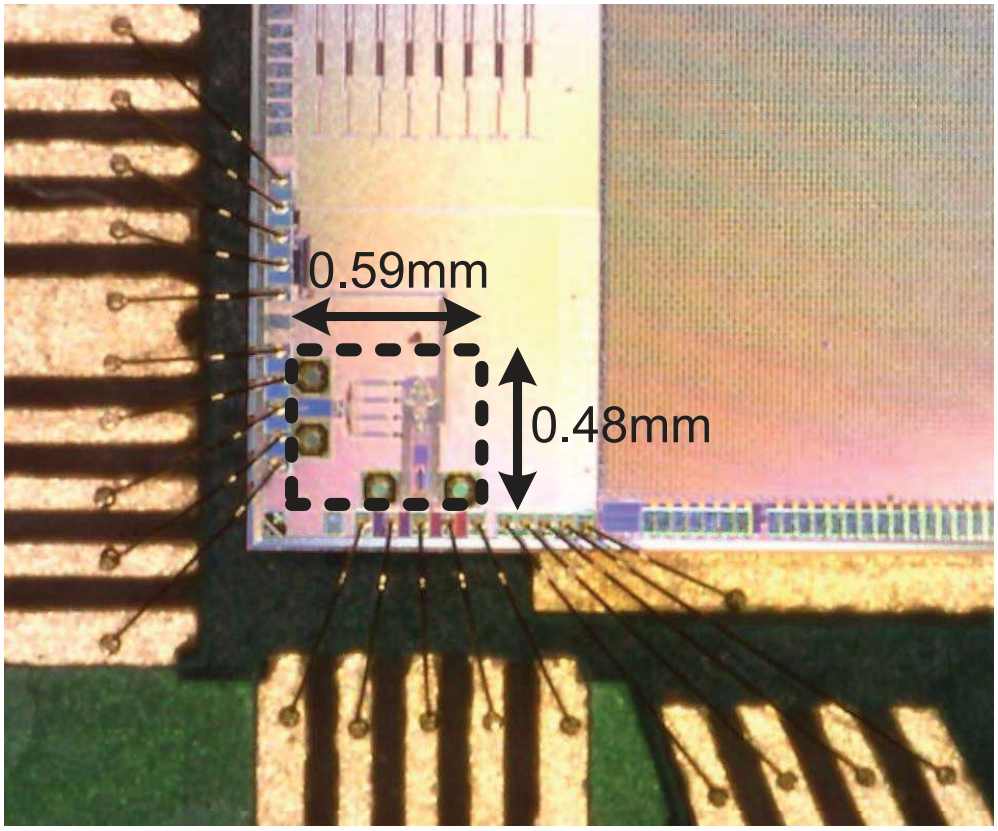

Figure 4.4. Chip micrograph of the interleaver.

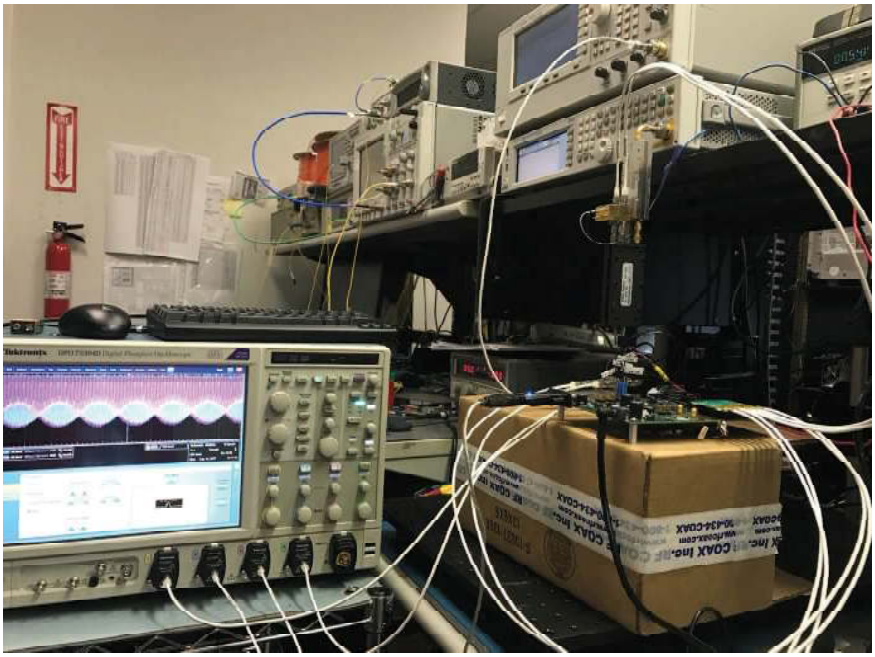

Figure 4.5. Test environment of the interleaver.

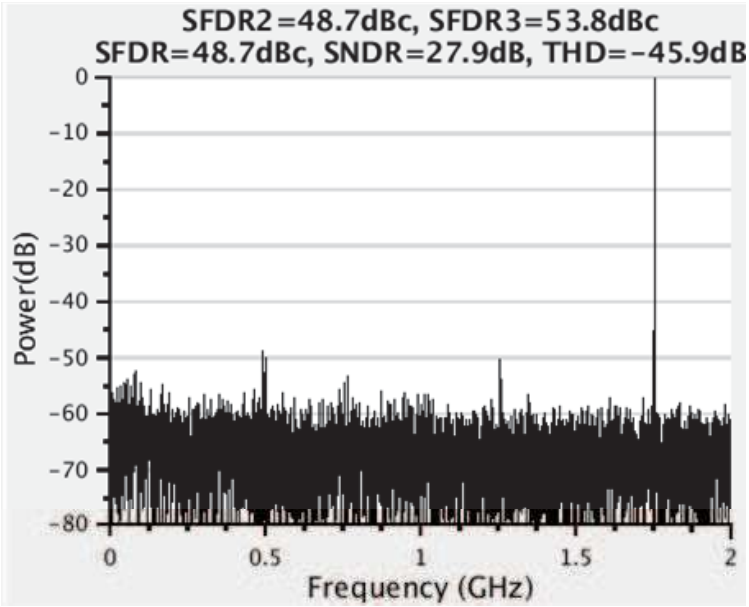

Figure 4.6. Output spectrum of one channel output buffer with Fin=1.75 GHz.

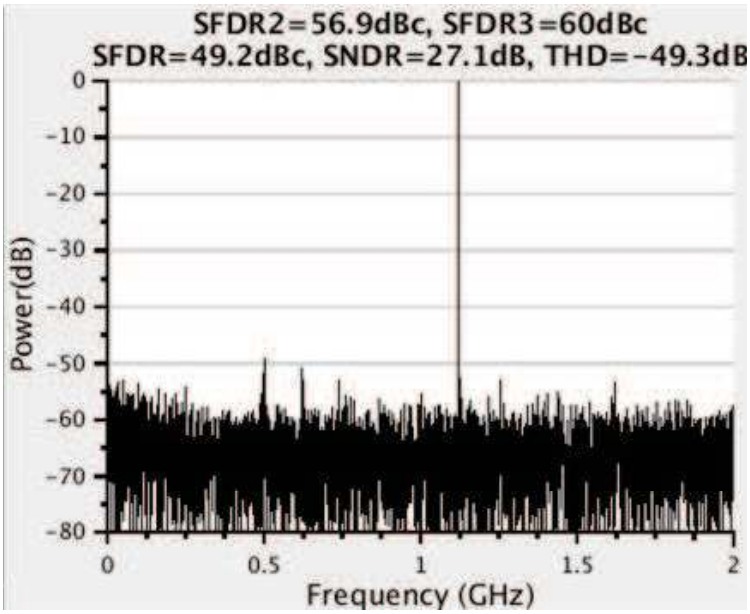

Figure 4.7. Output spectrum of one channel output buffer with Fin=14.9 GHz.

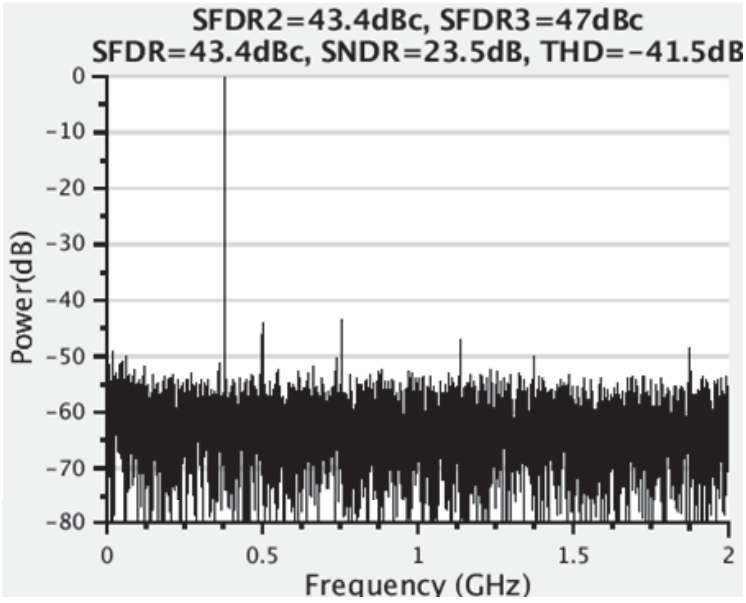

Figure 4.8. Output spectrum of one channel output buffer with Fin=32.4 GHz.

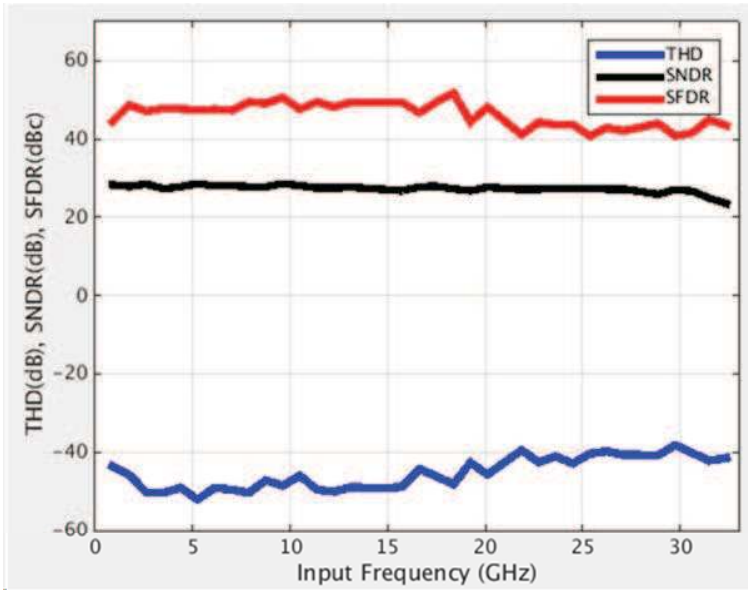

Figure 4.9. THD, SNDR, SFDR vs. input frequency of the interleaver.

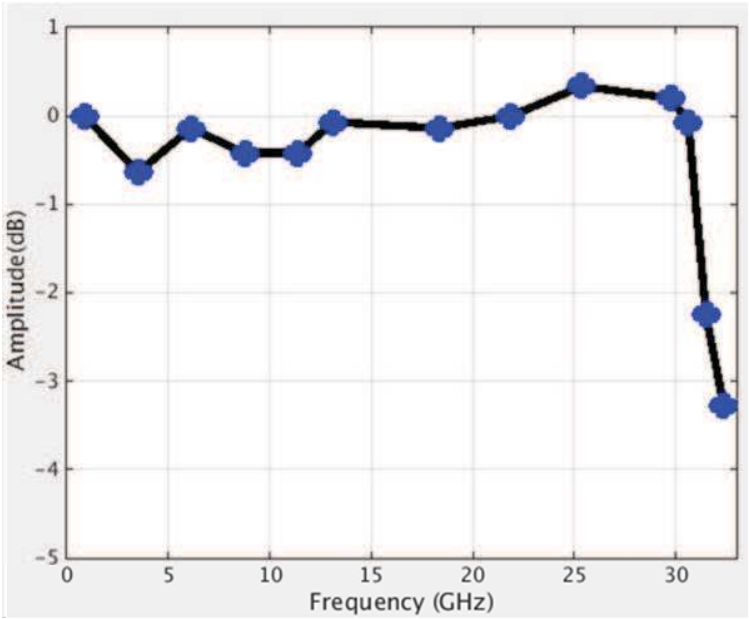

Figure 4.10. Measured output amplitude vs. input sine frequency of the interleaver.

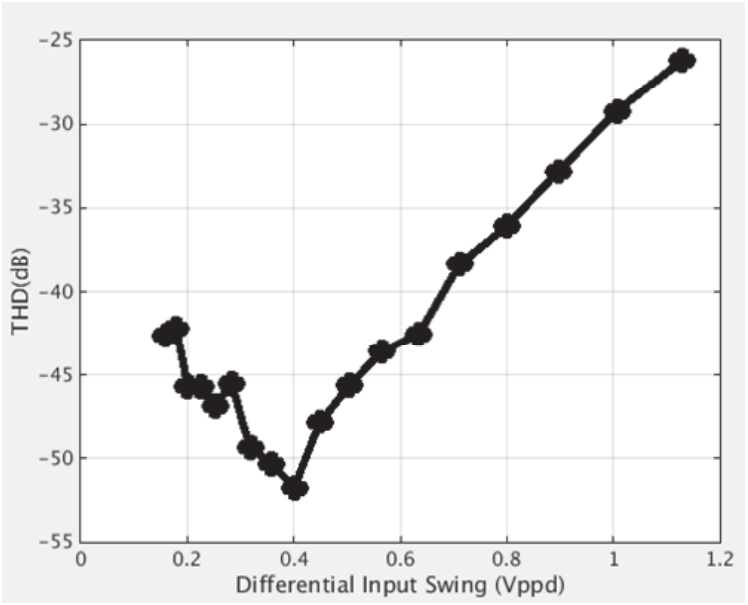

Figure 4.11. Measured THD vs. input signal swing of the interleaver.

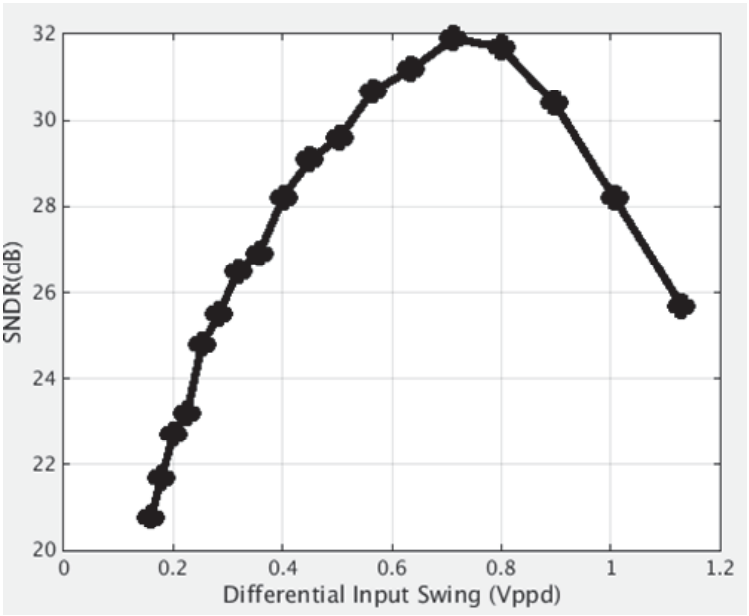

Figure 4.12. Measured SNDR vs. input signal swing of the interleaver.

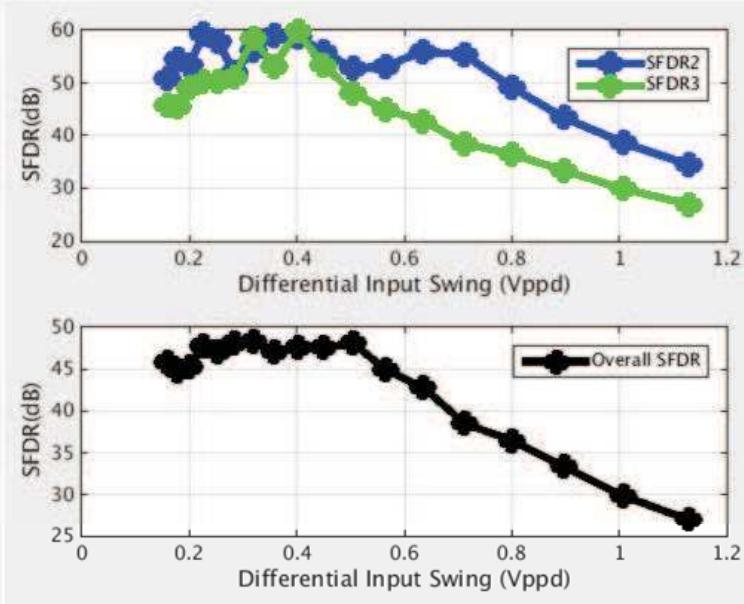

Figure 4.13. Measured SFDR vs. input signal swing of the interleaver.

Table 4.2. Comparison of 64 GS/s Interleaver with the State of the Art.

	TCAS II 2016 [51]	IMS 2012 [10]	JSSC 2014 [9]	This work
f_S(GS/s)	25	50	50	64
BW (GHz)	55	40	27	32
Input Range (V)	0.4	1	1.8	0.4
THD@Fin (dB@GHz)	-32@50	-36.5@25	-29.5@15	-41.5@32.4
Power (mW)	73	1850	1200	372
Area (mm^2)	0.03 (active)	1.8	0.73	0.28 (active)
Process	28 nm CMOS	700 nm InP	250 nm InP	28 nm CMOS

A 1.75 GHz input signal is sampled by 16-way 4 GS/s samplers composed 64 GS/s sampler. The spectrum of one channel outputs of 4 GS/s samplers is shown in Figure 4.6. The SFDR and THD are observed as 48.7 dB and -45.9 dB, respectively. The SNDR performance is limited by the 5.5-bit ENOB of the oscilloscope (Tektronix DPO 73304D). Figure 4.7 shows the output spectrum of one channel output buffer with Fin=14.9 GHz. The SFDR and THD are observed as 49.2 dB and -49.3 dB, respectively. Figure 4.8 shows the output spectrum of one channel output buffer with Fin=32.4 GHz. The SFDR and THD are observed as 43.4 dB and -41.5 dB, respectively. Figure 4.9 showss the plot of THD, SNDR and SFDR vs. input sine frequency of the interleaver. Because of the linearity improvement by switched output buffer and parametric amplifier, the THD is < -38.2 dB up to 32.5 GHz. Figure 4.10 shows the measured output amplitude vs. input sine frequency of the interleaver. The measure 3-dB BW is 32 GHz.

The performance of THD, SNDR and SFDR are also investigated as the input signal swing changes. Because an additional driver stage Buf_{meas} with 50Ω output impedance is needed, the linearity of the entire interleaver will also be limited by that driver stage. Figures 4.11, 4.12 and 4.13 show the measured THD, SNDR and SFDR vs. input signal swing. The SNDR performance is limited by the 5.5-bit ENOB of the oscilloscope. Because the output 50Ω buffer will limit output swing, the maximum input swing of the interleaver is a little smaller than that of our ADC. To achieve the good performance of SNDR and ENOB, the linearity of the ADC should be good enough, meaning a low THD is desired. Table 4.2 shows the performances comparison of the proposed interleaver with the state of art. Our 64 GS/s interleaver achieves the best performance of THD for the same input frequency, compared with the other three works.

4.4. Conclusion

This section presents a 64 GS/s time-interleaved track-and-hold amplifier. The techniques of ESD protection on common-mode input node, input buffer with dual power supply and parasitic sampling capacitors are utilized to achieve 32 GHz bandwidth. The switched output

buffer and parametric amplifier are proposed to improve the linearity and maintain the large enough signal swing for the requirement of the signal-to-noise ratio of the following quantization. The measured THD <-38.2 dBc up to 32.4 GHz input, smaller than those measured at high input frequency of previously reported THA [2, 9, 10, 51].

Chapter 5

CONCLUSION

5.1. Results

This thesis presented the ADC design details that can achieve the requirements of sampling rate, bandwidth and ENOB imposed by 112 G/224 Gb/s digital coherent receivers. Several analog circuit techniques and digital circuit techniques are proposed and utilized to overcome the design challenges and improve the performance. Those techniques include parametric T/H amplifier, switched sub-channel, multiple bandwidth enhancement techniques, curve fitting based foreground comprehensive digital calibration for intra-channel and inter-channel mismatches. Because of those innovative methods, this 56 GS/s 8-bit ADC in 28 nm technology achieves nearly the same performance of SNDR with the same input frequency of the an ADC in 14 nm FinFET technology [23], but has a higher bandwidth of 31.5 GHz. Note that the 3D 14 nm FinFET technology can provide up to 55% high device performance compared to 28 nm technologies [14].

This thesis proposed the techniques that make contributions to the performance improvement of BW and ENOB. The measured results of this ADC in 28-nm CMOS even achieved the competitive performance of BW and ENOB compared with the ADC implemented in a more advanced 14-nm FinFET technology.

5.2. Outlook

Because of the ever-increasing demands of high-speed data services, the needs for capacity and bandwidth in the metro, regional and long-haul optical communication systems never stops. With the coherent technology, the system capacity is a product of three dimensions: the number of multilevels, the number of subcarriers, and the symbol rate. WDM systems

today primarily use the wavelength band of 1530-1625 nm, because of the inherent lowest loss and excellent optical amplifier in that region [39]. Given the fix optical wavelength band, possible solutions to increase the data rate is to increase the symbol rate and utilize high order modulation formats. On March 2017, Fujitsu announced that it released a 64 Gbaud/s DP-64QAM integrated coherent receiver for use in single carrier 600 Gbps coherent transmission applications [13], which is the world's fastest recevier so far. In future, such ADCs for high order modulation formats will be required for higher-speed short-haul links, where low power becomes more important because the number of these links is large. Fortunately, the 3D 14 nm FinFET technology can provide up to 55% higher device performance and 60% lower total power compared to 28 nm technologies [14]. Furthermore, the 3D 7 nm FinFET transistor with EUV (Extreme Ultraviolet Lithography) compatibility can deliver $>$ 40% performance boost or $>$ 60% total power reduction, compared to 14 nm foundry FinFET offerings [15]. Overall, ADCs with higher sampling rates far beyond 100 GS/s and low power consumption in the most advanced technolgy seem to be possible to realize, however, circuit design techniques are needed to overcome various design challenges and achieve the required performance of bandwidth and ENOB.

Based our existing work and proposed methods, the recommended future work is to build a higher sampling rate ADC by using 10-nm or 7-nm FinFET technology. It can be expected that some ADC implemented in such technology will soon appear in the near future.

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