A 57.9-to-68.3GHz 24.6mW Frequency Synthesizer with In-Phase Injection-Coupled QVCO in 65nm CMOS

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Under the influence of increasing demand for high-data-rate communication systems such as 60GHz band application, the requirements of PLLs keep getting higher. In an mm-wave direct-conversion transceiver, the quadrature LO signals generation is challenging. The conventional techniques to generate quadrature LO signals suffer from many problems. The method of using divide-by-2 divider after a VCO with double LO frequency is popular in multi-GHz designs, but it is difficult to be realized in mm-wave frequency. Employing passive *RC* complex filter is another way to generate quadrature signals, but high power is required to compensate its loss. The conventional parallel-coupled QVCO seems to be a good choice for mm-wave application. However, this approach suffers from poor phase noise. This work presents a fully integrated 57.9-to-68.3GHz frequency synthesizer, which employs an in-phase injection-coupled QVCO (IPIC-QVCO) to produce low phase noise quadrature signals with low power.

The block diagram of the frequency synthesizer is shown in Figure 1. It comprises a QVCO, a low-power divider chain, a PFD, a programmable self-correcting low spur charge pump (CP) and an integrated 2^{nd}-order LPF. The schematic of QVCO is also depicted in Figure 1. Digitally-controlled variable resistor *R*, instead of transistor current source, is used in order to reduce flicker noise. By adopting 3 binary-weighted digitally-controlled capacitors and an A-MOS varactor, the QVCO has 8

overlap bands to get a large tuning range and low sensitivity. The coupling network is composed of 4 diode-connected transistors linked back-to-back.

From the point view of injection locking, the in-phase coupling in QVCO lowers both white and flicker noise, and improves quadrature accuracy [1]. Many techniques achieve in-phase coupling by introducing a phase shifter, but the phase shifter usually causes extra power and noise, and it is mostly frequency-dependent. Since the quadrature signals always exist in QVCO inherently, in this work, the in-phase coupling is realized by utilizing the quadrature signals in QVCO. The operation of the diode-connected transistor M_{C2} in the coupling network in Figure 1 will be analyzed first in order to understand the in-phase coupling in this QVCO. When the QVCO is operating, the phase of drain and source voltages of M_{C2} are 0 and -π/2 respectively, as shown in Figure 2(a). Thus, the phase of gate-source voltage V_{gs} is π/4. M_{C2} turns on when V_{gs} is larger than the threshold voltage V_t. Since the conduction angle is less than π, M_{C2} works in Class C operation mode. The phase of drain-source current I_{C2} is also π/4. Similarly, the phase of M_{C1} drain-source current I_{C1} is 3π/4. The current I_{inj}, injected into the node I+ from the coupling network, is equal to I_{C1} - I_{C2}, Therefore, the injection current I_{inj} is in-phase with the tank current I_{tank}, as shown in Figure 2(b). The proposed IPIC-QVCO offers several advantages over conventional QVCO topologies. Firstly, the injection current is injected in-phase with the tank current, so both phase noise and phase error are reduced. Secondly, this coupling network does not surfer from the frequency-dependent limitation in *RC* or *LC* coupling schemes such as superharmonic coupling or magnetic coupling [2]. Finally, the coupling network consumes no dc current and thus contributes negligible noise, and the total power consumption also decreases. Compared with a conventional parallel-coupled QVCO (with coupling factor of 0.5) with the same power and device size, the simulated phase noise of the proposed QVCO has more than 10dB improvement at 1MHz offset frequency.

The divider chain consists of a dynamic CML (DCML) divide-by-4 divider, an injection-locked divide-by-4 frequency divider (ILFD) and a programmable true single-phase-clock (TSPC) divide-by-27/28/29/30 divider. Figure 3 shows the schematics of the DCML and ILFD dividers. By using these divider topologies, the low power and small area can be achieved simultaneously. In this DCML divider, the switches of the same input clock are merged compared with the DCML divider in [2]. This modification provides some improvements in both maximum operating frequency and locked bandwidth due to smaller *RC* time constant and larger oscillation amplitude. In order to balance the output loadings, all the 8-phases outputs of DCML divider serve as the inputs of ILFD. Each two adjacent phase inputs of ILFD are added through transistors to become quadrature inputs. The multi-phase injection can improve the locking range of the divide-by-4 ILFD. The bias voltage V_{bp1} and V_{bp2} can be tuned externally to cope with the PVT variation.

The programmable self-correcting low spur CP, shown in Figure 4, is modified from [3]. The VI-converter, containing a rail-to-rail amplifier, senses the voltage difference between V_1 and V_2, and corrects the mismatch of charge/discharge current. Compared with [3], two measures are taken in order to reduce spurious level. Firstly, the UP/DN switches are moved to the source of current sources to eliminate the clock feedthrough and charge injection. Secondly, V_1 can be regarded as V_2 after a unity-gain amplifier, as shown in the simplified equivalent schematic in Figure 4. The VCO control voltage V_{ctrl} is connected to V_1, instead of V_2. The benefit is that the ripple in V_2 caused by reference clock can be filtered by this follower as long as its bandwidth f_{amp} is less than reference frequency f_{ref}. On the other hand, f_{amp} is designed to be significantly larger than the PLL loop bandwidth f_{LBW}, to avoid the impact on the system loop characteristics and stability. In this design, f_{LBW}, f_{amp} and f_{ref} are about 0.5, 40 and 135MHz, respectively. Figure 4 depicts the simulated

waveforms of V_{ctrl} when it is connected to V_1 and V_2 respectively. As expected, the amplifier does not interfere in the locking process, and the ripple of V_{ctrl} connected to V_1 is much smaller. The measurement results show no observed reference spurs when the PLL is locked.

The frequency synthesizer is implemented in a 65nm CMOS technology. Figure 7 shows the die micrograph of the standalone QVCO and the complete PLL, which occupy 0.26×0.15 and 0.32×0.60mm^2, respectively. The PLL consumes 24.6mW (not including open drain output buffers) from a 1.2V supply, of which, about 11.4mW, 12.7mW and 0.5mW are consumed by QVCO, divider chain and other blocks, respectively. The 8 bands of QVCO cover a frequency range of 57.88 to 68.33GHz, i.e. 16.6% around centre frequency. As depicted in Figure 5(a), the measured QVCO phase noise for a 62.66GHz carrier are -94.2 and -115.0dBc/Hz at 1 and 10MHz offset, respectively. The FOM and FOM_T are -179.6 and -184.0dBc/Hz at 1MHz offset, respectively. The phase and amplitude errors are measured by down-converting the quadrature signals to about 250MHz. The phase error is less than 0.7° and the amplitude error is less than 0.6dB across different dies. The operation range of PLL is from 57.9 to 68.3GHz. When reference input f_{ref} = 135MHz, the PLL can be locked to the 4 frequencies of IEEE 802.15.3c 60GHz standard. The phase noise of PLL, shown in Figure 5(b), is -91.0dBc/Hz at 1MHz offset when carrier frequency is 62.64GHz. Since the reference spurs are buried in the noise floor, the spurious level is less than -45dBc. The measured QVCO and PLL performance are summarized and compared with state-of-the-art works in Figure 6.

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Captions:

Figure 1: The frequency synthesizer and QVCO.

Figure 2: (a) Waveforms in a coupling transistor and (b) the current phasor relationship in QVCO.

Figure 3: The DCML and ILFD ÷4 dividers.

Figure 4: The CP with simulated waveforms of V_{ctrl}.

Figure 5: Measured phase noise of (a) QVCO and (b) PLL.

Figure 6: Measured QVCO and PLL performance summaries and comparisons with state-of-the-art works.

Figure 7: Die micrograph of the standalone QVCO and the complete PLL.

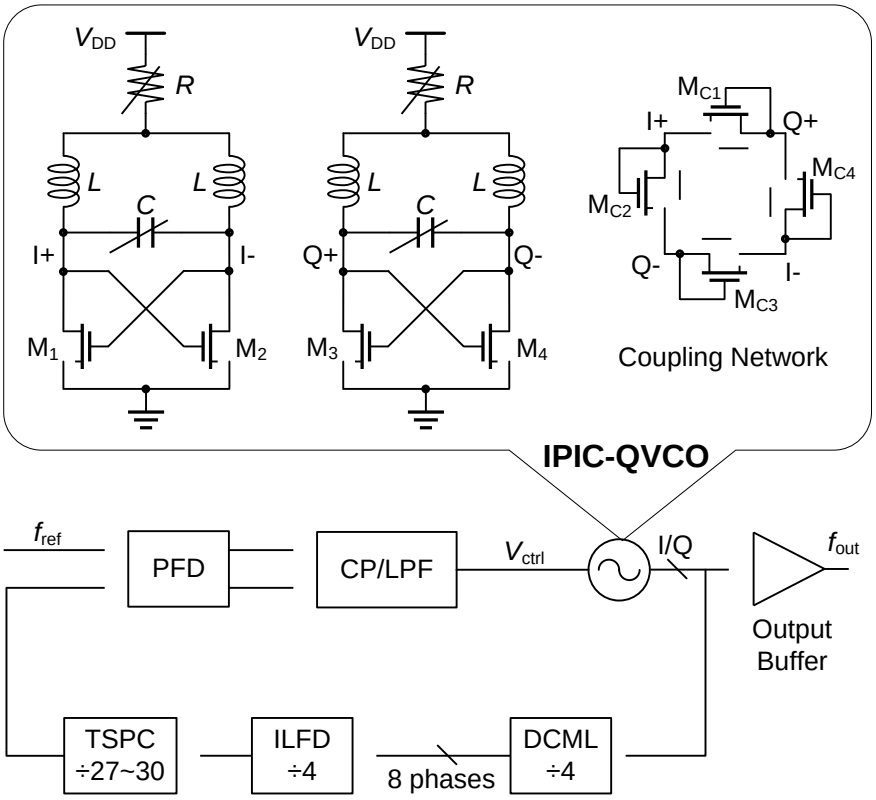


Figure 1: The frequency synthesizer and QVCO.

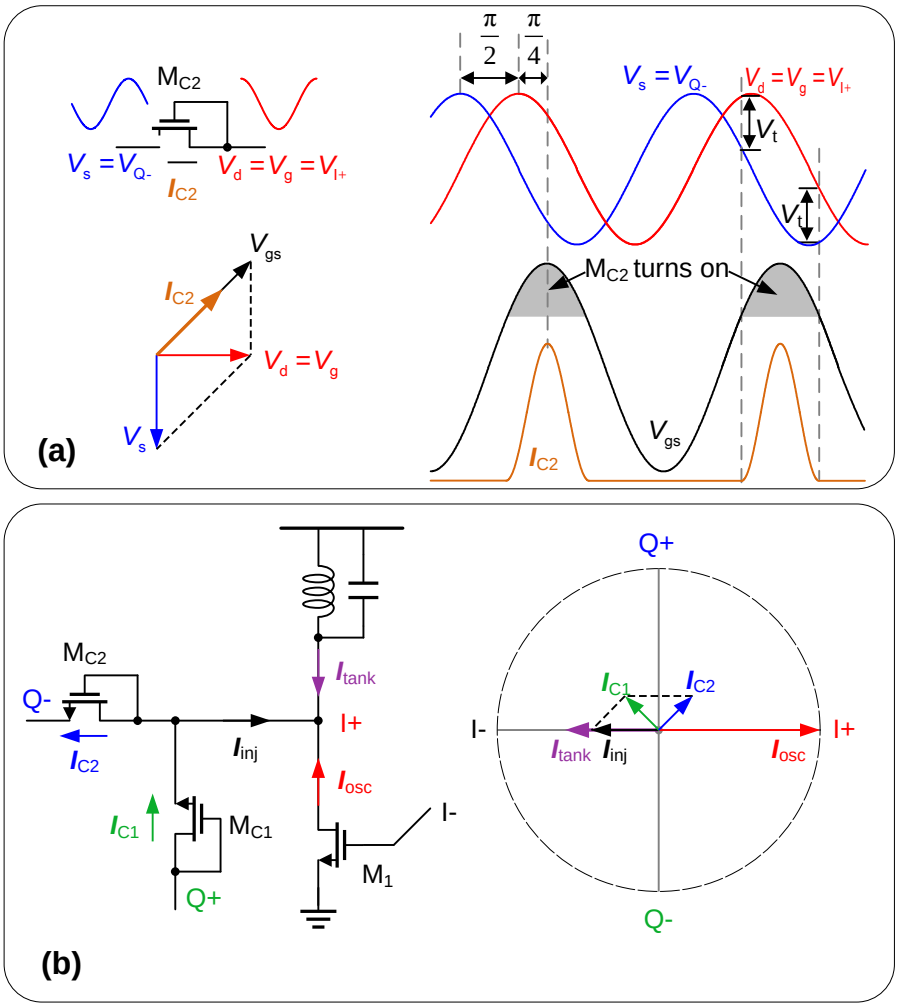


Figure 2: (a) Waveforms in a coupling transistor and (b) the current phasor relationship in QVCO.

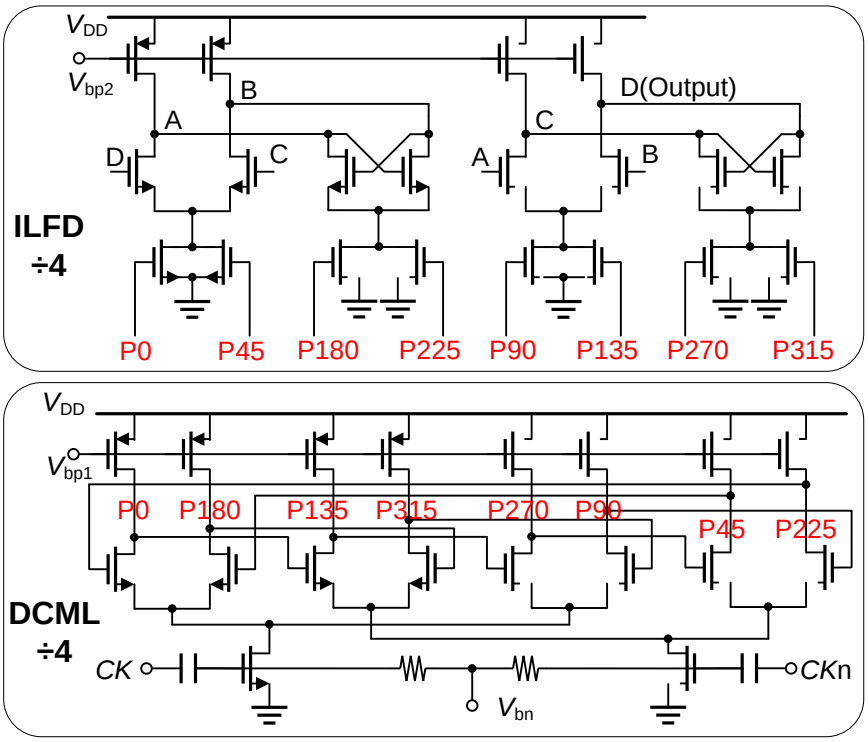


Figure 3: The DCML and ILFD ÷4 dividers.

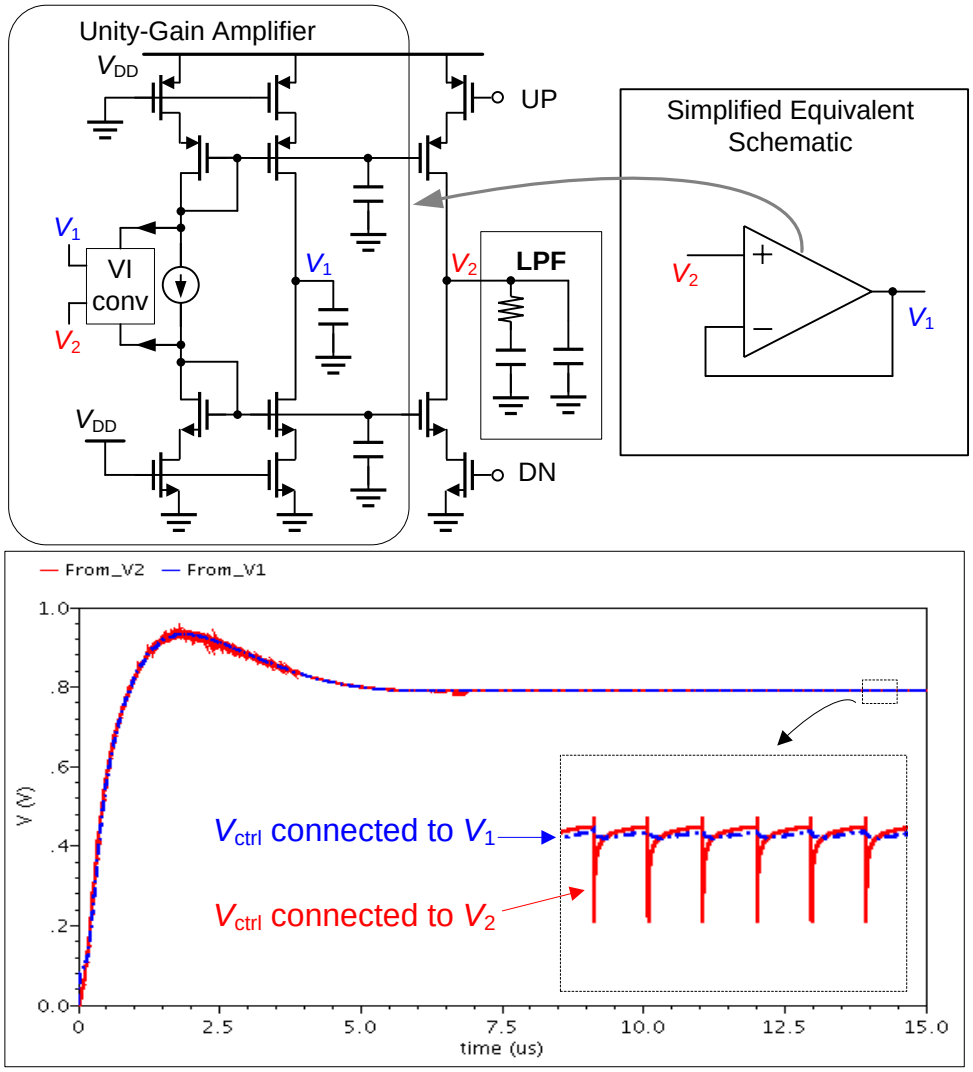


Figure 4: The CP with simulated waveforms of V_{ctrl}.

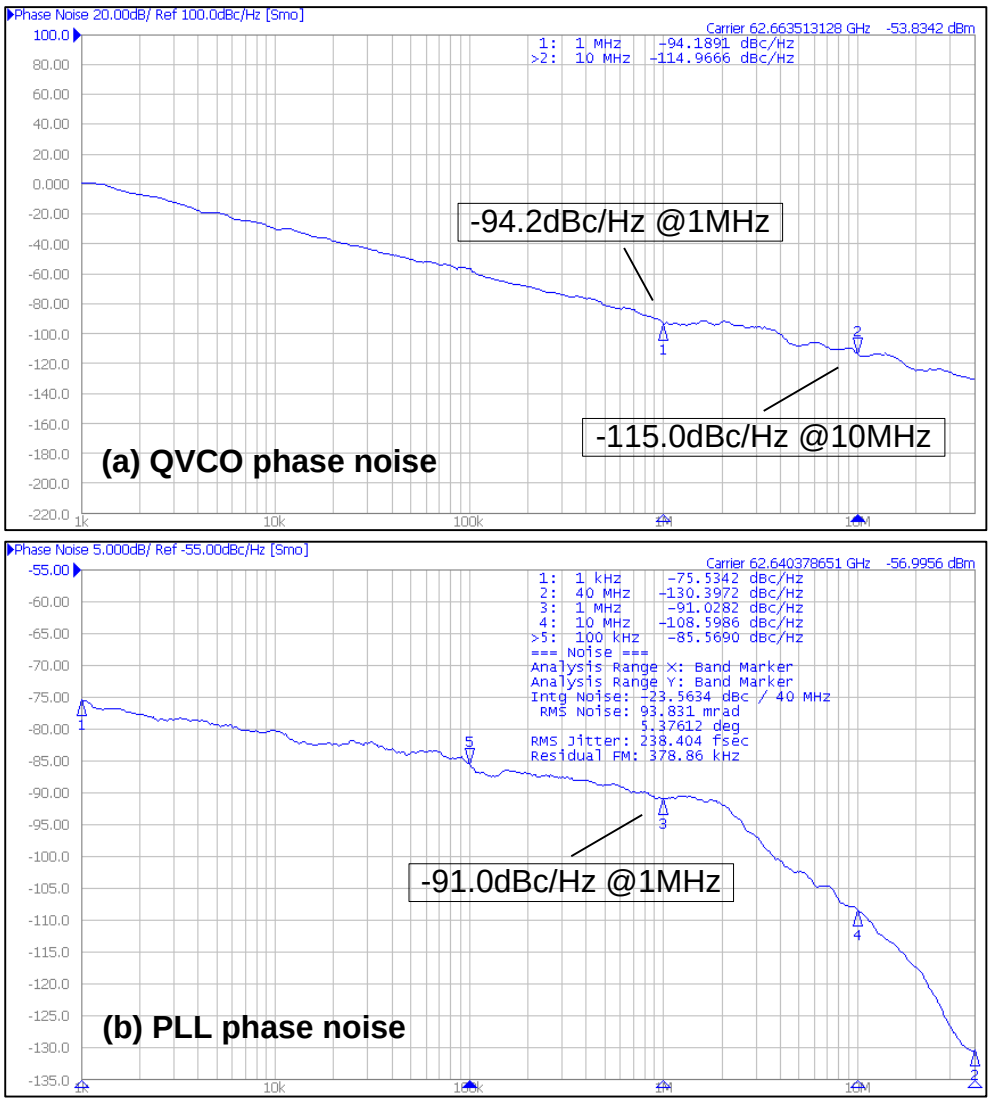


Figure 5: Measured phase noise of (a) QVCO and (b) PLL.

60GHz Quadrature VCO Comparison								
Ref.	Tech. (nm)	V_{DD} (V)	Operating Range (GHz)	P.N.@1MHz (dBc/Hz)	FOM* (dBc/Hz)	FOM_T** (dBc/Hz)	Phase Error	Power (mW)
[2]	65 CMOS	1.0	56.0~60.4 (7.6%)	-95/-97	-176.9/ -178.9	-174.6/ -176.6	<1.5°	22
[4]	45 CMOS	1.1	57~66 (14.6%)	-75***	-156.3	-159.6	n.a.	28
This work	65 CMOS	1.2	57.88~68.33 (16.6%)	-94.2	-179.6	-184.0	<0.7°	11.4

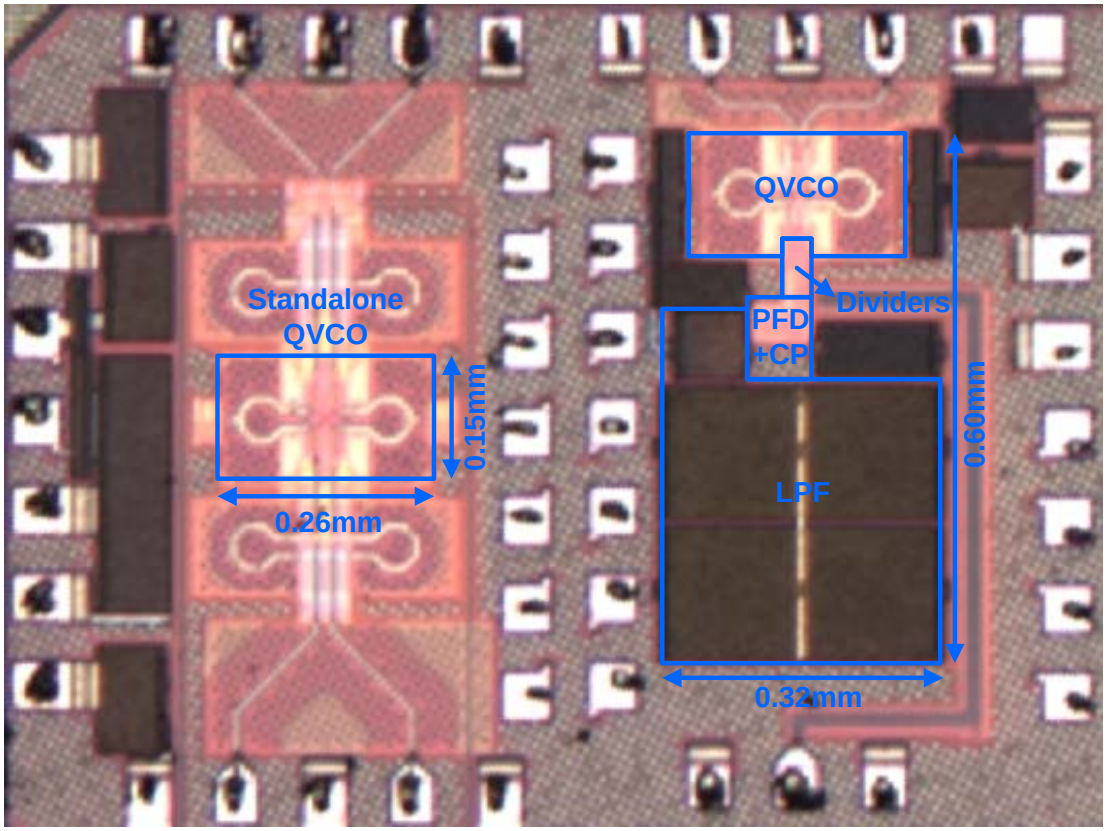
* FOM = P.N. – 20log($f_0/\Delta f$) + 10log(Power/1mW)

** FOM_T = FOM – 20log(% of Operating Range/10%)

*** PLL phase noise

60GHz Quadrature PLL Comparison								
Ref.	Tech. (nm)	V_{DD} (V)	f_{ref} (MHz)	Operating Range (GHz)	P.N.@1MHz (dBc/Hz)	Reference Spur (dBc)	Topology	Power (mW)
[5]	90 CMOS	0.7/ 1.2	117	59.6~64.0 (7.1%)	-72.5	-23	30GHz PLL + 60GHz Hybrid	76.3
[6]	65 CMOS	1.0/ 1.2	36	54~61 (12.2%)	-94.2	n.a.	20GHz PLL + 60GHz QILO	80.9
[4]	45 CMOS	1.1	100	57~66 (14.6%)	-75	-42	60GHz QPLL	78
[7]	40 CMOS	1.1	20000	55~66 (18.2%)	<-96	n.a.	60GHz QILO	112
This work	65 CMOS	1.2	135	57.9~68.3 (16.5%)	-91	<-45	60GHz QPLL	24.6

Figure 6: Measured QVCO and PLL performance summaries and comparisons with state-of-the-art works.



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