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Eduardo V. P. Anjos[*†], Marzieh SalarRahimi[*†], Robert Rehammar[‡**] Dominique M. M.-P. Schreurs[*], Guy A. E. Vandenbosch[*], Marcel Geurts[†]

[*]*ESAT-TELEMIC, KU Leuven, Leuven, Belgium*; e-mail: {name}.{lastname}@kuleuven.be

[†]*NXP Semiconductors, Nijmegen, The Netherlands* e-mail: {name}.{lastname}@nxp.com

[‡]*Bluetest AB, Sweden*. e-mail: {name}.{lastname}@bluetest.se

[**]*Department of Electrical Engineering, Chalmers University of Technology, Sweden*

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***Index Terms*—5G, active antenna, antenna tile, hybrid beamforming, phased-array.**

I. Introduction

Antenna arrays with Hybrid Beamforming (HBF) are expected to be one of the main enablers to deliver the two-fold increase in data-rate, combining advances in both deep-integrated phased-array transceivers and massive MIMO [1].

When implementing HBF arrays, the use of a tile approach [2]–[4] is very beneficial. Using a tile to implement the analog beamforming sub-array in a large array with HBF architecture allows the system to be flexible and scalable, as each tile operates as a stand-alone device. The flexibility given through the tile configuration can be used to explore different architectures beyond simulation. For example, the higher spectral efficiency benefits of sparse arrays could be explored on a sub-array level [5].

Another advantage of the tile approach is the effort reduction to test and characterize the array. It is greatly simplified to the tile level, which can potentially increase manufacturing yield.

In this work, a scalable antenna tile system is presented, with a 2×2, 0.5λ inter-element spacing (IES) sub-array per tile. The presented tile can operate both as transmitter and receiver and is manufactured using a low-cost standard PCB technology. The overall system configuration was conceived to allow full scalability of the array, from antennas to DC supply, including also thermal management, making it an innovative flexible solution at mm-wave frequencies. To verify the tile performance, over-the-air measurements were performed in a Reverberation Chamber (RC), achieving up to 1.6 GHz bandwidth over a central frequency of 27.8 GHz.

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II. Tile System and Design

In this section we introduce the tile system and its main parts, mainly motherboard and the antenna tile itself. The core concept here is the ability to scale the system according to the application requirement, whether emulating receiving nodes using a single tile or base-stations using several units.

A. System Overview

The system is pictured in Fig. 1. It is composed mainly by the antenna tiles, with analog beamforming capabilities, and a motherboard, to deliver DC and control signals to the tiles.

The tiles are the core of the system, consisting of the radiating elements, beamforming chip, and DC and RF connectors. Each tile has its own RF connector, allowing its usage on Hybrid Beamforming (HBF) arrays. If analog beamforming (ABF) is desired, a power splitter/combiner can be used prior to the tiles. This flexibility allows the experimental study on array architectures.

The choice for a motherboard was made to provide signal integrity for the digital control, and equal voltage levels between the modules. The digital control is performed through a serial bus, which can be cascaded with other boards if needed, as shown in the figure. This property allows the system to be as large as required.

The proposed tile system is scalable in every aspect, in order to allow a seamless increase/decrease in the number of elements. An often overlooked aspect is the thermal management, and it was handled here by using a heat-sink which fits within the tile boundary. If needed, an axial fan can be used to provide extra cooling.

B. Tile Design

Each tile has a 2×2 antenna array with an analog beamforming chip per tile. To obtain extra space to fit the connectors, the tile was elongated on one of its edges and the sub-array was placed at one end of the board. This compromise limits the possible array architectures, namely limited to a $4 \times N$ configuration.

The RF signal goes via cables to the SMPM connectors, and is directed to the ABF chip by a CPW line. The chip is controlled using a serial bus through the motherboard, which is connected using a DF52-8S connector from Hirose. With

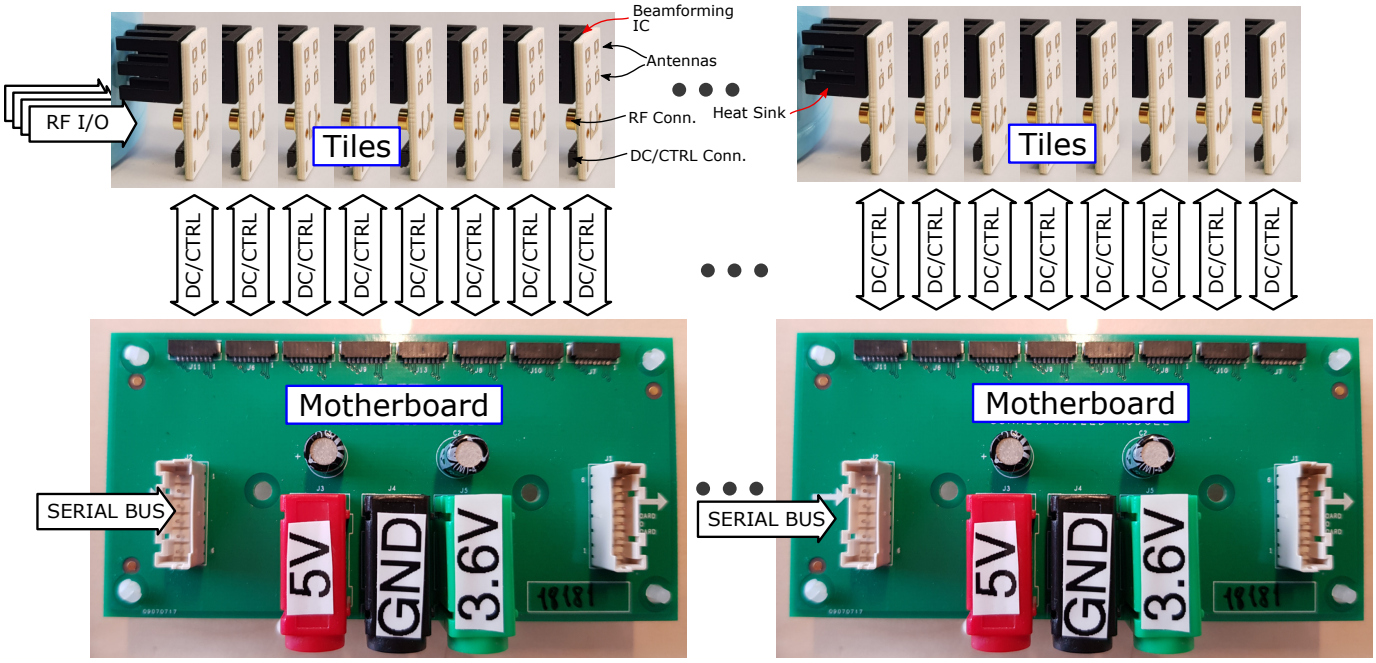

Fig. 1. Tile antenna system diagram.

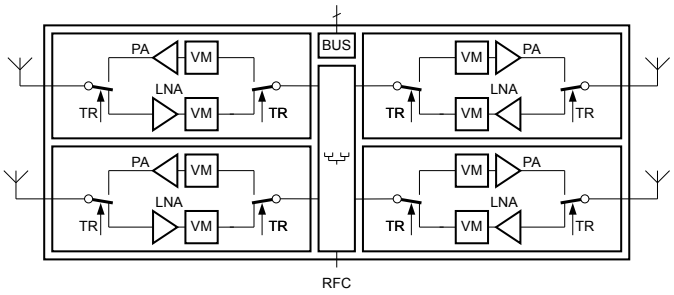

Fig. 2. Analog beamforming chip block diagram.

Fig. 3. Reverberation chamber OTA measurement setup using Bluetest RTS65. All elements within chamber, including PC, were taking into account during calibration.

0.8 mm pitch, it fits well within the tile width of 10 mm. The final tile size is 10×23 mm^2.

The radiating elements are proximity-fed patch antennas. They were designed taking into account manufacturing limitations from low-cost PCB technology, using coarse vias ($250\ \mu m$) and only four metal layers. More details about the antennas can be found in [6].

C. Analog Beamforming Chip

The powerhouse of the tile is the analog beamforming integrated circuit from NXP and its block diagram is pictured in Fig. 2. The analog beamformer has a 1:4 splitter/combiner and four individually controlled channels, where each channel utilizes a vector modulator to achieve a phase shifting resolution of 6 bits ($5.625°$) with amplitude resolution of 0.4 dB while delivering up to 20 dB gain in Tx mode. It operates in both Tx and Rx mode, allowing the tile to be bi-directional. The control of the chip is performed through a serial bus.

III. Reverberation Chamber Characterization

In order to validate the proposed tile module, over-the-air measurements were performed using Bluetest RTS65 reverberation chamber. The tile was evaluated in both Tx and Rx modes to show its bi-directional capabilities. The OTA measurement setup is pictured in Fig. 3.

A. Total Radiated Efficiency (TRE)

In a rich isotropic multi-path (RIMP) environment, the main measurement performed was the total radiation efficiency (TRE) of the tile, which is defined by

$$TRE = TRP - P_{input} \tag{1}$$

where TRP is the total radiated power. To obtain the DUT TRE, the system is first calibrated by a reference antenna with known radiation efficiency as described in [7]. The DUT

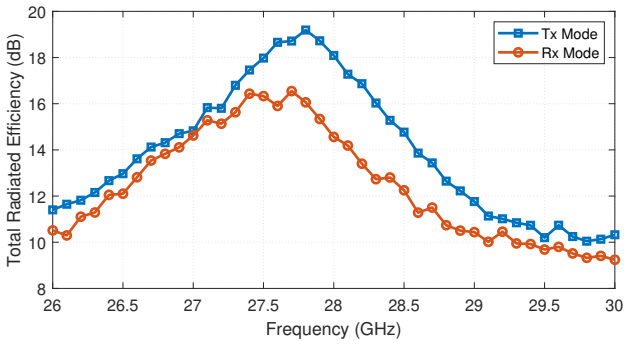

Fig. 4. Measured TRE vs. frequency for Tx and Rx mode.

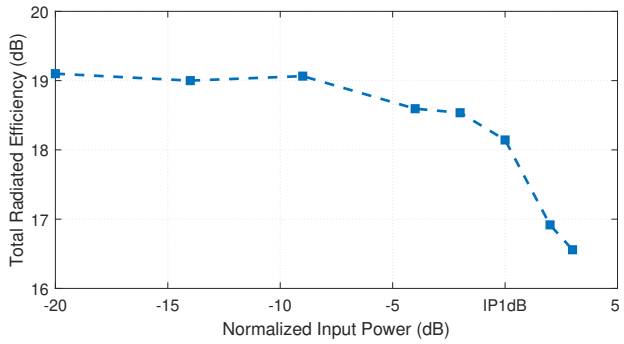

Fig. 5. Measured TRE vs. Input power in Tx mode at f= 27.9 GHz, with input power normalized w.r.t. IP1dB.

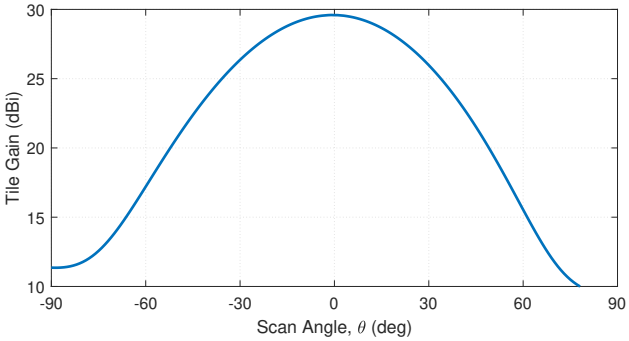

Fig. 6. Simulated broadside antenna pattern with gain estimated from TRE measurement @ 27.8 GHz.

TRE is then obtained by the ratio between the average transfer function of both scenarios.

The tile TRE was measured for different frequencies and different input power levels, and the average TRE versus frequency for both Tx and Rx are pictured in Fig. 4. Notice here that the TRE only takes into account the transfer function between RF input and output power, with DC power not included in the measurement definition. Due to the gain delivered by the ABF chip, the TRE can be above 0 dB.

Although a measured TRE above 0 dB seems unusual, it gives insight over the system RF gain, taking into consideration all amplification and losses from input to output while averaging out the directivity of the antenna. In the case of the tile (or phased arrays in general) the TRE provides an average RF gain per element, accounting all losses from splitting and combining (over-the-air). Therefore, this measurement is an excellent tool to analyze the system bandwidth.

From Fig. 4, a 3-dB bandwidth of 1.2 GHz around a central frequency of 27.8 GHz was obtained in Tx mode, while in Rx mode a slightly larger 1.6 GHz bandwidth around the central frequency of 27.6 GHz was obtained. The difference in TRE between modes is due to a slightly higher gain in Tx mode. The achieved bandwidth is more than sufficient to comply with the 5G NR standards [8].

B. TRE vs. Input Power characterization

Since there are no ports available between the RF front-end and the antenna, characterization of the RF front-end must now be performed OTA. One important metric that used to be possible to measure directly on the front-end, is the 1 dB compression point and the front-end behaviour around that point. To characterize the non-linear behavior, the TRE was measured with respect to different input power levels. The results can be seen in Fig. 5. [1]

All measurements were performed using a VNA. To accurately measure the absolute power level, the regular VNA S-parameter calibration was complemented with a power calibration step. The power calibration consists in using a high-accuracy thermal power meter, connecting it to the VNA and recording the actual power for different VNA power level settings.

As the input power approaches the Input-referred 1dB compression point (IP1dB) level, the chip starts to go into compression, dropping the TRE. For input power levels much below the IP1dB, the change in power does not affect the TRE.

C. RIMP and Radiation Patterns

Due to the multi-path nature of the RC measurements, the antenna radiated power is averaged out over every direction, and directivity information is lost. However, using the simulated gain of the radiating elements, the radiation pattern of the complete system can be estimated [9] using

$$G_{\text{tile}}(\theta) = TRE + G_{\text{sim}}(\theta) \tag{2}$$

This assessment is particularly useful as the TRE assesses all possible losses within the system and displays them over the gain information from the simulation. Fig. 6 shows the simulated radiation pattern of the tile, estimated from (2), at 27.8 GHz. The radiation pattern of the passive array was simulated using CST. The tile shows a maximum gain of 29.5 dBi at 27.8 GHz.

IV. Conclusion

This work presented a 5G-enabled, fully scalable active antenna tile system. The tile was designed, fabricated, and

[1]In order to preserve sensitive data, all absolute power values were normalized with respect to the compression point, which will not be disclosed.