5.4: A 5GHz CMOS Transceiver for IEEE 802.11a Wireless LAN

David Su, Masoud Zargari, Patrick Yue,
Shahriar Rabii, David Weber, Brian Kaczynski,
Srenik Mehta, Kalwant Singh, Sunetra Mendis,
and Bruce Wooley[1]

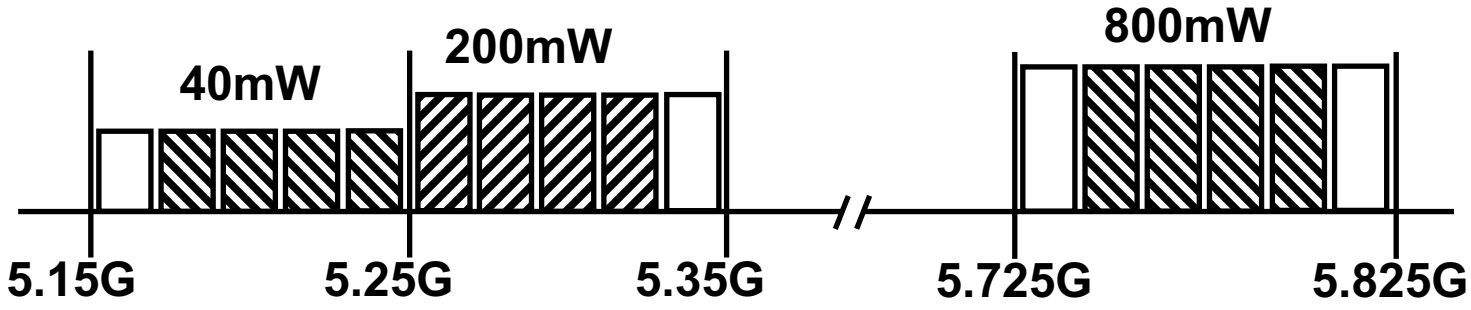
Atheros Communications, Sunnyvale, California
[1]Stanford University, Stanford, California

Outline

- Introduction: 802.11a Wireless LAN
- Architecture
- Radio Design
  - Transmitter
  - Receiver
  - Frequency Synthesizer
- Summary

IEEE 802.11a WLAN

- **Frequency: 5 GHz UNII (Unlicensed National Information Infrastructure)**



- **Total UNII Bandwidth: 300 MHz (> IEEE 802.11b)**
- **Modulation: OFDM (Orthogonal Frequency Division Multiplexing) + BPSK / QPSK / 16QAM / 64QAM**
- **Data Rate: 6 - 54 Mbps**

Spectral-Efficient Modulation

- 64-QAM (Quadrature Amplitude Modulation)
  - — Large signal to noise ratio > 30dB
    - Phase noise
    - I/Q mismatch
- OFDM (Orthogonal Frequency Division Mux)
  - — Large peak to average power ratio of $\sqrt{52}$ or 17dB
    - TX: large power backoff
    - RX: large dynamic range
    - Some signal clipping can be tolerated

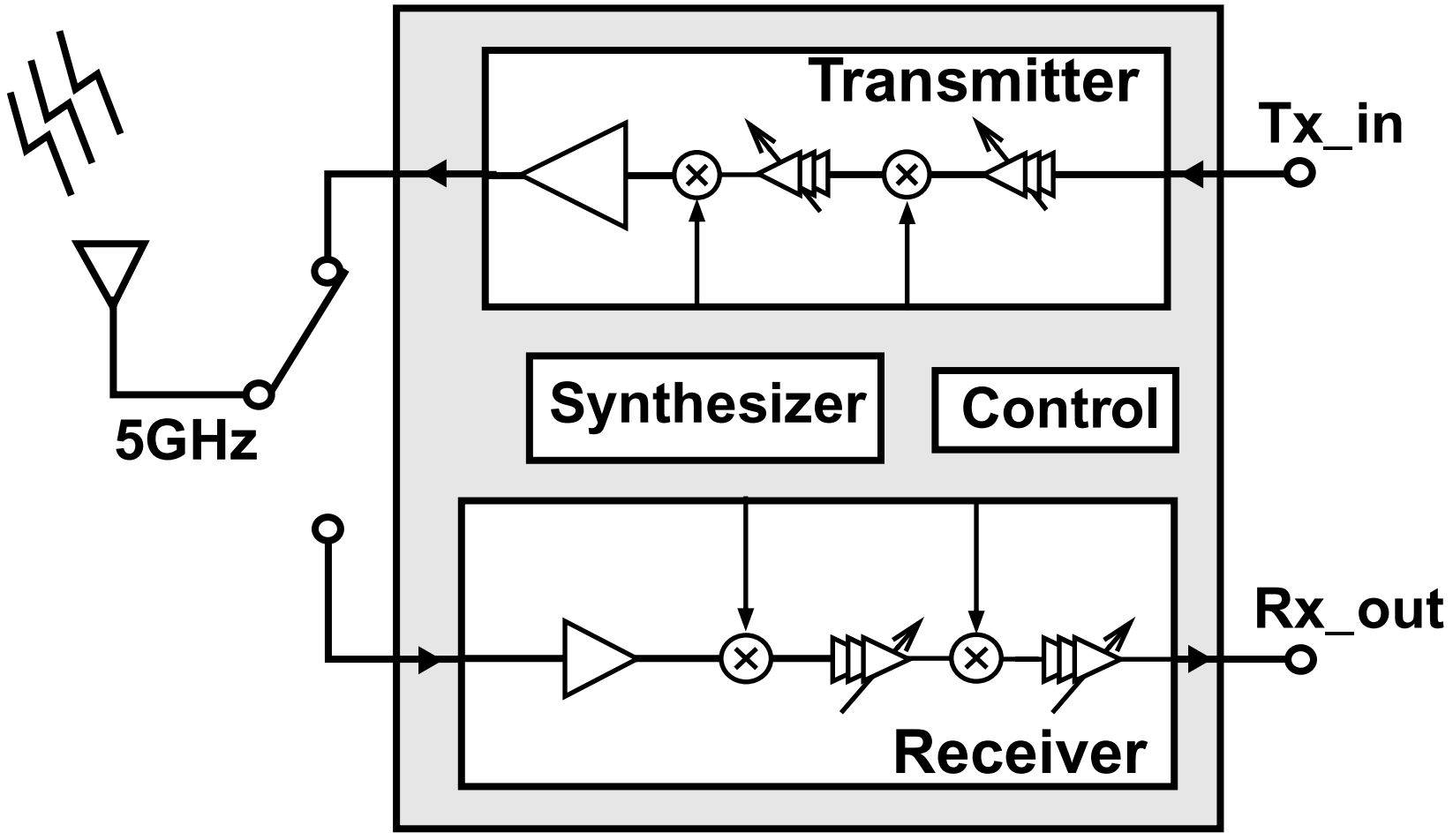
→ Requires High Linearity

Architecture

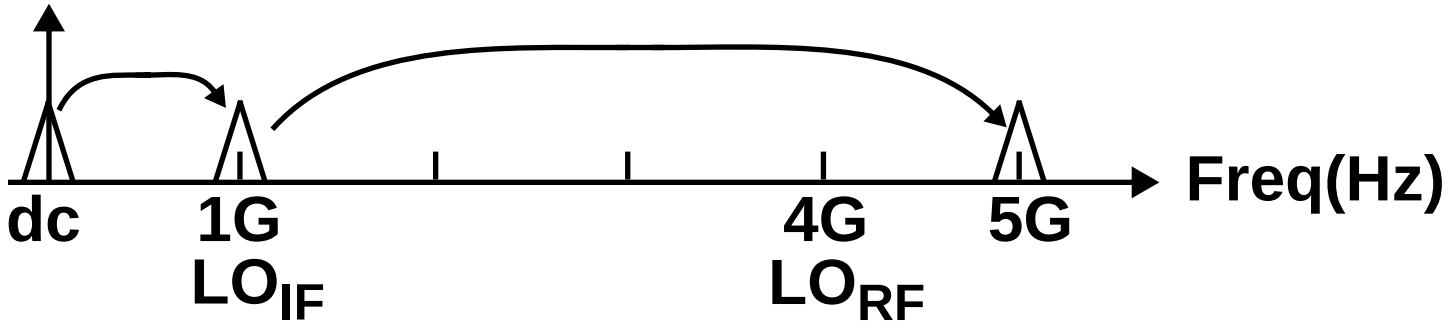
Architecture	+	–
Direct Conversion	- No off-chip IF filter - Single synthesizer	- LO leakage - LO pulling - Quadrature LO_{RF} - DC offset
Traditional Superheterodyne	- Low LO leakage - Weak LO pulling - No quadrature LO - Design flexibility	- Off-chip IF filter - Two synthesizers

→ **Dual conversion with 1GHz sliding IF**

Radio Transceiver

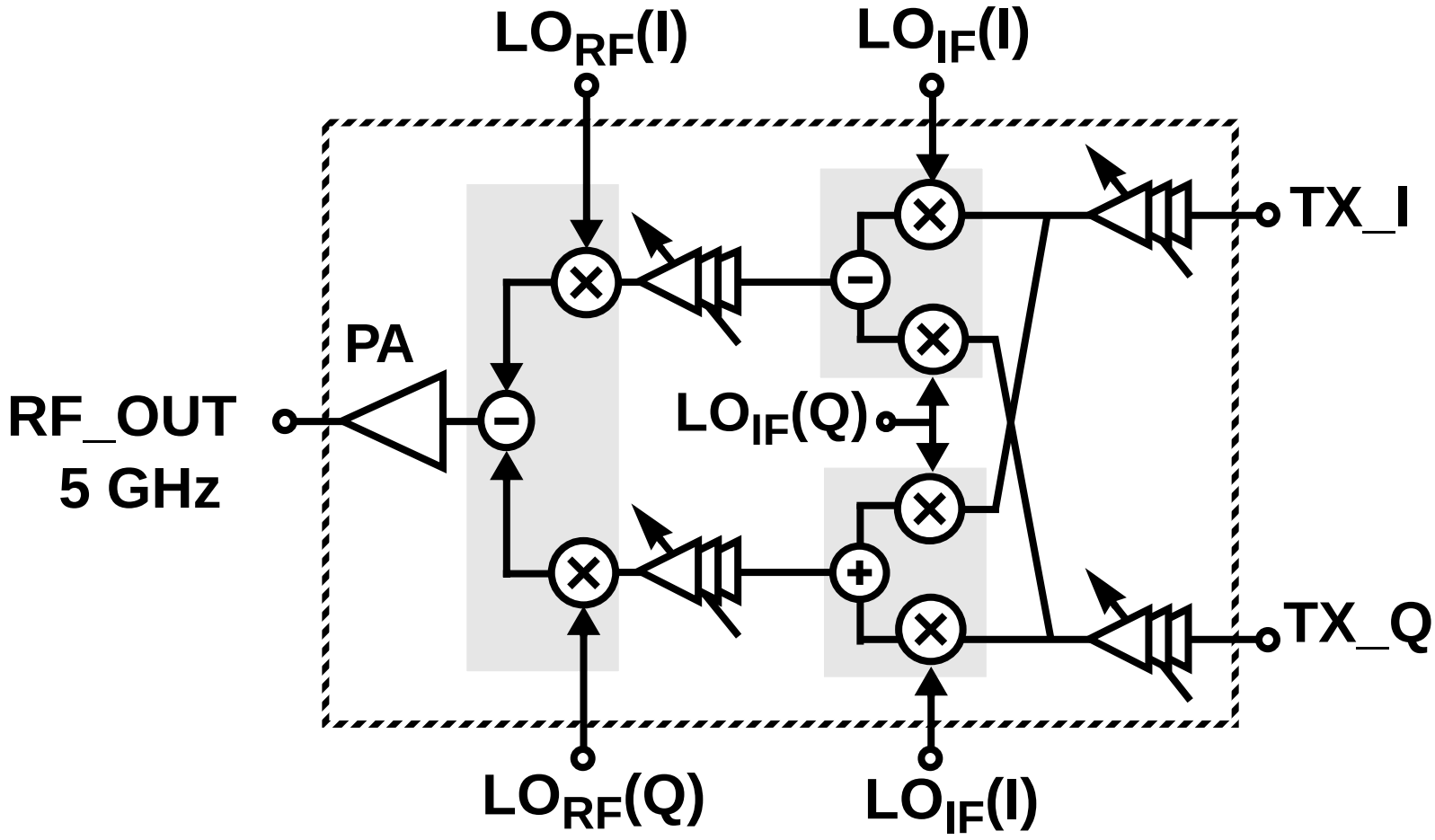


Dual Transmit Conversion

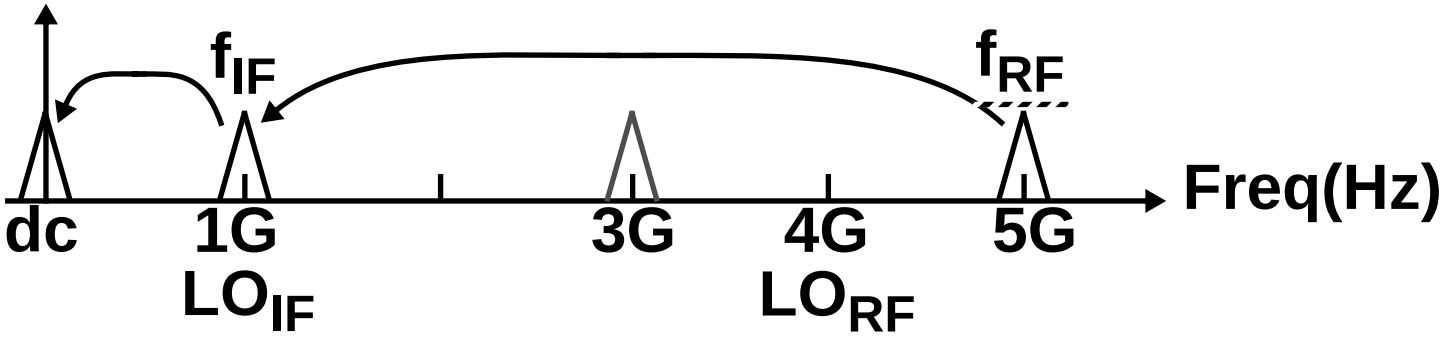


- Radio Frequency (RF) ≠ Local Oscillator (LO)
  - LO leakage is out of band
  - LO pulling by power amplifier is reduced
- Sliding Intermediate Frequency (IF): $LO_{IF} = \frac{LO_{RF}}{4}$
  - Single synthesizer
  - Excellent 1 GHz quadrature for good transmit image rejection
- Double Image-reject mixers
  - Avoid IF filtering of sideband

Transmitter Block Diagram

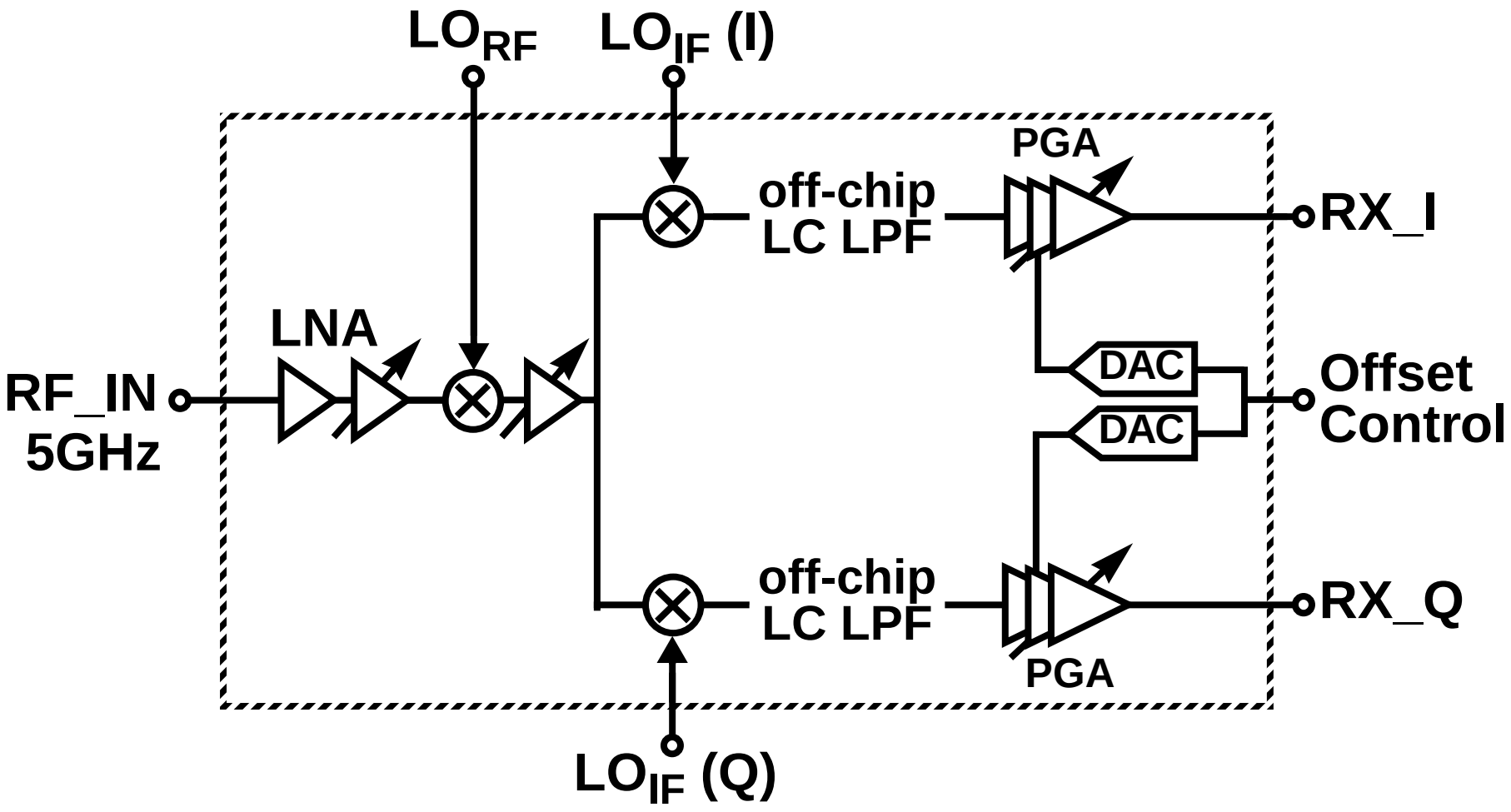


Dual Receive Conversion



- No external IF filtering
- Channel selection at Baseband with passive LC filtering
- Very high IF of 1GHz
  - 3GHz image is 2GHz away from 5GHz signal
  - Inherent bandpass filtering of 3GHz: –23dBc
  - RF mixer: 5-4 = 1GHz (IF) and 5+4 = 9GHz
  - No image-reject mixers

Receiver Block Diagram



Synthesizer

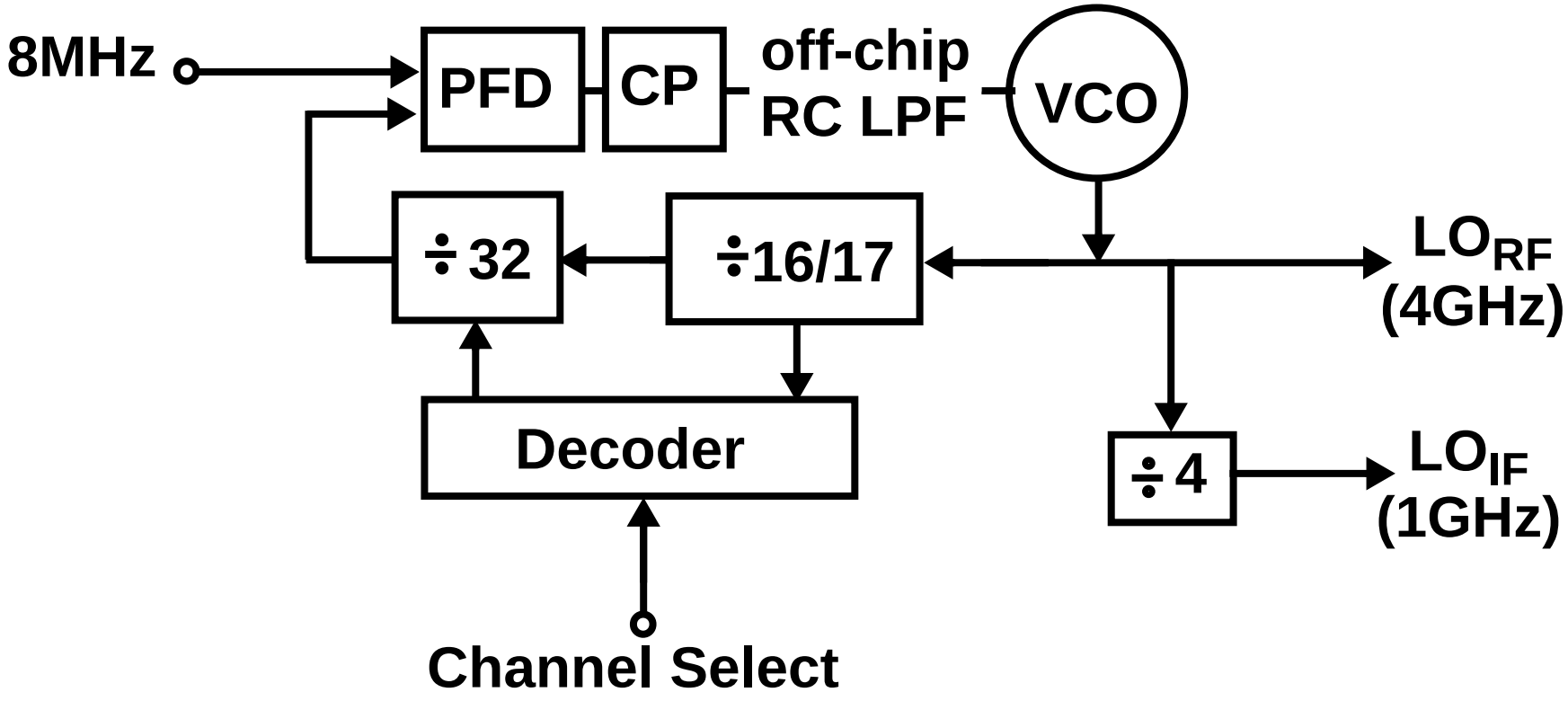
- Single synthesizer with sliding IF:

$$LO_{IF} = \frac{LO_{RF}}{4}$$

- Divide-by-four generates quadrature LO_{IF}
  - Excellent I/Q matching
- P+/N-well varactor
- Frequency Plan:

RF	5.160 to 5.340 GHz	10 MHz spacing
LO_{RF}	4.128 to 4.272 GHz	8 MHz spacing
LO_{IF}	1.032 to 1.068 GHz	2 MHz spacing

Synthesizer Block Diagram



5GHz CMOS RF Design

- **Advantages:**
  - **Low-cost, high-yield**
  - **Multi-layer interconnect makes *decent* inductors**
  - **High-level of integration supports sophisticated digital signal processing***

- **Challenges:**
  - **5 GHz: 0.25μm + narrowband with inductors**
  - **No high-Q BPF: architecture + dynamic range**
  - **Process/Temp Variation: DSP algorithms**
  - **Noise/Power performance limitations**

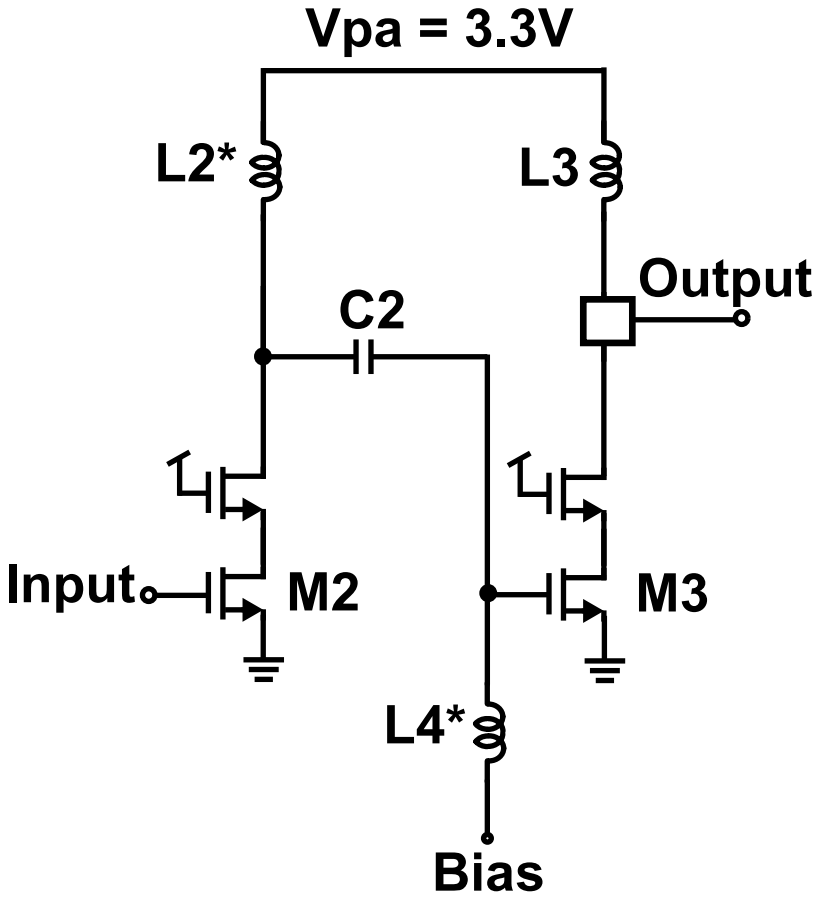
*** J. Thomson et al, ISSCC 2002, Paper 7.2**

Power Amplifier Design

- Large peak to average ratio (PAR) of $\sqrt{52}$ or 17dB
- Signal peaks are infrequent: 0.25dB SNR degradation when PAR reduced to 6dB for 16-QAM*.
- Implications:
  - Poor power efficiency
  - With 6dB PAR, to obtain 40mW (16dBm) requires Psat of ~22dBm or 160mW
  - With 17dB PAR, to obtain 40mW (16dBm) requires Psat of ~33dBm or 2W

*Van Nee & Prasad, OFDM for Wireless Multimedia Communications, Artech House, 2000

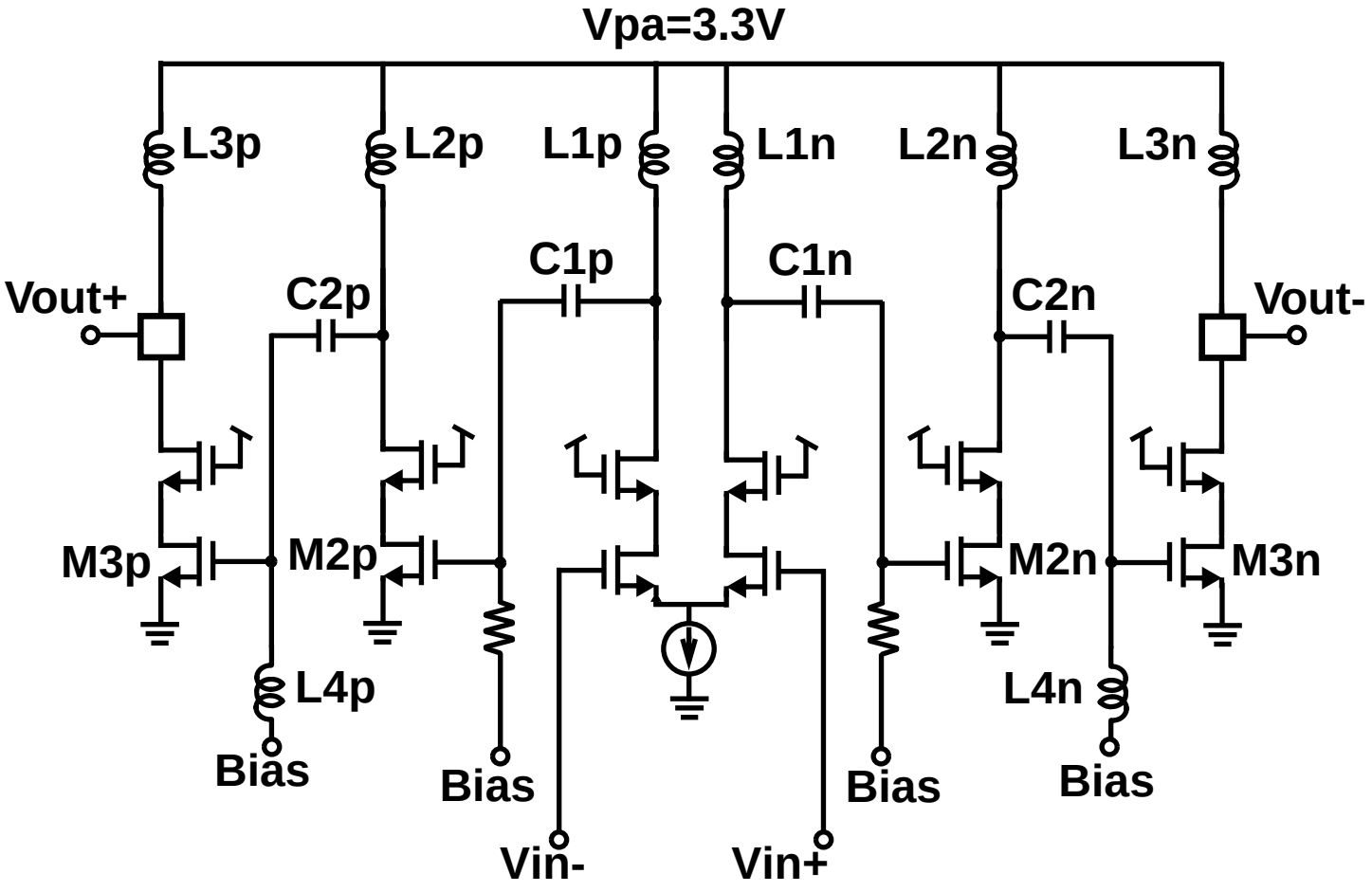
Power Amplifier Topology



- Class A operation
- Cascoded
  - 3.3V supply voltage
  - Stability
- Capacitive Level-shift
  - Metal-2,3,4,5 stacks
- Inductive loads
- Differential
  - Off-chip balun

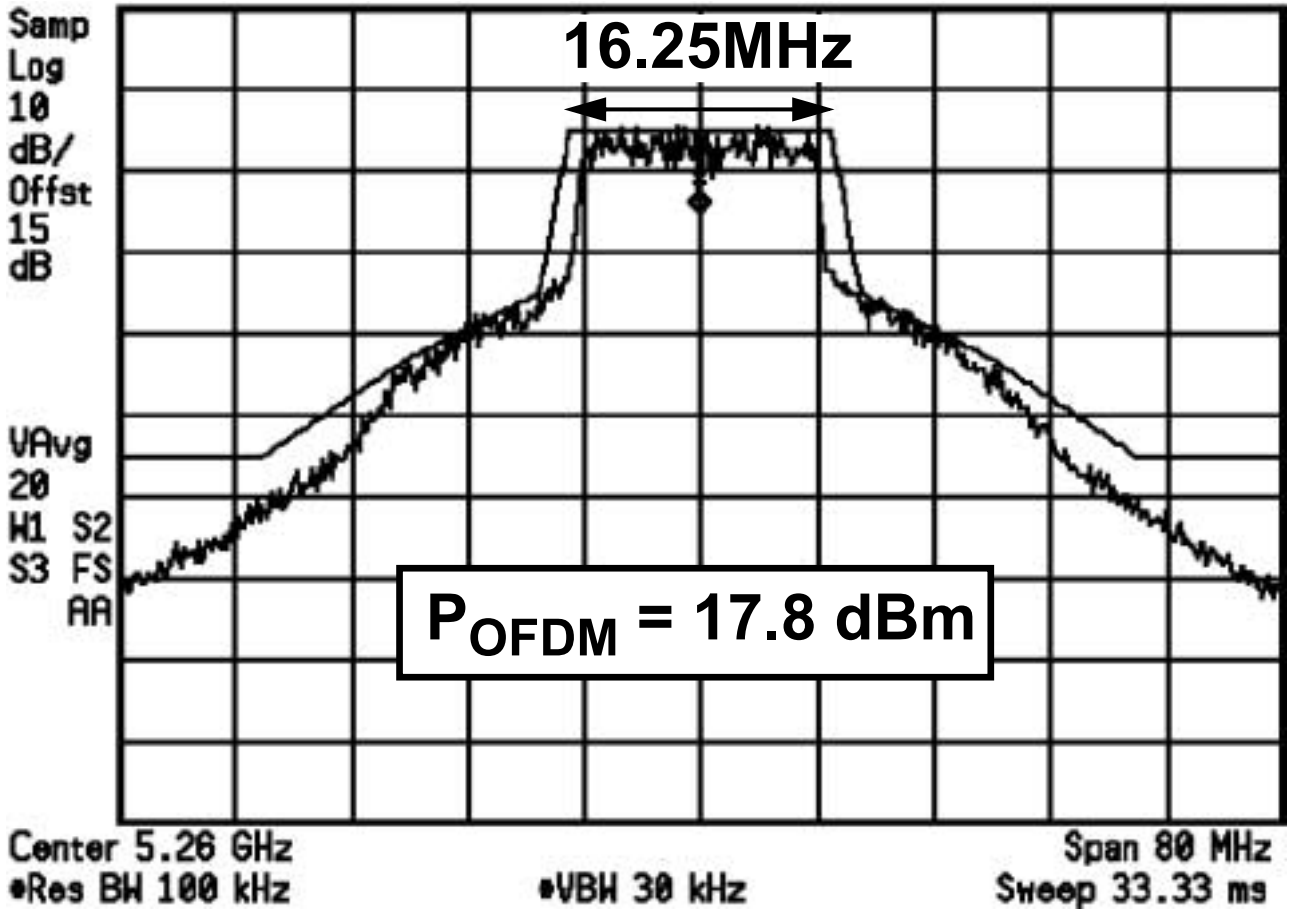
* C.P. Yue and S.S. Wong, IEEE JSSC, May 1998

Power Amplifier Schematic

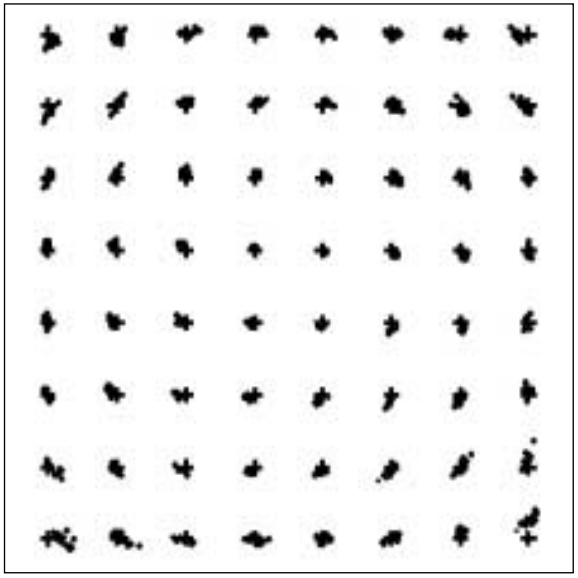


P_{SAT} = 22 dBm

Measured BPSK OFDM Spectrum



Measured Transmit Constellation

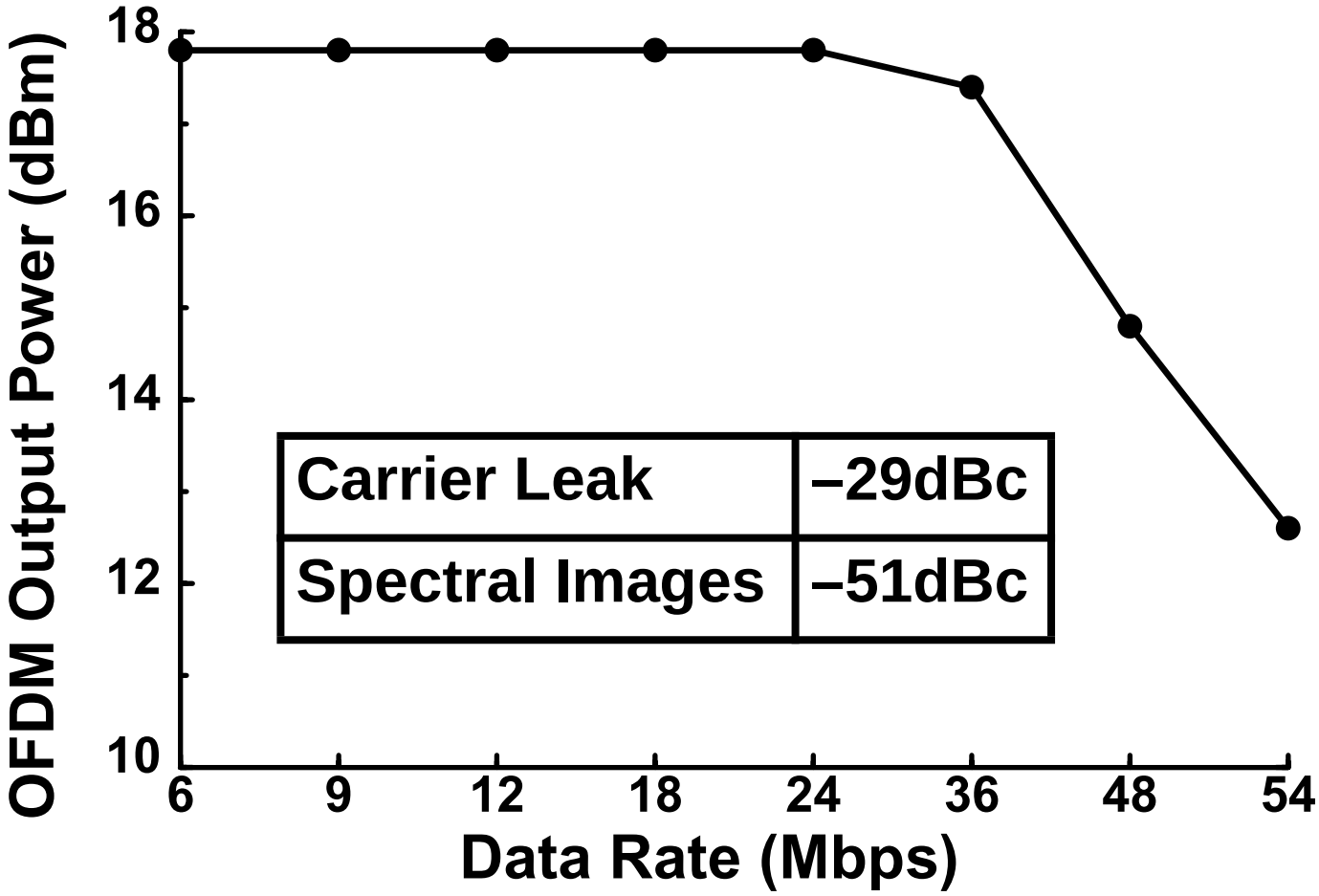


D: Ch1 64QAM Syms/Errs

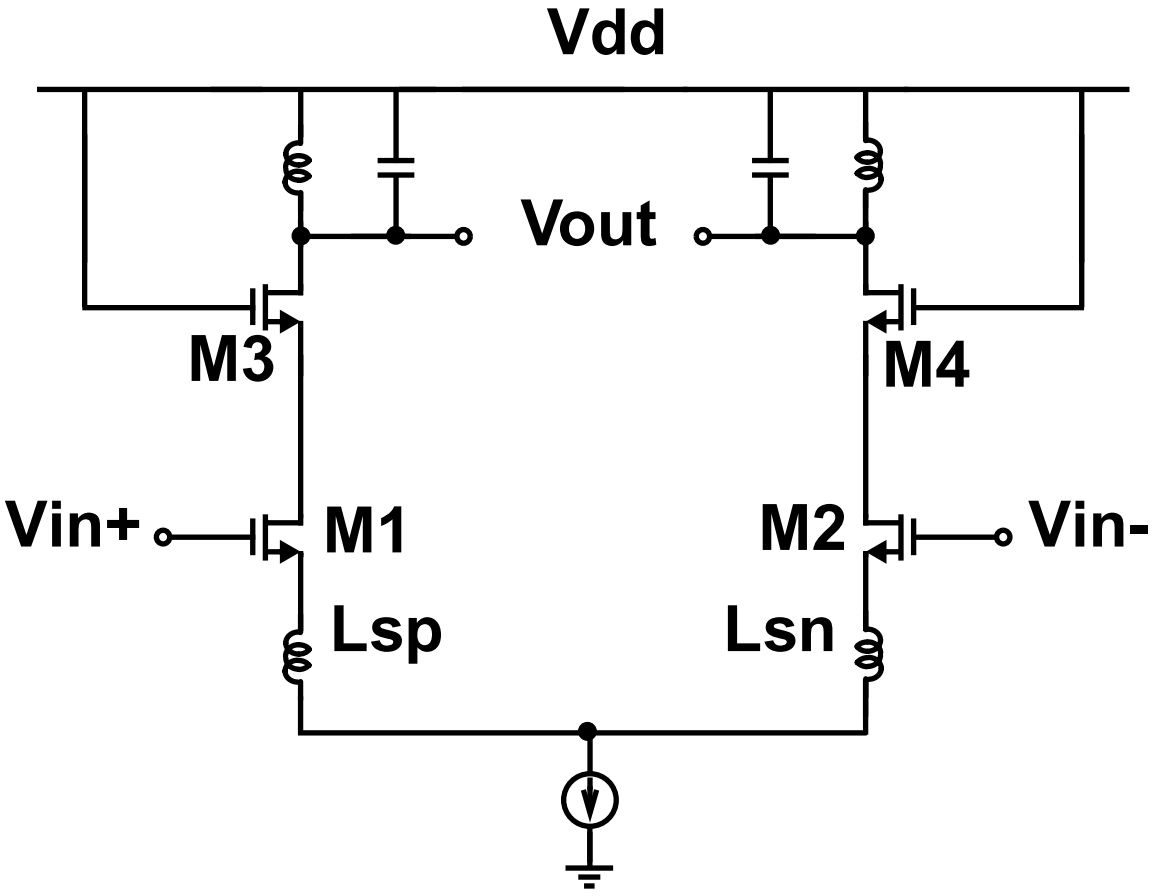
EVM	= 2.3381	%rms	8.4535	% pk	at	sym	305
Mag Err	= 1.2839	%rms	-5.2289	% pk	at	sym	608
Phase Err	= 1.9657	deg	-7.9703	deg pk	at	sym	781
Freq Err	= -878.12	Hz					
IQ Offset	= -32.74	dB	SNR (MER)	= 28.925			dB
Quad Err	= 219.81	mdeg	Gain Imb	= 0.024			dB

64QAM (300kHz) modulated signal

Measured Transmit Output Power

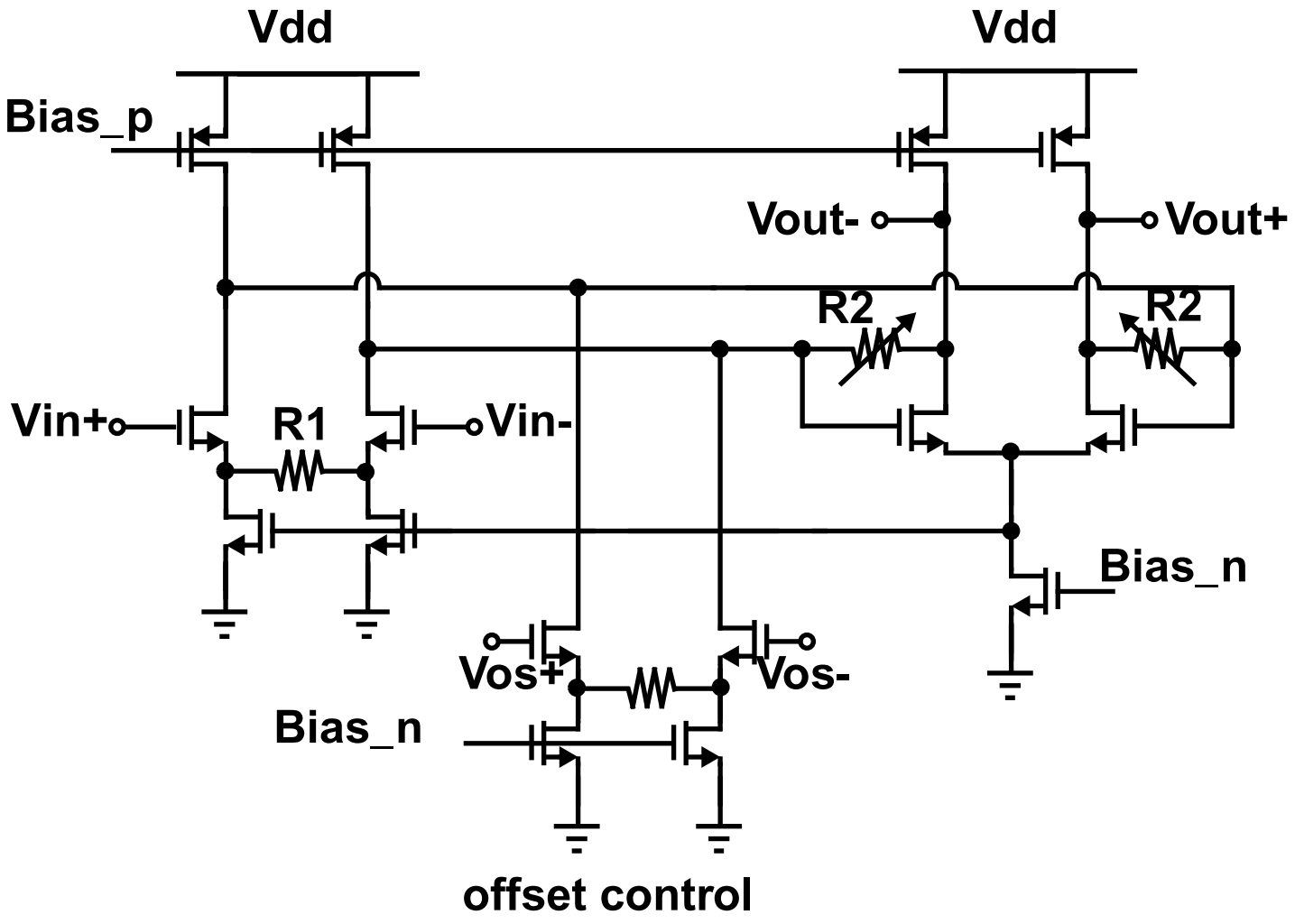


LNA Schematic

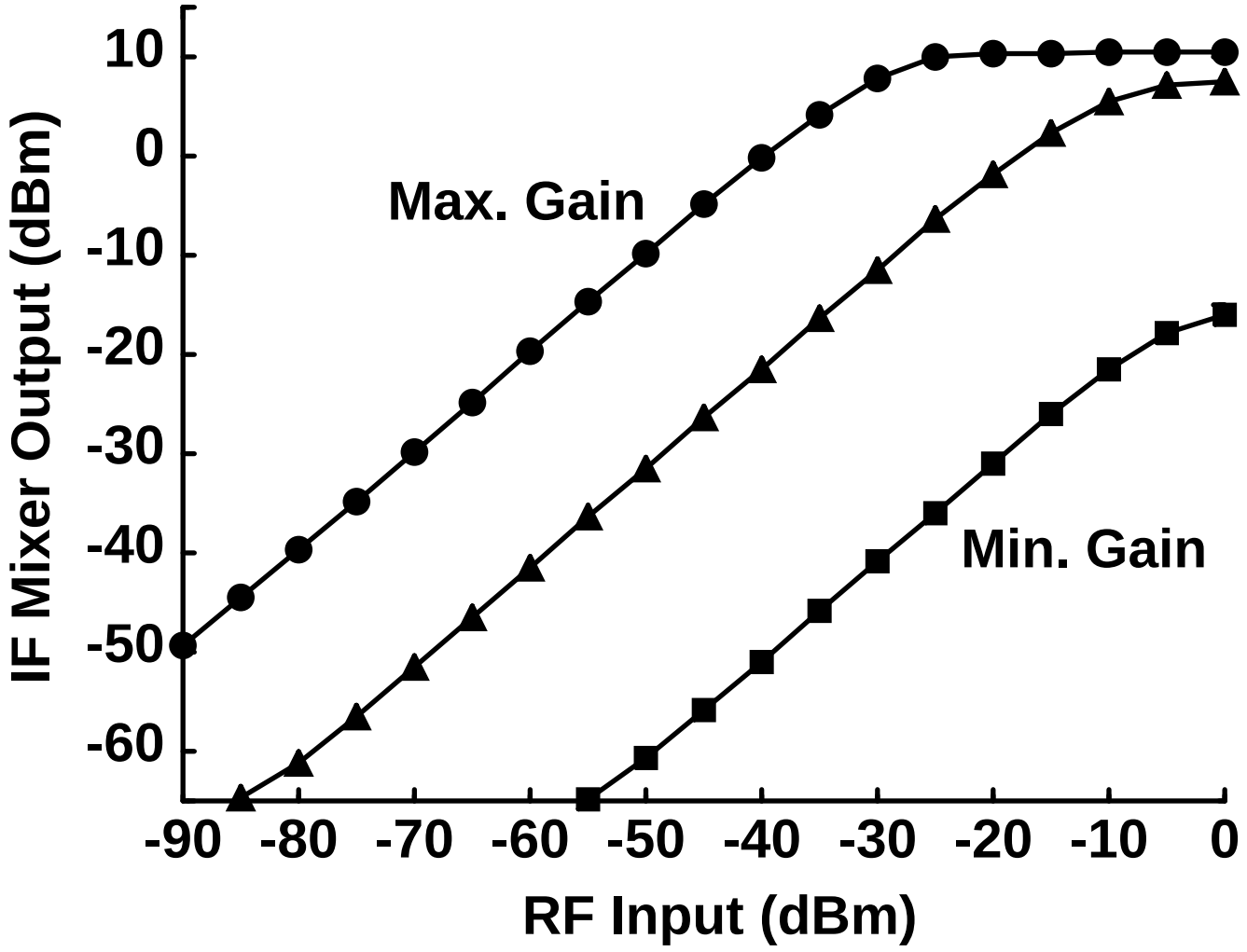


Receiver NF: LNA to Baseband = 8dB

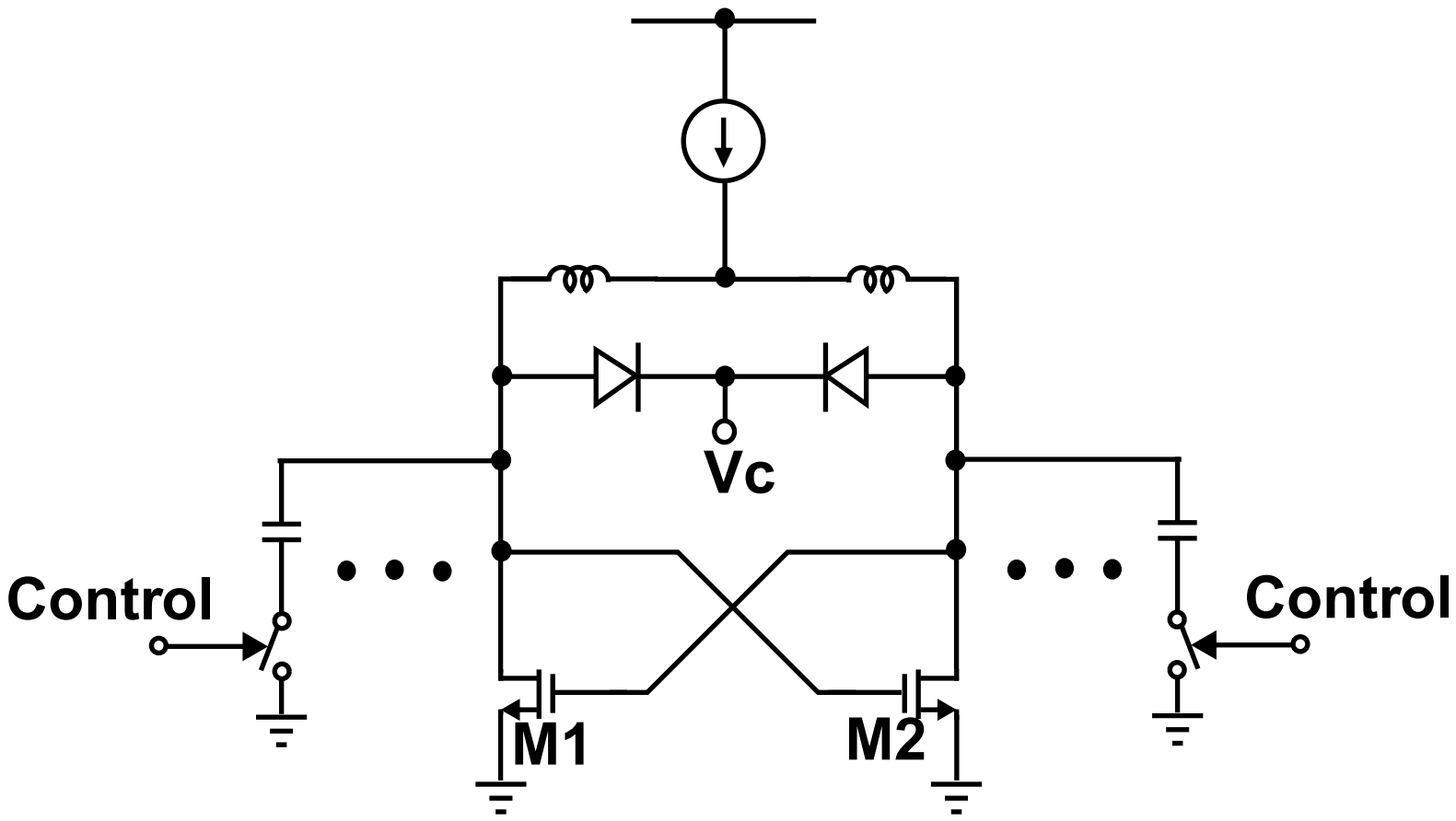
Programmable Baseband Amplifier



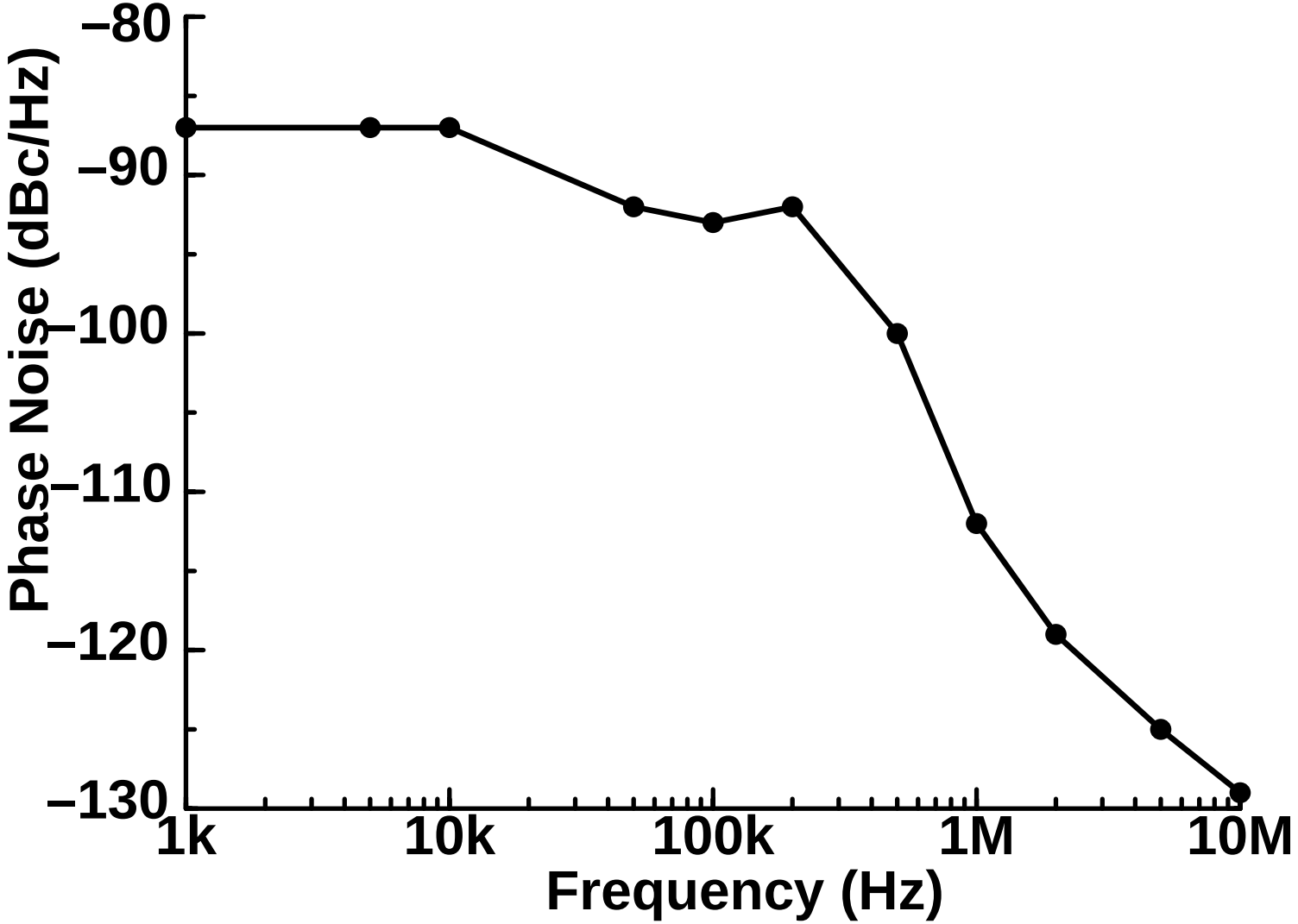
Measured Receiver Performance



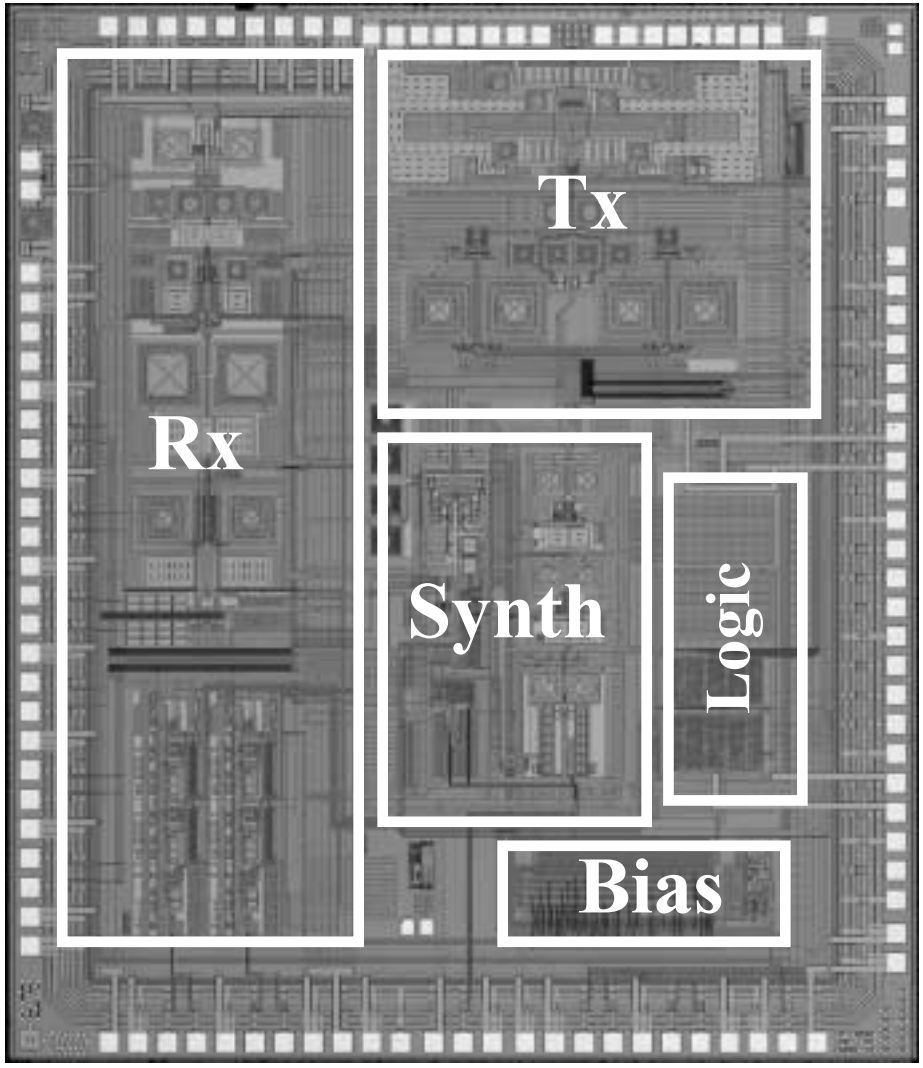
Voltage Controlled Oscillator (VCO)



Composite Phase Noise at 5GHz



Die Photograph



Measured Performance

TX Output Power Level	22 dBm
RX Chain Noise Figure	8 dB
Phase Noise (Δf=1MHz)	–112 dBc/Hz
Supply Voltages	2.5 V & 3.3 V I/O
TX Chain Power Dissipation	790 mW
RX Chain Power Dissipation	250 mW
Synthesizer Power Dissipation	180 mW
Technology	0.25 μm 1P5M CMOS
Package	64-pin LPCC
Die Size	22 mm^2

Conclusions

- IEEE 802.11a radio transceiver in 0.25 μm standard digital CMOS for 5-GHz WLAN
- No external IF filter:
  - TX: double image-reject mixers
  - RX: very high IF of 1GHz
- Dual conversion with sliding IF: single synthesizer
- Integration of:
  - transmitter with 22dBm output power
  - receiver with 8dB noise figure
  - synthesizer with –112dBc/Hz (Δf=1MHz)

Acknowledgement

- Support of the Wireless Team at Atheros for design, layout, and testing. In particular: H. Dieh, J. Kung, R. Popescu, A. Ong, J. Zheng, D. Nakahira, R. Subramanian, J. Kuskin, A. Dao, D. Johnson, C. Lee, L. Thon, P. Husted, W. McFarland, S. Wong, R. Bahr, T. Meng
- Assistance of TSMC. In particular: S. C. Wong and B. K. Liew.