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A 6.3μW 20bit Incremental Zoom-ADC with 6ppm INL and 1μV Offset

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Abstract – A 20-bit incremental ADC for battery-powered sensor applications is presented. It is based on an energy-efficient zoom ADC architecture, which employs a coarse 6-bit SAR conversion followed by a fine 15-bit ΔΣ conversion. To further improve its energy efficiency, the ADC employs integrators based on cascoded dynamic inverters for extra gain and PVT tolerance. Dynamic error correction techniques such as auto-zeroing, chopping and dynamic element matching are used to achieve both low offset and high linearity. Measurements show that the ADC achieves 20-bit resolution, 6ppm INL and 1μV offset in a conversion time of 40ms, while drawing only 3.5μA current from a 1.8V supply. This corresponds to a state-of-the-art figure-of-merit (FoM) of 182.7dB. The 0.35mm^2 chip was fabricated in a standard 0.16μm CMOS process.

Index Terms – A/D conversion, battery-powered sensors, low power circuits, incremental ADC, zoom ADC, SAR ADC, delta-sigma ADC, inverter-based integrator, and dynamic error correction techniques.

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I. INTRODUCTION

Instrumentation applications, such as the readout of bridge transducers and smart sensors, require analog-to-digital converters (ADCs) with high absolute accuracy and linearity as well as high resolution [1]-[3]. Since the signals of interest are typically near DC, such ADCs must also be robust to offset and 1/*f* noise. However, fulfilling all these requirements often results in ADCs with poor energy-efficiency and/or high power consumption, thus making them unsuitable for use in battery-powered autonomous systems.

SAR converters can be very energy efficient (< 10fJ/conv-step) [4], [5], but component mismatch typically limits their resolution to the 12–14 bit level, although this can be extended to the 18-bit level with the help of calibration and dithering [6]. Dual-slope and delta-sigma (ΔΣ) ADCs are capable of achieving even higher resolution and so are widely used in instrumentation applications. However, the resolution of a dual-slope ADC is linearly proportional to their conversion time, making them relatively slow and resulting in poor energy-efficiency [7]. In contrast, delta-sigma (ΔΣ) ADCs, by utilizing oversampling and higher-order noise-shaping, are able to achieve high resolution in less time and so can achieve better energy efficiency. In instrumentation applications [8]-[14], ΔΣ ADCs are usually operated in *incremental* mode, in which they are first reset and then operated for a fixed number of cycles.

For many applications, e.g. in smart sensors, first or second-order incremental ΔΣ ADC are often used [9]-[10]. However, achieving high resolution still requires a relatively long conversion time, resulting in poor energy-efficiency. Higher-order or multi-bit architectures

are faster, but reported implementations still only achieve moderate energy efficiency [2], [11], [12]. Another alternative is the extended counting architecture, in which the residue of a coarse incremental ΔΣ ADC is digitized by a fine Nyquist ADC [13], [14]. This two-step architecture is more energy efficient, since the resolution requirements on the relatively slow ΔΣ ADC are now relaxed, leading to a faster conversion. However, the overall linearity of the ADC is limited by the linearity of the Nyquist ADC. A recent implementation [14], achieves good energy-efficiency (160dB FoM) from a 1.8V supply, but only achieves 15-bit linearity.

This paper describes the design of an energy-efficient 20-bit incremental *zoom* ADC. It employs an energy-efficient two-step architecture, in which a coarse SAR ADC is used in conjunction with a fine incremental ΔΣ ADC. Initially, the SAR ADC makes a coarse conversion with a low resolution e.g. 6-bit. In the succeeding fine conversion, this result is used to adjust the references of the ΔΣ ADC so as to zoom into a small range around the input signal. In contrast to conventional two-step ADC architectures, the fine converter of a zoom ADC does not digitize the residue of the coarse converter, and so the accuracy of the conversion depends exclusively on the accuracy of the fine converter. Moreover, zooming relaxes the resolution requirement of the fine converter, which, in turn, results in shorter conversion times and small internal signal swings, which can then be handled by simple and energy-efficient amplifiers. In this work, inverter-based integrators are used. The ADC's performance is further improved by the use of dynamic error correction techniques, such as dynamic element matching (DEM) for high linearity, and auto-zeroing and chopping for low offset and 1/*f* noise. The zoom ADC is implemented in a standard 0.16μm CMOS process and achieves 119.8dB SNR, 6ppm INL, and 1μV offset in a conversion time of 40ms, while drawing only 3.5μA current from a 1.8V supply [15].

This paper is organized as follows: Section II describes the zoom ADC architecture, while

Section III addresses the fundamental limitations and trade-offs in the design of a 20-bit incremental zoom ADC. Section IV discusses the implementation details, and Section V is devoted to the experimental results. Finally, conclusions are presented in Section VI.

II. ZOOM ADC ARCHITECTURE

The general concept of a two-step ADC is illustrated in Fig. 1. The first stage is a low resolution ADC, which performs a coarse conversion whose output is then processed by a DAC. The difference between the input signal X and the DAC's output is the residue Q_1 which is further processed by the second stage. The second stage is a fine ADC with a reduced conversion range. Assuming that the DAC is ideal, the overall output Y_{out} of such an ADC contains only the quantization error of the fine ADC, while the ADC's overall accuracy and linearity is limited by the fine ADC. In order to mitigate this, the ADC may be preceded by a residue amplifier. However, both the amplification and the preceding subtraction will themselves introduce offset, gain and linearity errors. Furthermore, DAC non-idealities will also introduce extra errors.

In a zoom ADC, an incremental ΔΣ ADC is directly used as the fine converter of a two-step ADC, but without any residue computation, [15]-[17]. The results of the coarse conversion are used to dynamically adjust the references of the fine ADC such that its input range just straddles the current value of the input signal. The resolution of the fine ADC can now be considerably relaxed, since its input range is now much smaller than that of the coarse ADC. This, in turn, reduces the ADC's conversion time and improves its energy efficiency. Furthermore, there are no errors associated with residue computation. Although the linearity of the coarse ADC will still be limited by component matching, the linearity of the ΔΣ ADC can be significantly improved by employing DEM. The associated ripple, together with the modulator's quantization noise will be suppressed by the ADC's decimation filter.

Fig. 2 shows a zoom ADC, based on a first-order ΔΣ ADC, i.e. a ΔΣ modulator followed by a decimation filter. The first stage is an M-bit Nyquist ADC, which efficiently shares the same set of references as the ΔΣ ADC. The results of the coarse conversion are then used to

select a *P*-bit subset of these references, where $P < M$, for use by the ΔΣ modulator. In other words, the references are chosen to *zoom* into the region determined by the coarse ADC. A key observation is that since the input range of the ΔΣ modulator is now quite small, typically only a few LSBs of the coarse ADC, the internal signals in its loop filter will also be small, thus allowing it to be implemented with simple and energy-efficient amplifiers.

III. SYSTEM-LEVEL DESIGN

A. Incremental ΔΣ modulator

Fig. 3 shows the general block diagram of a single-loop ΔΣ modulator. When used in an incremental mode, its signal-to-quantization noise-ratio (SQNR) will depend on three parameters: the loop filter's order, the quantizer resolution, and the number of clock cycles *N*. Due to its ideal linearity, a 1-bit quantizer is best suited for precision applications. To illustrate the modulator's design space, Fig. 4 shows the SQNR of a 1-bit incremental ΔΣ modulator versus the number of cycles *N* for various modulator orders *L*. It can be seen that for the same SQNR, the *N* can be reduced by using higher order loop filters. However, this is at the expense of a reduction in the range of input signals for which the modulator is stable. For example, the usable input range for the 3rd order ΔΣ modulator is only about 67% of its reference range [2]. This, in turn, requires less circuit noise and more power to achieve a given resolution. As will be shown in the following, the zoom ADC architecture circumvents most of these issues.

B. Incremental Zoom ADC

The maximum SQNR obtainable from the 1st and 2nd order zoom ADCs versus *N* is illustrated in Fig. 4, assuming a coarse ADC resolution of 6-bit for both cases. For comparison, the SQNRs of the conventional 2nd order and 3rd order ΔΣ modulators are also included. In order to achieve the target SQNR of 130dB (to allow a thermal noise-limited resolution of 20

bits), the 1st order zoom ADC requires 32k cycles, which is still too long for good energy efficiency. In this work, as shown in Fig. 5, a 2nd order zoom ADC was chosen, which theoretically only requires 300 cycles to achieve the target SQNR.

C. Redundancy

The coarse ADC is designed for a moderate resolution of 6 bits, while its offset and quantization errors are accommodated by making the fine conversion range equal to 2 LSBs of the coarse conversion. This redundancy relaxes the required accuracy of the coarse ADC, and ensures that the input X will always lie safely within the input range of the fine ΔΣ ADC. Since extending the range comes at the price of increasing the required resolution of the ΔΣ phase, the number of cycles should be appropriately increased to maintain the target SQNR. In the case of a 2nd order zoom ADC, simulations show that 400 cycles are required to meet the target SQNR of 130dB, as shown in Fig. 4.

Assuming a 1.8V reference voltage and a fine input range of 2 LSBs, the error in the coarse ADC should be less than half LSB, i.e. about 14mV. The full scale range of the fine step is then 56mV. By combining the results from the two conversion steps, the digital output Y_{out} of the zoom ADC can be expressed as follows:

$$Y_{out} = Y_{coarse} \cdot 2^{n-1} + Y_{fine}, \quad (1)$$

where n is the bit resolution of fine ΔΣ ADC, and Y_{coarse} and Y_{fine} are the results of coarse and fine ADCs, respectively. The overlap between the two conversion steps is readily implemented by setting the feedback reference range of the ΔΣ modulator to $2 \cdot V_{LSB,COARSE}$, as will be described in Section-IV.

D. ΔΣ Modulator

Fig. 6 shows the maximum amplitude (normalized to the reference voltage) at the output of the first integrator of a zoom ADC as a function of the coarse ADC's resolution. As shown,

the output swing is inversely proportional to the resolution of the coarse ADC. Therefore, for a 6-bit coarse ADC, the proposed zoom ADC requires an output swing of only 4.5% of the reference voltage i.e. 81mV for a 1.8V reference. As a result, the required OTAs have very relaxed settling requirements and so can be realized in a simple and power-efficient manner.

The OTA's finite DC gain and gain variation are a critical source of error. The DC gain can be approximated by a third-order polynomial [18] as follows:

$$A_{dc}(V_{out}) \approx A_{dc} \cdot (1-\sigma(V_{out}/V_{max})^3), \quad (2)$$

where A_{dc} is the DC gain at the midlevel output, σ is the gain variation coefficient, V_{out} is the output swing, and V_{max} is the maximum output swing. Fig. 7 shows the simulated SQNR degradation due to the finite DC gain and gain variation of the OTA in the first integrator, assuming that the second integrator is ideal. To tolerate 1dB degradation from the target SQNR, a DC gain of only 60dB is sufficient for $\sigma = 0.9$, which represents a significant third-order variation coefficient. In order to achieve similar performance with a 1-bit 3rd order $\Delta\Sigma$ ADC [2], a minimum DC gain of 120dB would be required, which is considerably higher and more difficult to achieve especially at supply voltage of 1.8V or below.

Due to their reduced output signal swing, the OTA's of a zoom ADC do not slew and so their settling follow a single pole response. In this case, incomplete settling just results in a fixed integrator gain error in the integrator. As long as this error does not significantly alter the loop filter's transfer function, it will not impair performance. A clock period equal to 7 time constants results in a gain error of 0.1%, which is sufficient to maintain the target SQNR.

E. Decimation Filter

A decimation filter provides the digital output Y_{fine} by filtering the bit-stream of the fine $\Delta\Sigma$ modulator. For an incremental $\Delta\Sigma$ modulator, a matched filter made from a cascade of integrators can be used as an optimal decimation filter in the sense that it minimizes the

number of ADC cycles required to achieve a target SQNR [19]. Such a filter, however, does not adequately suppress power line noise or the ripple associated with dynamic element matching. This is because its coefficients are asymmetrical, with the highest weight on the first sample and decreasing thereafter. In contrast, a sinc^2 filter, whose impulse response is a symmetrical triangular shape, sufficiently suppresses such errors and is a suitable candidate to optimize the performance of a 2nd order zoom ADC. The transfer function of a sinc^2 filter is given by

$$H(z) = 1/D^2 \left((1-z^{-D})/(1-z^{-1})\right)^2 \quad (3)$$

where D is the decimation ratio. The filter has notches at the integer multiples of f_s/D. Therefore, periodic noise such as power line noise can be suppressed by appropriately choosing the sampling frequency and decimation ratio. The required number of ADC cycles N increases by a factor of 2 for the target SQNR when a sinc^2 filter is used. In this work, f_s=25.6kHz, D=512, and N=1024 are chosen, which creates a first notch at the power line frequency of 50Hz.

F. Precision Techniques

As will be described later, the offset and 1/*f* noise of the integrators are mitigated by employing auto-zeroing. This results in a few tens of μV residual offset, which is not enough to achieve the targeted μV level offset. To reduce the offset further, the ADC is chopped at system-level. In contrast to [2], [16], [20], this was implemented in a digital rather than an analog manner. As shown in Fig. 8, the overall conversion is performed twice with swapped input polarities and the two conversion results are averaged. This eliminates the need for either state-preserving choppers around integrators [16] or complex sequencing of chopper control [2], which could be a potential source of charge injection. After system-level chopping, the residual offset can be reduced to the level of ADC's resolution at the cost of an extra

conversion cycle, i.e. N=2048. However, this also improves the overall SNR by 3dB, since it is limited by thermal noise.

The zoom ADC's ΔΣ modulator uses a 1-bit quantizer, and so its linearity is not limited by quantizer offset and offset spread. However, the ADC's overall linearity is limited by the nonlinearity of the multibit DAC (M=6-bit), which is caused by the mismatch of the various DAC elements. Although this can be improved by calibration and/or trimming, it is not enough to achieve the targeted ppm-level of nonlinearity. A more effective solution is to apply DEM to the unit elements of a capacitor DAC. In the chosen process, an initial mismatch of 0.05% can be achieved by using 160fF unit cap made from lateral metal-metal capacitors. This can be reduced even further by DEM. It can be shown that the residual error E after DEM and for a number of cycles N is bounded as follows:

$$E=|1/N\cdot\sum_{i=1}^{N}\ \delta_i\ |<1/N\cdot\sqrt{2^M}\cdot\delta_{max} \qquad (4)$$

where δ_i is the relative error of the i^{th} capacitor with respect to an average capacitor value, and δ_{max} is the worst-case mismatch [21]. Therefore, assuming δ_{max}=0.05%, M=6 and N=2048, an error level of ±2ppm should be theoretically possible. However, errors introduced by the DEM switches will be a source of residual non-linearity, and will limit the ultimate INL. It should be noted that eq. (4) defines a tradeoff between M, N and E. Increasing M to reduce the number of ΔΣ cycles will also results in a loss of linearity, so making M larger than 6 bits is not necessary to achieve 20-bit performance. The complete block diagram of the proposed 2nd order incremental zoom ADC and the associated timing diagram are shown in Fig. 9. It is noted that the reset signal is applied to both modulator and sinc^2 filter at the start of each conversion to bring them in a well-defined state.

G. Capacitor Sizing

The size of the sampling capacitors was informed by the need to ensure that during the coarse conversion the errors due to noise and mismatch are less than $0.5V_{COARSE,LSB}$ (14mV). In practice, this means that the value of the sampling capacitors is determined by matching requirements. Since there is no residue computation or storage in a zoom ADC, its thermal-noise level is solely determined by the *kT/C* noise of the fine ΔΣ ADC. The sampling capacitor of the fine ΔΣ ADC's first stage is 10.2pF, which was chosen to meet the *kT/C* noise constraints with N =1024. This was then sub-divided into 64 unit capacitors of 160fF, which serve as the unit elements of the coarse ADC. Due to the scaled noise requirements, the second stage of the fine ΔΣ ADC use a 0.2pF sampling capacitor.

IV. Implementation Details

A. Coarse SAR ADC

In most instrumentation applications, the input is a static signal, which remains essentially constant throughout a conversion. This means that the coarse and fine conversions of a zoom ADC can then be performed sequentially. As shown in Fig. 9, this implies that the same Cap-DAC can be used during both conversion steps, resulting in a compact realization. In the actual implementation, the quantizer is also shared between the two conversion steps.

Fig. 10 shows a simplified circuit diagram of the coarse SAR ADC. The actual implementation employs a pseudo-differential configuration. The circuit is based on an auto-zeroed inverter-based integrator. At the start of each comparison step, the input signal is sampled on all the capacitors of the Cap-DAC, while the first integrator is auto-zeroed and reset. The sampled value is then compared to a weighted sum of the references and the result is transferred to the integration capacitor. After six comparison steps, the coarse result k is found such that $k \cdot V_{LSB,\,SAR} < V_i < (k+1) \cdot V_{LSB,\,SAR}$. The value k is then stored in the SAR register and used to reconfigure the references of the fine ΔΣ ADC. The 6-bit unary-weighted Cap-DAC was implemented using 160fF fringe capacitors realized in three metal layers (metal-2 to 4). The use of metal-1 was avoided to reduce the undesirable parasitic capacitance to ground. The 1-bit quantizer was implemented as a dynamic latch proceeded by a two-stage preamplifier, which ensures that its total offset is well below $0.5V_{LSB.SAR}$.

B. Fine Incremental ΔΣ Modulator

During the fine conversion step, V_i is accurately digitized by a 1-bit 2^{nd} order ΔΣ modulator with a extended range of $2 \cdot V_{LSB,\,SAR}$. However, ensuring that the input V_i is always roughly in the middle of this extended range requires an extra comparison step. This involves comparing V_i to $(k+0.5) \cdot V_{LSB,\,SAR}$ at the end of the coarse conversion. Depending on the result,

the references of the fine converter can then be set to cover the range from (k-1) to (k+1) or the range from k to (k+2). This extra step was implemented by adding a half size capacitor $C_{S,65} = C_{S,1\text{-}64}/2$ to the Cap-DAC.

Fig. 11 shows a simplified circuit diagram of the fine ΔΣ modulator. Before each conversion, both integrators are reset. Like the 1st integrator, the 2nd integrator is also implemented with a pseudo-differential inverter-based amplifier. To avoid output common-mode drift due to mismatch and charge injection, a passive CMFB circuit is implemented as in [22]. During the sampling phase ϕ_1, the input voltage V_i is sampled on all 64 elements of the Cap-DAC. At the same time, the first integrator is in the unity-gain configuration and auto-zeroed with the help of offset-storage capacitor C_C. During the integration phase ϕ_2, m elements of the Cap-DAC are connected to either V_{REF+} or V_{REF-}, depending on the bit stream value, thus transferring an amount of charge proportional to $V_i \pm m/64 \cdot V_{REF}$ to the integration capacitor C_I (8.3pF). Sampling and integration capacitors in the second stage are scaled down to 0.2pF and 0.4pF, respectively. A passive switched-capacitor adder at the quantizer input combines the outputs of two integrators, thus forming the feed-forward path around the second integrator. During the coarse conversion, the 2nd integrator is bypassed, and thus the output of the first integrator is directly connected to the quantizer, as shown in Fig. 10.

C. Inverter-based Integrator

As previously discussed, a DC gain larger than 60dB is required in the first integrator. A ΔΣ modulator employing energy-efficient inverter-based integrators has been proposed in [22]. The proposed topology, however, does not provide the required DC gain and is prone to PVT variations. To address these issues, a novel inverter-based integrator is proposed in this work. As shown in Fig. 12, it consists of a cascoded inverter, which is dynamically biased to enhance its immunity to PVT variations. During the sampling phase, M_{p1}, M_{n1} are biased via

cascode transistors M_{p21}, M_{n21} and a floating current source consisting of M_1, M_2, while M_{p22}, M_{n22} are in the off state. This ensures that both M_{p1}, M_{n1} are biased with exactly the same bias currents. At the same time, the bias voltages V_{OP} and V_{ON} associated with this operating condition are stored on the offset-storage capacitors C_C. This auto-zeroing process simultaneously cancels the inverter's offset and 1/*f* noise. During the integration phase, the bias voltages of cascode transistors M_{p21}, M_{n21} are swapped with those of M_{p22}, M_{n22}. This disconnects the inverter from the floating current source and reconfigures it as a high gain push-pull common-source amplifier with a well-defined bias current. As a result, the inverters of the 1st and 2nd stages draw only 2μA and 300nA, respectively, while obtaining DC gains greater than 80dB over PVT variations. Fig. 13 shows the implemented configurations of the integrator together with its bias circuit during the sampling phase.

Due to noise-folding, the auto-zeroing process reduces 1/*f* noise at the cost of increased thermal noise near DC [23]. Therefore, the amplifier's noise becomes a dominant noise source in auto-zeroed (AZ) integrator. This, in turn, requires a large increase in power consumption to maintain the target noise level. This noise penalty can be overcome by decoupling the amplifier's noise density from its bandwidth [24], [25]. During the auto-zeroing phase, the effective noise bandwidth can be lowered by increasing the value of compensation capacitor C_C and thus reducing the amount of noise-folding. This does not affect the amplifier's settling time during the integration phase, because C_C is then connected in series with the amplifier's input and so does not load the amplifier. In this work, C_C=3C_S, which significantly mitigates the effect of noise-folding.

D. Dynamic Element Matching

The target linearity of the feedback DAC is achieved by using data weighted averaging (DWA), a well known form of DEM [26]. Compared to traditional multi-bit architecture, the

timing overhead associated with the DEM logic is quite relaxed. This is because the coarse result k is known throughout the conversion and only the last two unit elements need to be selected (or deselected) by the current value of the modulator's bit-stream.

V. Experimental Results

The prototype chip was realized in a standard 0.16μm CMOS process. The ADC has an active area of 0.375 mm^2 as shown in Fig. 14. For flexibility, the digital logic and $sinc^2$ filter were implemented in an off-chip FPGA. The ADC draws only 3.5μA from a 1.8V supply. It can operate with a supply voltage in the range of 1.2–2V. An external voltage reference of 1.8V is used as ADC's reference voltage.

Fig. 15 shows the output spectrum of the free-running ΔΣ modulators with DEM "on" at a sampling frequency of 25.6 kHz. It can be seen to be free of DEM-related tones. Fig. 16 shows the measured input-referred ADC noise as a function of the number of ADC cycles. For $N < 700$, the ADC is in the quantization-noise-limited region. In a conversion time of 40ms, a thermal-noise-limited output noise of $0.65\mu V_{rms}$ was measured, resulting in an SNR of 119.8dB for a ±0.9V differential input. As illustrated in Fig. 17, the ADC exhibits an average offset of 0.5μV with a maximum of 1μV based on measurements from 9 samples. With DEM "off," the ADC's linearity is mainly limited by Cap-DAC mismatch, resulting in an INL of about 180ppm, as shown in Fig. 18. This drops to 6ppm with DEM "on." The ADC's PSRR was measured to be about 120dB at DC and about 103dB at 50Hz.

In Table I, the ADC's performance is summarized and compared to other state-of-the-art in high resolution incremental ADCs [2], [3], [12], [14]. Compared to these designs, it requires significantly less area and power. For incremental ADCs, the figure-of-merit (FoM) derived from Schreier's *FoM* [27] can be calculated as follows:

$$FoM = SNR_{max} + 10 \cdot \log\left(1/(Power \times 2T_{conv})\right), \quad (5)$$

where T_{conv} is conversion time, and SNR_{max} is the maximum SNR, which corrects the crest factor to enable fair comparison with general-purpose ADCs characterized by using a sine input. This work achieved a *FoM* of 182.7dB, which represents a 16dB improvement on the

state-of-the art.

VI. Conclusion

A 20-bit incremental analog-to-digital converter has been realized in a 0.16μm CMOS technology. The prototype ADC achieves 20-bit resolution, 6ppm INL and 1μV offset in a conversion time of 40ms, while dissipating only 3.5μA current from 1.8V supply. This performance is achieved by using a zoom ADC architecture, a novel inverter-based integrator and various dynamic error correction techniques. This work achieves the state-of-the-art FoM of 182.7dB, which is the highest reported FoM for incremental ADCs published to date.

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Table Caption

Table I. Performance summary and comparison with previous work.

Figure Caption

Fig. 1. Block diagram of two-step ADC.

Fig. 2. A zoom ADC employing a 1st order ΔΣ ADC.

Fig. 3. A basic single-loop ΔΣ modulator.

Fig. 4. SQNR versus number of cycles (N), L=Loop filter's order, M=Coarse ADC's bit resolution (a) 1-bit ΔΣ ADCs (b) 1st and 2nd order zoom ADCs.

Fig. 5. A zoom ADC employing 1-bit 2nd order ΔΣ modulator.

Fig. 6. Normalized maximum output for 1st integrator versus Bits of coarse ADC.

Fig. 7. Effect of OTA's DC gain and its nonlinearity (a) Proposed zoom ADC (b) 1b 3rd order incremental ΔΣ ADC [2].

Fig. 8. System-level chopping of zoom ADC.

Fig. 9. Block diagram of the proposed zoom ADC.

Fig. 10. Simplified schematic of coarse SAR ADC.

Fig. 11. Simplified schematic of fine incremental ΔΣ modulator.

Fig. 12. Simplified circuit diagram of the inverter-based integrator in the sampling and integration phase.

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Table I. Performance summary and comparison with previous work.

Parameter	**This work**	[3]	[14]	[2]	[12]
Architecture	**Zoom ADC**	Amp+ΔΣ	EC (ΔΣ+SAR)	3rd order ΔΣ	Multibit ΔΣ
Technology	**0.16μm**	0.7μm	0.18μm	0.6μm	0.18-0.6μm
Chip area	**0.375mm^2**	6mm^2	3.5mm^2	2.08mm^2	2.4mm^2
Supply current	**3.5μA**	270μA	21.1mA	120μA	1.8mA
Supply voltage	**1.8V**	5.0V	1.8V	2.7 - 5.0V	3.3V
Conversion time	**40ms**	170ms	1μs	66.7ms	512μs[††]
Input range	**1.8V**	80mV	3.6V	10V	4V
Measured Noise	**0.65μV$_{rms}$**	—	—	2.5μV$_{rms}$	4.13μV$_{rms}$
SNR$_{max}$	**119.8dB**[†]	118dB[†]	89.1dB	123dB[†]	110.7dB[†]
DC offset	**0.5μV (typ)** **1μV (max)**	48nV (typ)	—	2μV (typ) 10μV (max)	1.5μV (typ)
INL	**±6ppm**	±5ppm	±61ppm	±5ppm	—
PSRR	**120dB@DC** **103dB@50Hz**	140dB@DC	—	120dB@DC	—
FoM[†††]	**182.7dB**	151.4dB	160.3dB	166.4dB	162.8dB

[†] Crest-factor corrected SNR$_{max}$=20·log((Max DC Input /$2\sqrt{2}$)/Output Noise).

[††]Calculated

[†††] FoM=SNR$_{max}$+10·log (1/(Power×2T$_{conv}$)),
which is drived from Schreier's *FoM* [27]: FoM=DR+10•log(BW / Power).

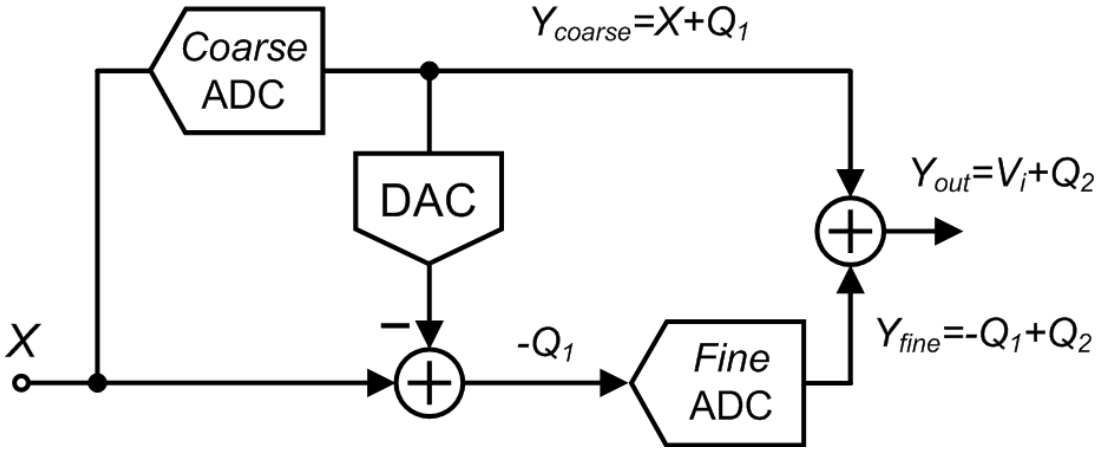


Fig. 1. Block diagram of two-step ADC.

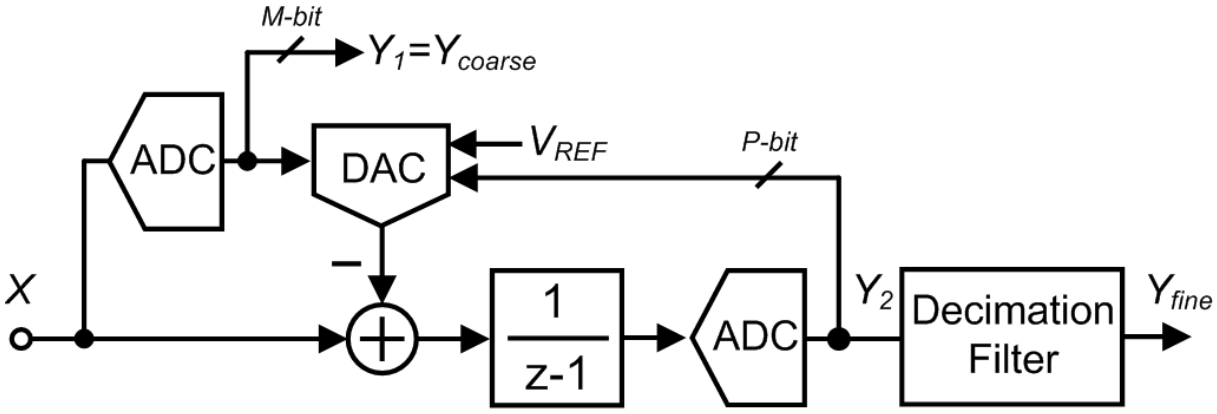


Fig. 2. A zoom ADC employing a 1st order ΔΣ ADC.

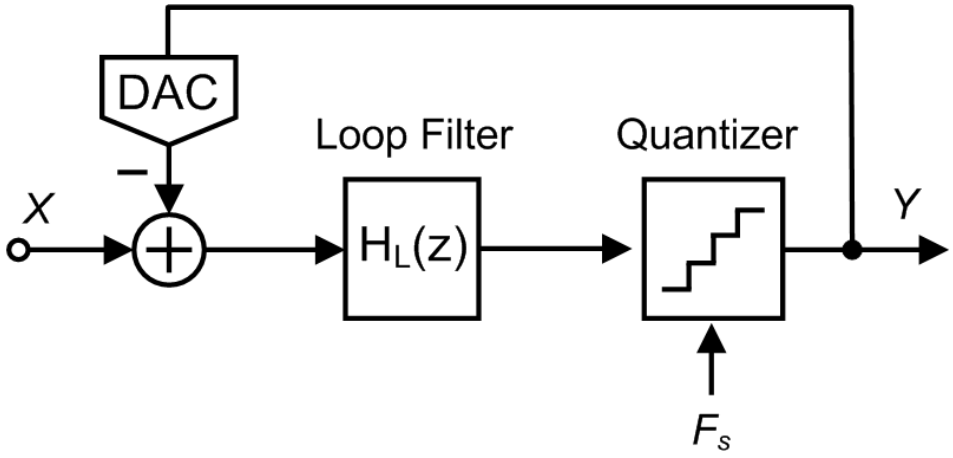


Fig. 3. A basic single-loop ΔΣ modulator.

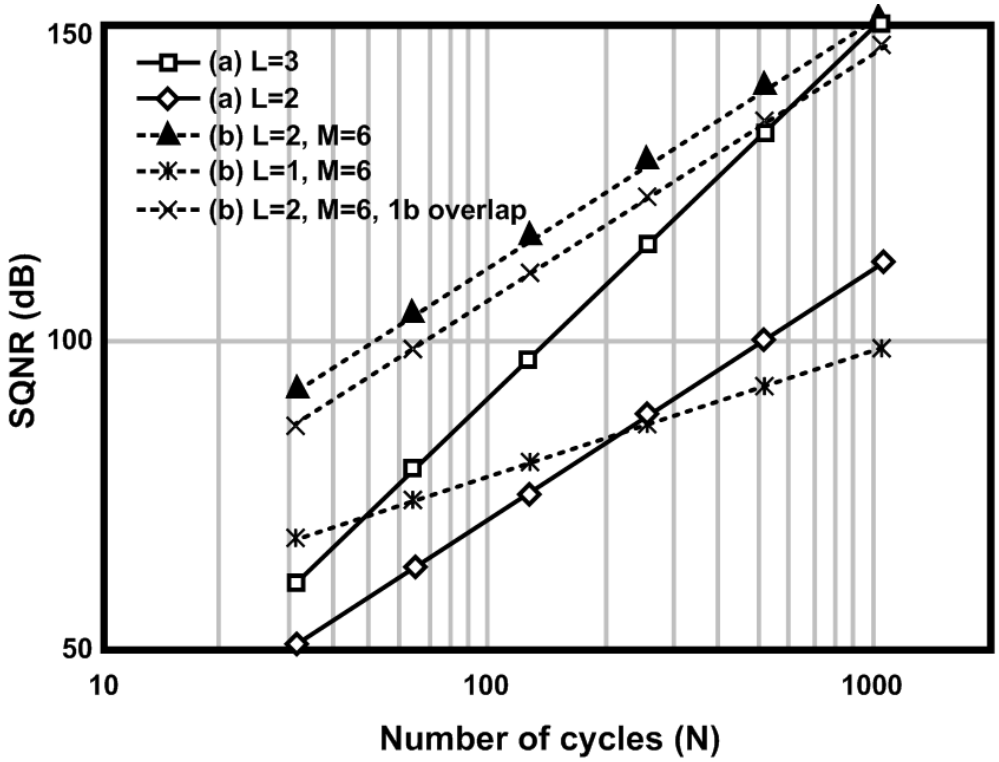


Fig. 4. SQNR versus number of cycles (N), L=Loop filter's order, M=Coarse ADC's bit resolution (a) 1-bit ΔΣ ADCs (b) 1st and 2nd order zoom ADCs.

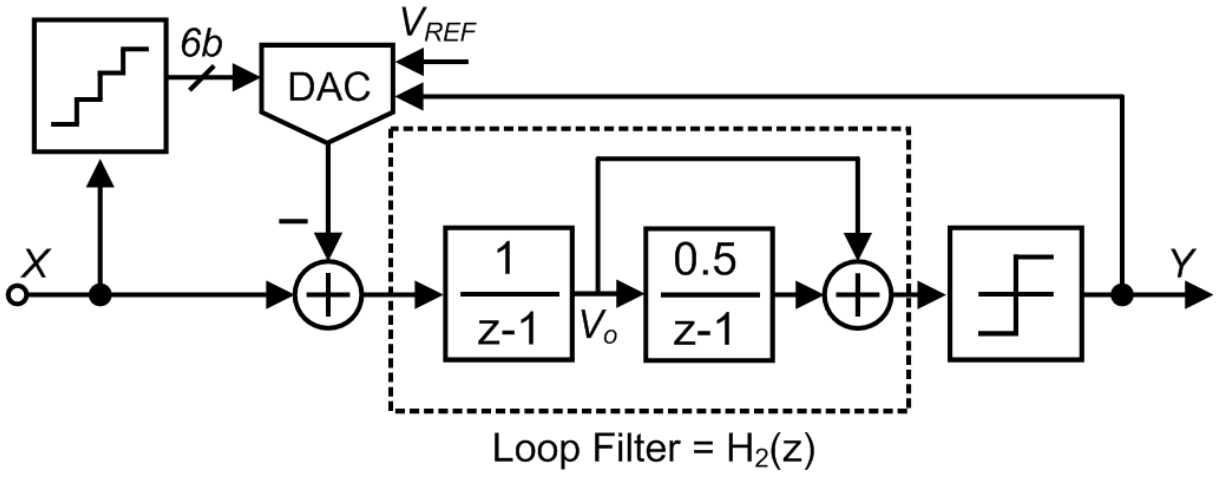


Fig. 5. A zoom ADC employing 1-bit 2nd order ΔΣ modulator.

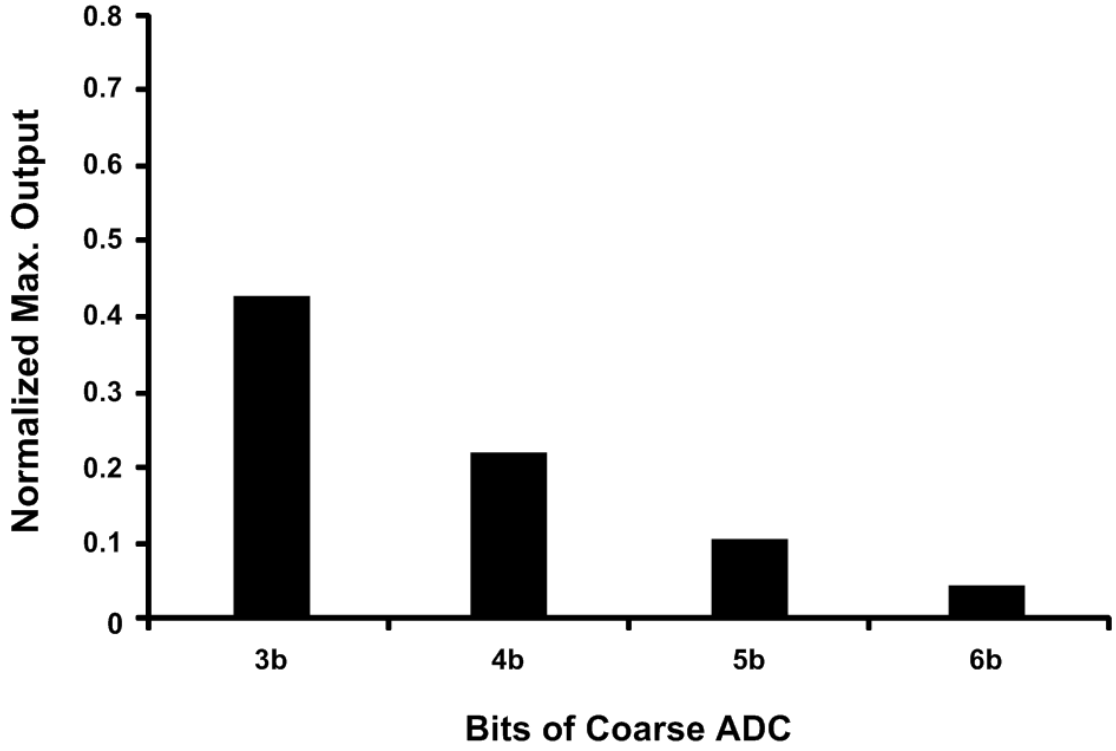
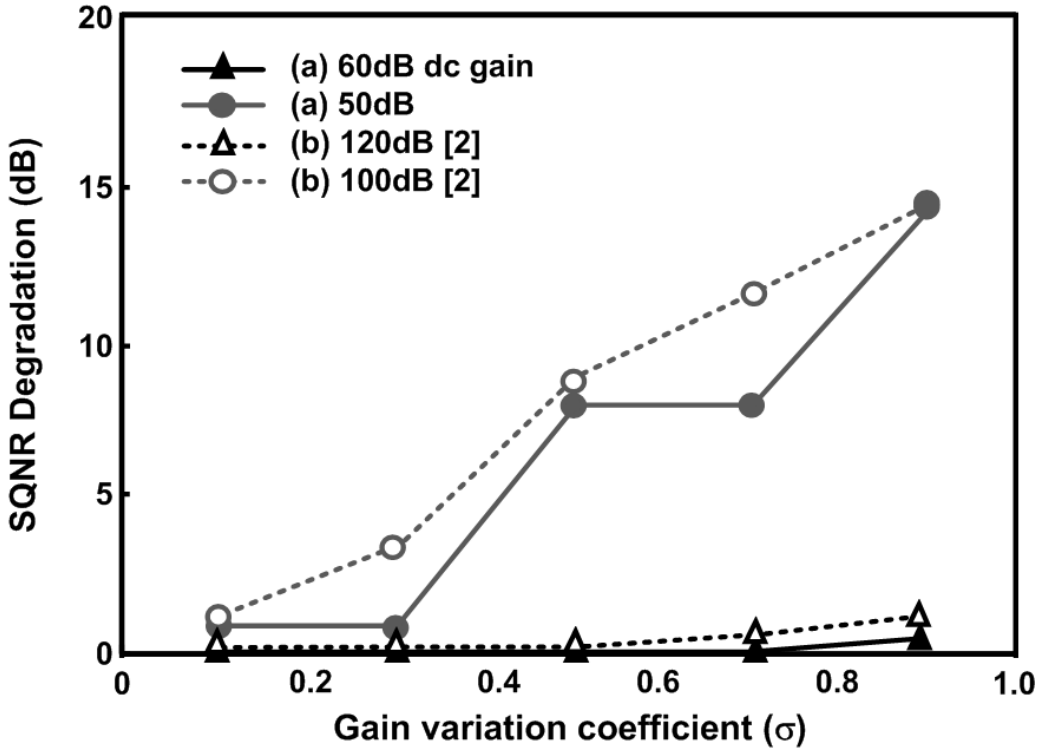


Fig. 6. Normalized maximum output for 1st integrator versus Bits of coarse ADC.



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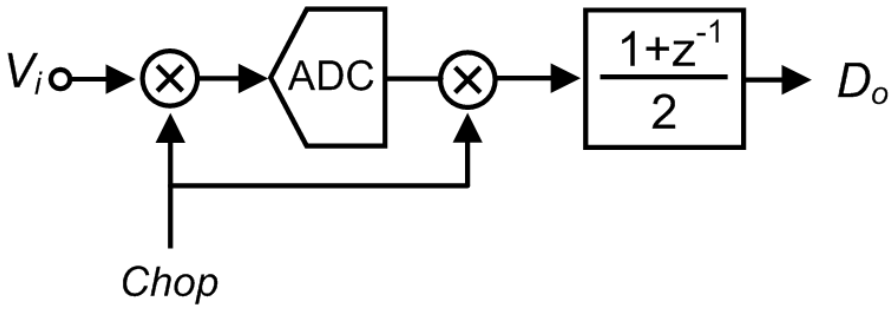


Fig. 8. System-level chopping of zoom ADC.

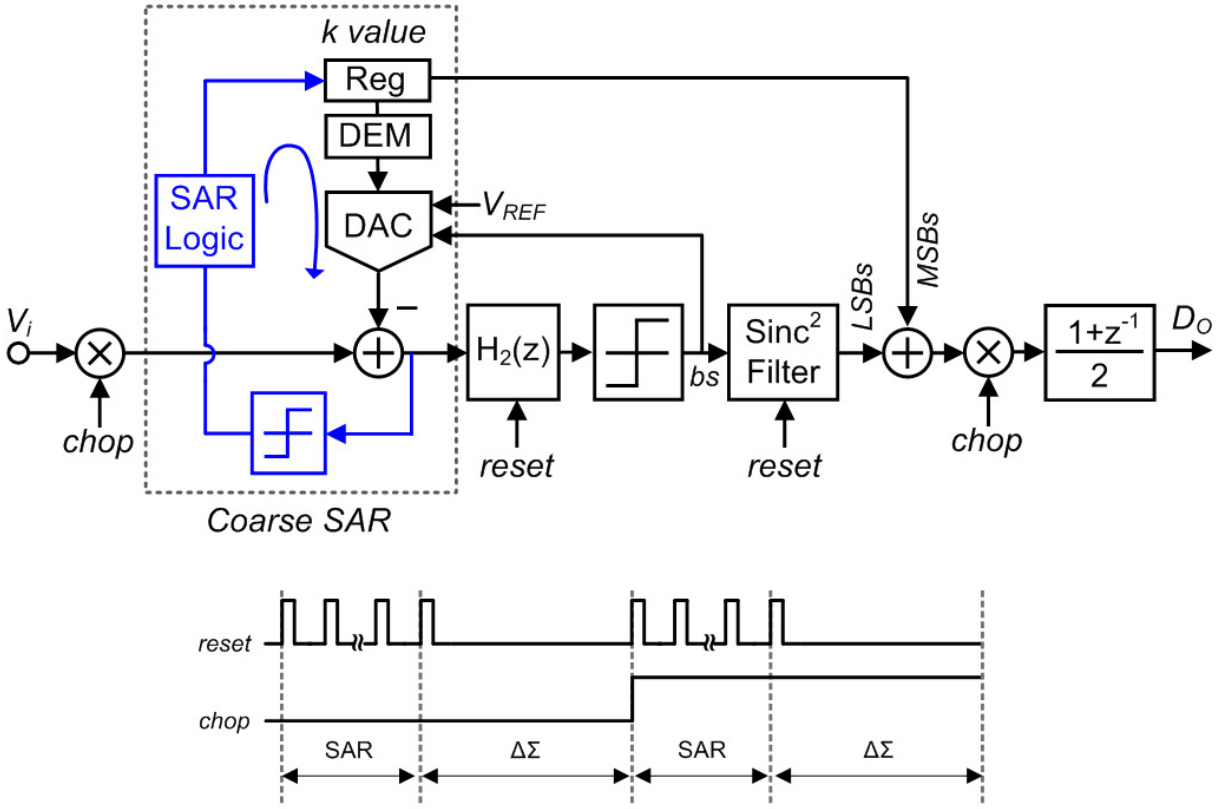


Fig. 9. Block diagram of the proposed zoom ADC.

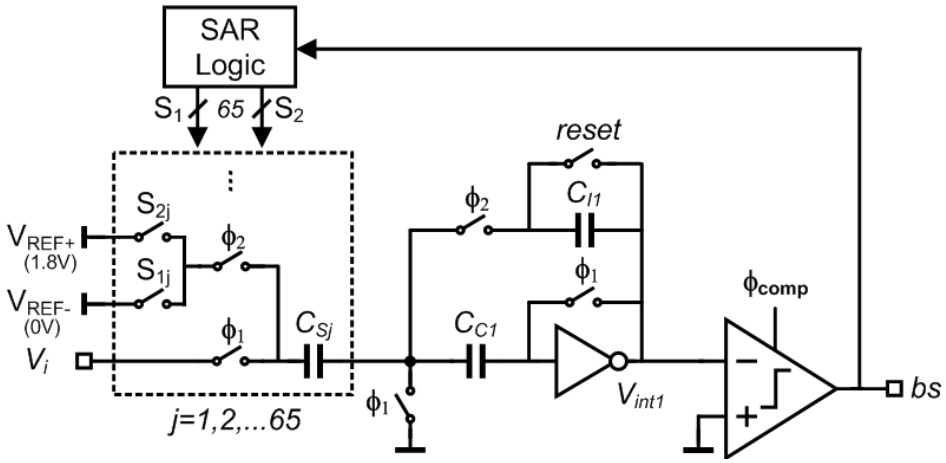


Fig. 10. Simplified schematic of coarse SAR ADC.

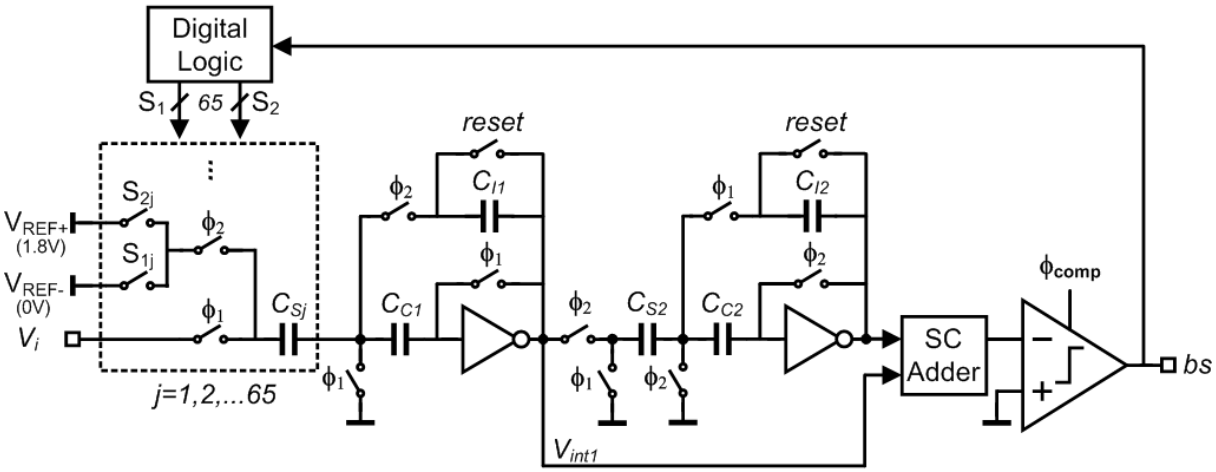


Fig. 11. Simplified schematic of fine incremental ΔΣ modulator.

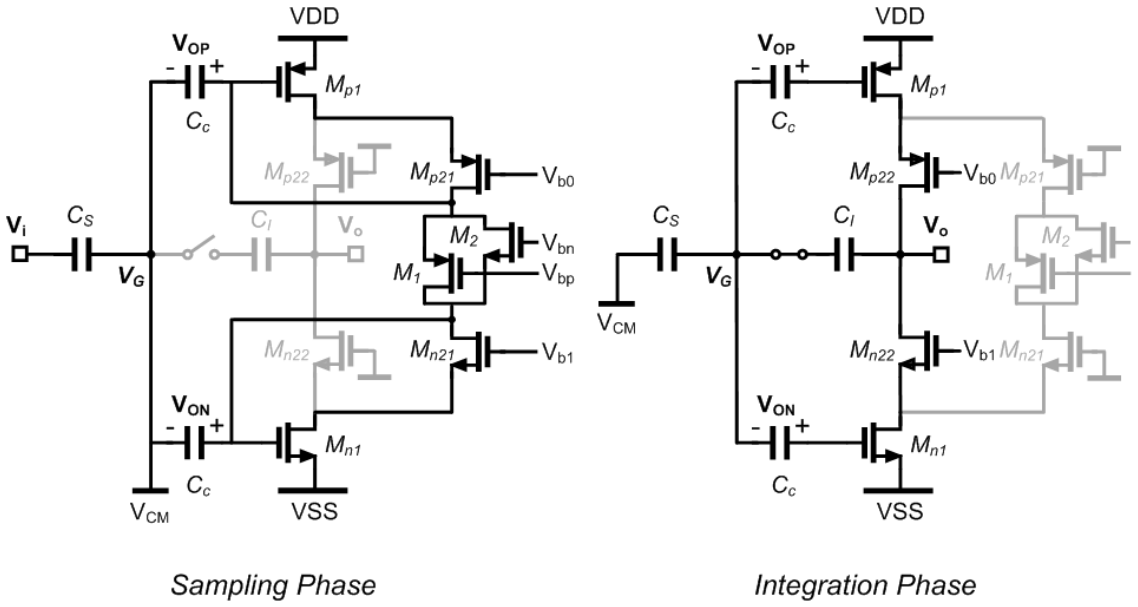


Fig. 12. Simplified circuit diagram of the inverter-based integrator in the sampling and integration phase.

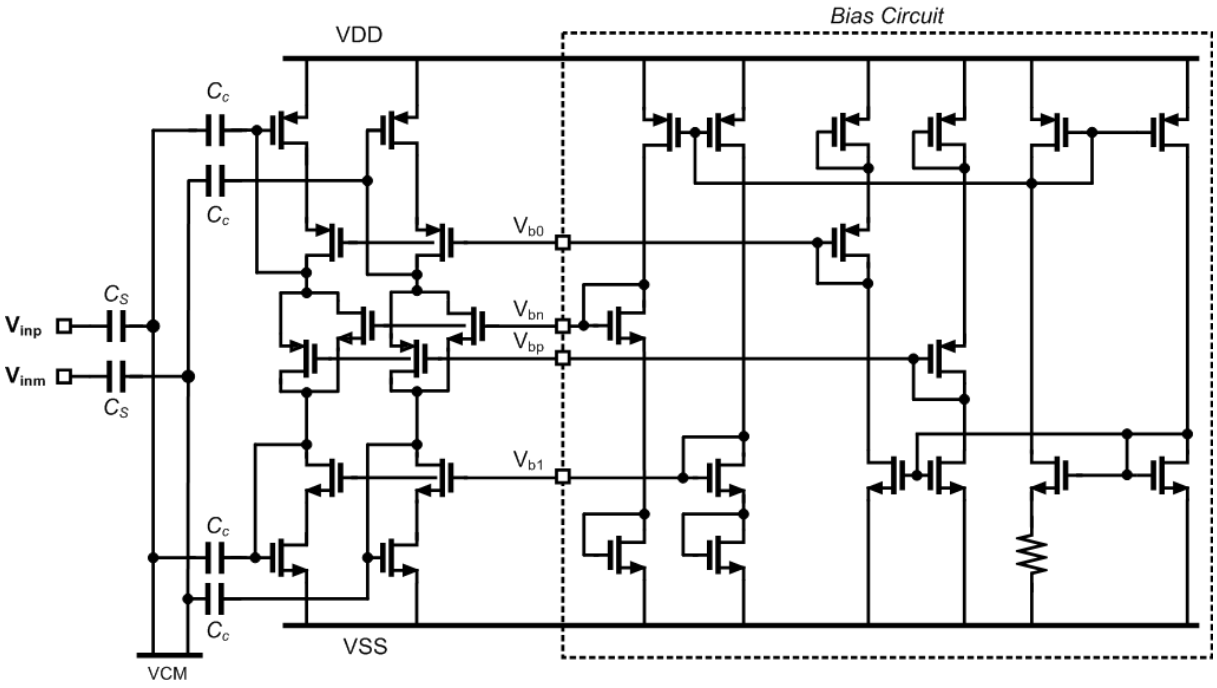


Fig. 13. Circuit diagram of the inverter-based integrator with bias circuit (Sampling phase).

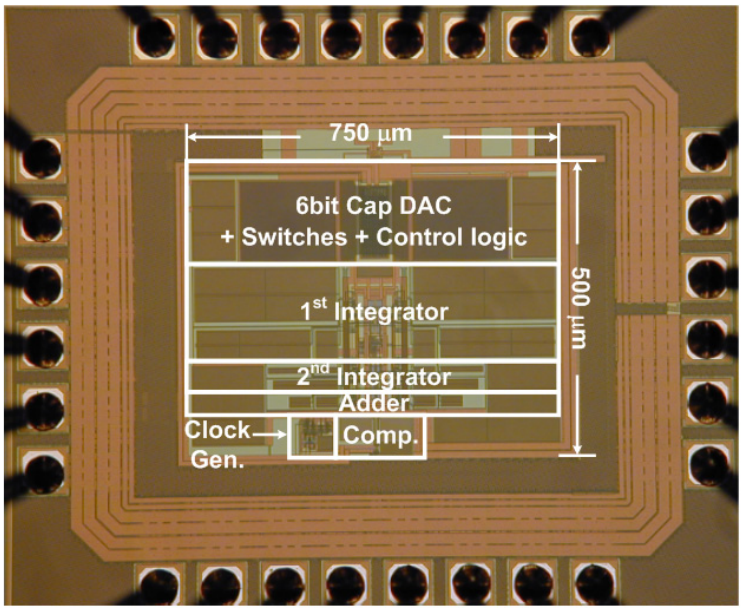


Fig. 14. Chip Micrograph.

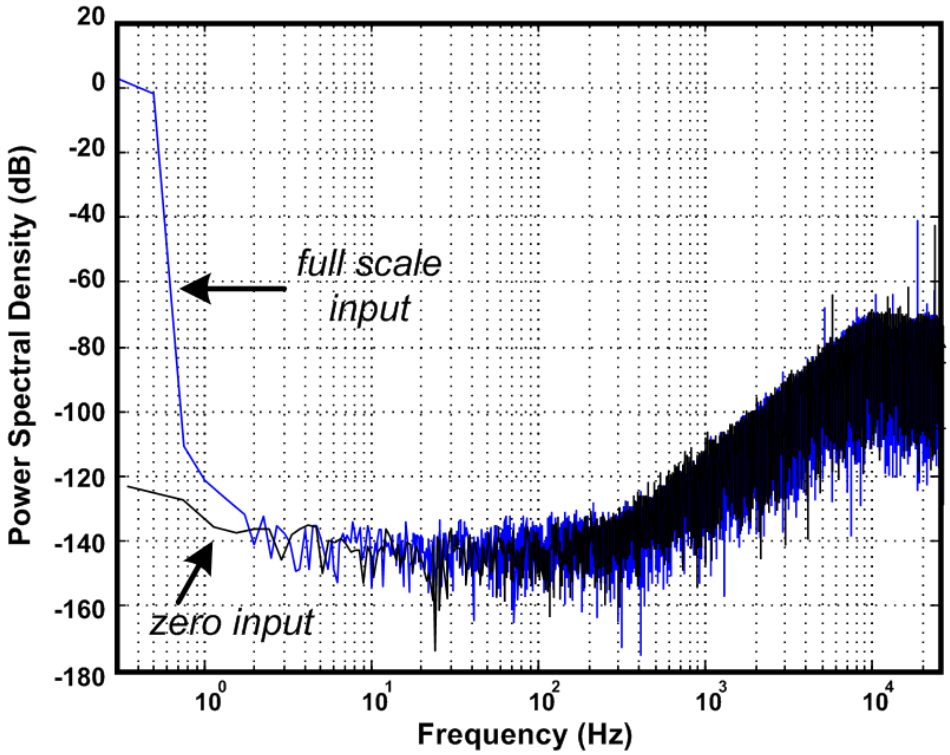


Fig. 15. Measured output spectrum of the free-running ΔΣ modulator with DEM on (2^{16} Samples).

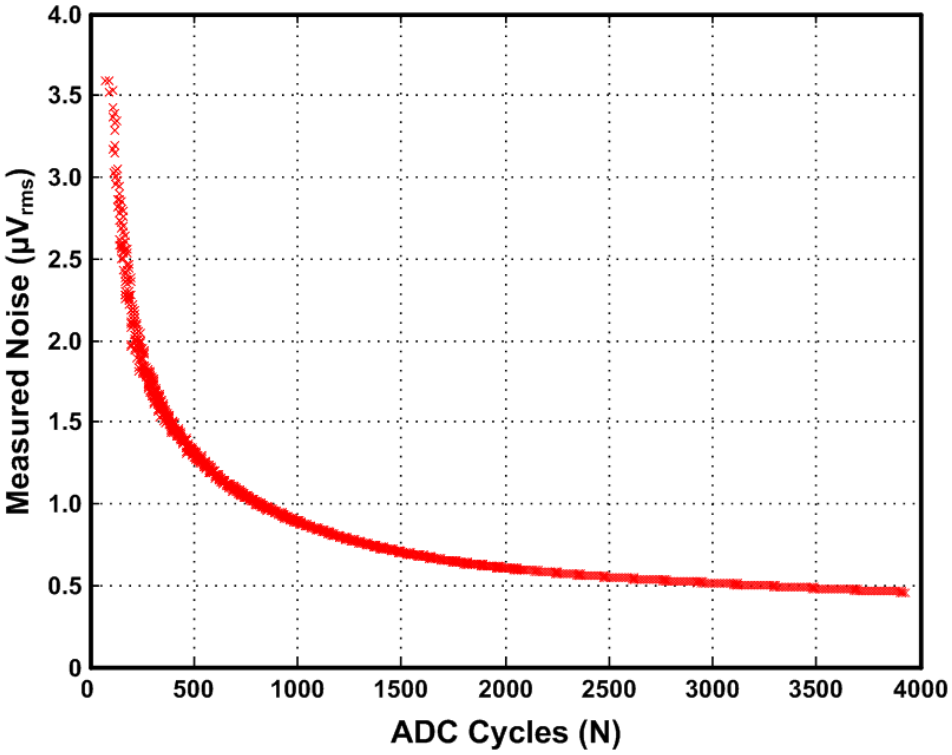
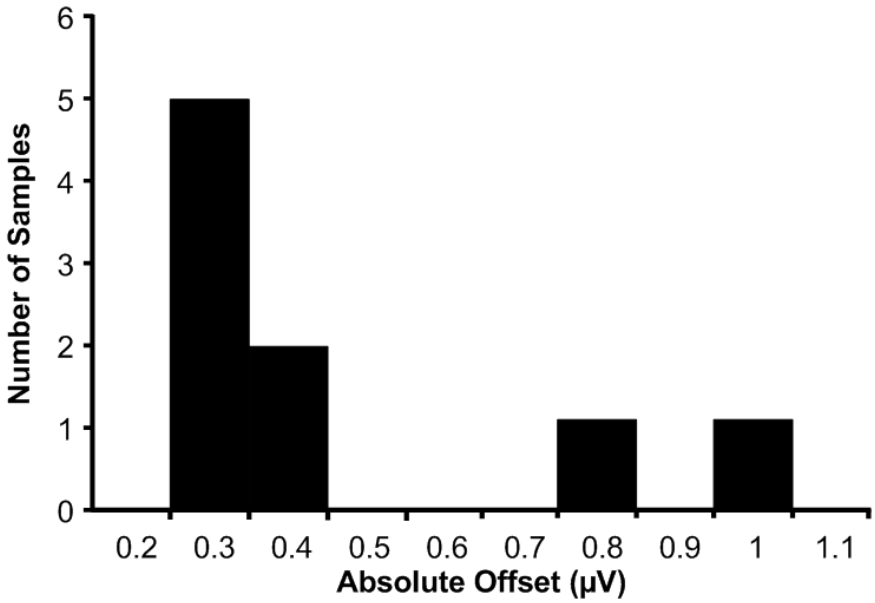


Fig. 16. Measured noise referred to input versus ADC cycles.



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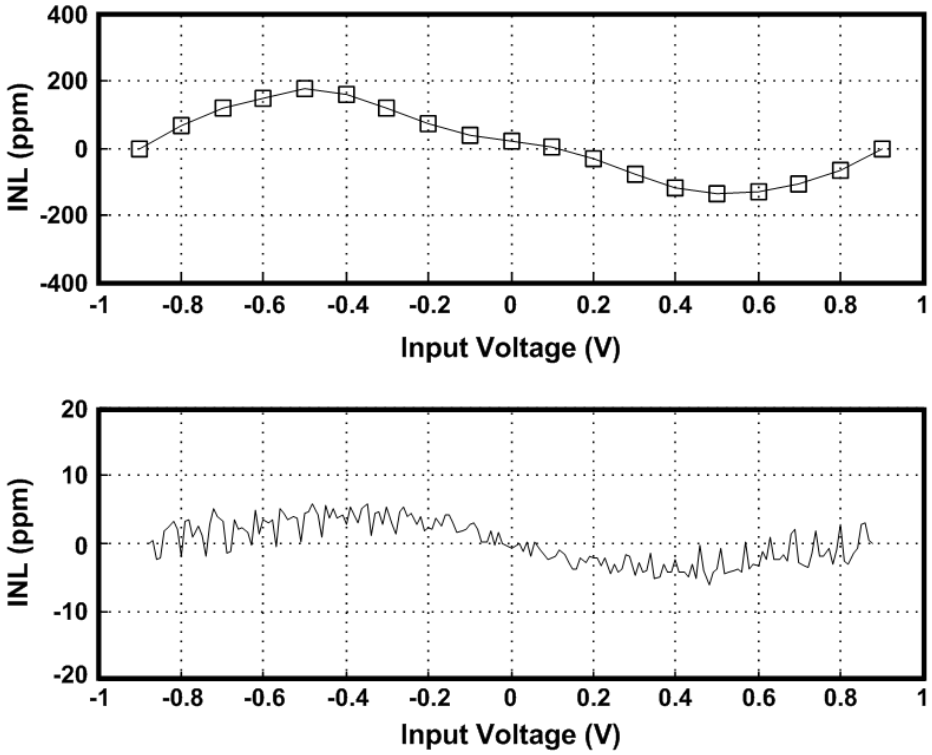

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