January 2009

A 6-Gb/s wireless inter-chip data link using 43-GHz transceivers and bond-wire antennas

Chen Wu-Hsin

Joo Sanghoon

S. Sayilir

R. Willmot

Choi Tae-Young

See next page for additional authors

Wu-Hsin, Chen; Sanghoon, Joo; Sayilir, S.; Willmot, R.; Tae-Young, Choi; Dowon, Kim; Lu, J.; Peroulis, D.; and Byunghoo, Jung, "A 6-Gb/s wireless inter-chip data link using 43-GHz transceivers and bond-wire antennas" (2009). *Department of Electrical and Computer Engineering Faculty Publications.* Paper 6.
http://dx.doi.org/http://dx.doi.org/10.1109/JSSC.2009.2027932

A 6-Gb/s Wireless Inter-Chip Data Link Using 43-GHz Transceivers and Bond-Wire Antennas

Wu-Hsin Chen, *Student Member, IEEE*, Sanghoon Joo, *Student Member, IEEE*, Serkan Sayılır, *Student Member, IEEE*, Russell Willmot, *Student Member, IEEE*, Tae-Young Choi, *Member, IEEE*, Dowon Kim, *Member, IEEE*, Julia Lu, *Student Member, IEEE*, Dimitrios Peroulis, *Member, IEEE*, and Byunghoo Jung, *Member, IEEE*

***Abstract*—A 43-GHz wireless inter-chip data link including antennas, transmitters, and receivers is presented. The industry standard bonding wires are exploited to provide high efficiency and low-cost antennas. This type of antennas can provide an efficient horizontal communication which is hard to achieve using conventional on-chip antennas. The system uses binary amplitude shift keying (ASK) modulation to keep the design compact and power efficient. The transmitter includes a differential to single-ended modulator and a two-stage power amplifier (PA). The receiver includes a low-noise amplifier (LNA), pre-amplifiers, envelope detectors (ED), a variable gain amplifier (VGA), and a comparator. The chip is fabricated in 180-nm SiGe BiCMOS technology. With power-efficient transceivers and low-cost high-performance antennas, the implemented inter-chip link achieves bit-error rate (BER) around 10^{-8} for 6 Gb/s over a distance of 2 cm. The signal-to-noise ratio (SNR) of the recovered signal is about 24 dB with 18 ps of rms jitter. The transmitter and receiver consume 57 mW and 60 mW, respectively, including buffers. The bit energy efficiency excluding test buffers is 17 pJ/bit. The presented work shows the feasibility of a low power high data rate wireless inter-chip data link and wireless heterogeneous multi-chip networks.**

***Index Terms*—Bond-wire antenna, high-speed link, on-chip antenna, wirebond antenna, wireless inter-chip link, wireless transceiver.**

I. Introduction

THE demands for high communication bandwidth in multi-chip systems are ever increasing. A large, complex system consisting of several chips in a module or across a printed-circuit board (PCB) may require up to several tens of Gb/s interconnecting data rate. This increasing data rate results in severe signal attenuation and distortion in electrical channels because of the skin effect, dielectric absorption, and impedance mismatches. The existing solutions are approaching the maximum bandwidth limit of electrical interconnects [1]. There have been efforts to replace the electrical channels with optical connections. Capability for the high bandwidth of the optical link has been proven through their wide deployment in internet backbone (SONET) applications [2]–[5]. However, the optical link requires non-Si devices that can generate and modulate optical signals, and optical waveguides for non-line-of-sight transmission. All of the extra devices increase system complexity and cost. To address the issues, the RF/wireless interconnect concept has been introduced [6], [7]. The RF/wireless data link improves system reliability and flexibility since the signal attenuation in the air is comparable with that of Cu channel in high data rate for relatively short distances [7], and more importantly, its unique broadcasting nature can be exploited in systems that require one-to-many transmissions. Fig. 1 shows a conceptual diagram of a wireless micro network system.

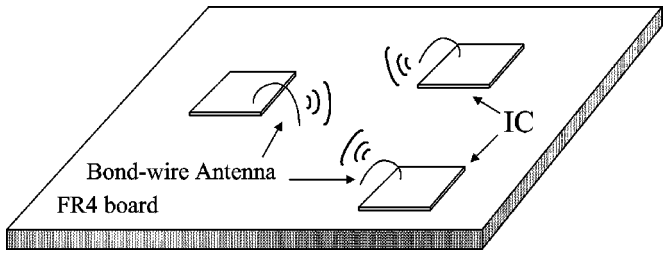


Fig. 1. Conceptual diagram of the on-board inter-chip communication.

With rapid device scaling in recent years, the f_T of RF transistors has increased up to several hundered GHz [8]. Using these RF technologies, many wireless transceivers working in U-band frequencies have been reported [9]–[12]. Since the quarter wavelengthes of the carrier frequencies in this band are in the range of 1.2 to 1.9 mm in free space, and even smaller on the silicon wafer, a monolithically integrated antenna is feasible [13], [14]. An on-chip antenna can reduce the assembly cost and eliminate the external transmission line connection. However, the silicon substrate has a high dielectric constant ($\epsilon_r \sim 11.7$) and low substrate resistivity ($\sim$20 Ω-cm), so on-chip planar antennas either provide low efficiency [15], [16] or require expensive extra process steps to improve the antenna performance [17]–[20]. For instance, the gain of the zigzag antennas used in [15] is about -10-dBi with 10% efficiency. In [17], a special silicon lens is added at the bottom of the chip to improve the gain to 2 dBi. In [18], a costly ion implantation process is added to increase the substrate resistivity and improve the gain to 6.4 dBi. Besides the efficiency and cost issues, the on-chip antennas occupy a significant portion of IC area and provide poor horizontal radiation pattern, which limit their applications in inter-chip communications.

In this paper, we present a fully integrated wireless inter-chip link using bond-wire antennas. The idea of the bond-wire

Manuscript received February 19, 2009; revised May 28, 2009. Current version published September 28, 2009. This paper was approved by Associate Editor Jafar Savoj. This work was performed through the 2007–2008 SRC/SIA IC Design Challenge.

The authors are with the School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47906 USA (e-mail: whchen@purdue.edu).

Digital Object Identifier 10.1109/JSSC.2009.2027932

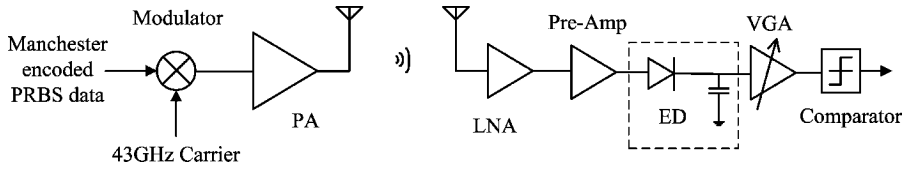


Fig. 2. Architecture of the transceiver.

antenna is first introduced in a U.S. patent in 2004 without implementation[21]. We have implemented bond-wire antennas and combined them with 43-GHz transceivers to create a short distance, high-speed communication link. The transceiver is implemented in 180-nm SiGe BiCMOS technology. To demonstrate its compatibility with standard technologies, the ICs are mounted on FR4 PCBs using a standard chip-on-board packag. The same packaging technique is used to form the bond-wire antennas. The bond-wire antenna effectively addresses several major issues in wireless inter-chip data link design such as on-chip area penalty, cost, and efficiency, especially in the horizontal direction.

Another important issue to be addressed for successful deployment is low-power implementation. Power consumption comparable with that of wired link is highly desirable. The high efficiency of the bond-wire antennas helps save power since it reduces the undesirable power loss in antennas. A low-power transceiver design is also crucial. The proposed transceiver adopts an ASK modulator and a non-coherent receiver for the ASK modulated signal because its compact architecture allows for a power-efficient implementation. Also, the wide baseband spectrum makes the modulation schemes and coherent receivers that require Nyquist rate data converters and high-speed digital processing with a limited power budget impractical. Hence the high target data rate in the multi-Gb/s range limits the choices in modulation schemes and types of receivers. Although non-coherent receivers are more sensitive to noise and interferences compared with coherent receivers, the issue can be mitigated by properly shielding the system, which is feasible because of the minuscule size of typical multi-chip systems[22].

The rest of the paper is organized as follows. Section II describes the transceiver architecture. Section III highlights the design and performance of bond-wire antennas. The circuit details in 180-nm SiGe BiCMOS technology are presented in Section IV. Section V shows the measurement results, followed by conclusions.

II. System Architecture

The block diagram of the transceiver system is shown in Fig. 2. Input data generated from a Pseudo Random Bit Sequence (PRBS) generator is modulated using an ASK modulator and amplified by a two-stage PA before transmitting through the bond-wire antenna. The modulator also serves as a differential to single-ended converter. The PA amplifies the modulated signal up to 0 dBm and sends it to the impedance matched antenna. Another bond-wire antenna receives the signal and passes the signal through a non-coherent receiver that demodulates and recovers the envelope of the transmitted signal. The pre-amplifier, consisting of a cascaded pair of a common emitter and an emitter follower, provides extra gain to guarantee that the amplified signal is larger than the threshold of the envelop detector (ED). A bipolar transistor based ED directly demodulates the high-speed signal and down-converts it to baseband. The VGA following the ED has a 35-dB dynamic range, so the gain of the receiver chain may vary from 50 dB to 85 dB. A comparator works as a one-bit quantizer that recovers the logic level of the input signals. It also converts the single-ended signals to differential output. The non-coherent receiver does not require a complicated local oscillation signal generator and fine phase alignment circuits. The simple architecture results in a compact low-power implementation. Also, ASK modulation has less stringent requirements on the linearity of the PA and receivers. During the simulation and design, Manchester coding is used to evenly distribute the ones and zeros in the PRBS data and maintain the DC bias point in the ED.

We assume that a line-of-sight path is dominant, and estimate the channel loss using the free space loss formula. At 43 GHz, the path loss in the 10-cm channel is about 45 dB. Assuming that the antenna gain is 0.4 dBi (from [23]), the output power of the PA is 0 dBm, and the miscellaneous margin, including multi-path fading, antenna mismatch and PCB body loss, is 20 dB, the signal power at the receiver input with the targeted 10-cm channel distance would be -64.2 dBm (about 0.4 mV on 50 Ω). This value defines the necessary sensitivity of the receiver, which will be discussed in following sections.

III. Bond-Wire Antenna

To create a successful chip-to-chip data link, there are several key considerations that impact the antenna. To send and receive signals between two chips on the same PCB, the antenna must have a relatively high gain in the direction parallel to the surface of the PCB. Antenna gain is a function of position relative to the antenna that describes how well that antenna radiates power to that location. The antenna must also be fairly efficient so that there is freedom to separate the two chips and so that the antenna may operate consuming as little power as possible. This rules out many of the planar antenna designs because they have poor radiation efficiency in the horizontal plane.

The antenna we used is a 25-μm thick round wire bent into a semicircle[23]. The length of the wire is $\lambda/2$ at the operating frequency. The antenna was modeled with Ansoft HFSS FEM [24] software. Fig. 3 shows the structure we used in HFSS simulation. In order for the antenna to function properly, the end of the antenna that is not being fed must be grounded. A patch of grounded metal with an area of $0.07\lambda^2$ was added underneath the antenna. This allowed for the end of the antenna to be grounded without creating a radiating environment that differed significantly from the surface of the silicon chip, since the chip

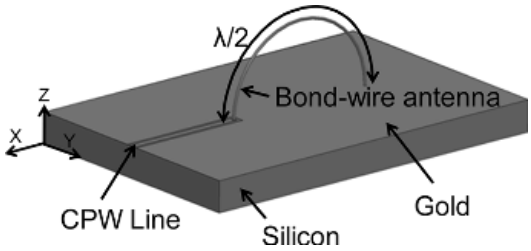


Fig. 3. Diagram of a sample bond-wire antenna.

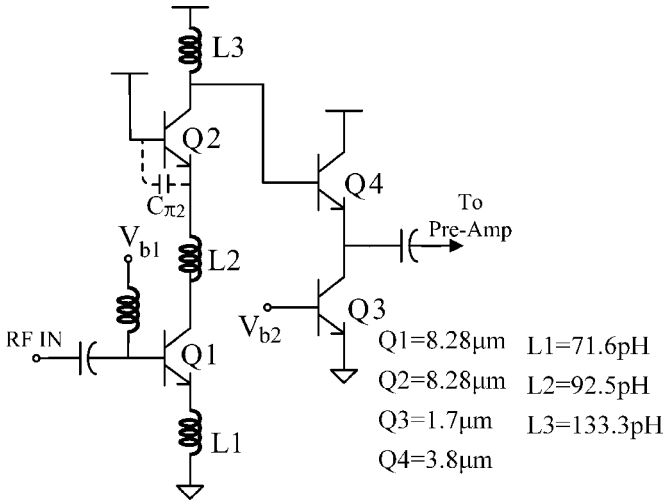


Fig. 4. Schematic of the LNA.

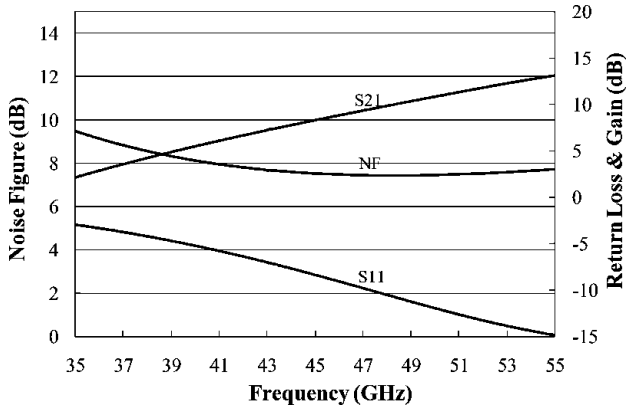


Fig. 5. Simulated gain, noise figure, and return loss of the LNA.

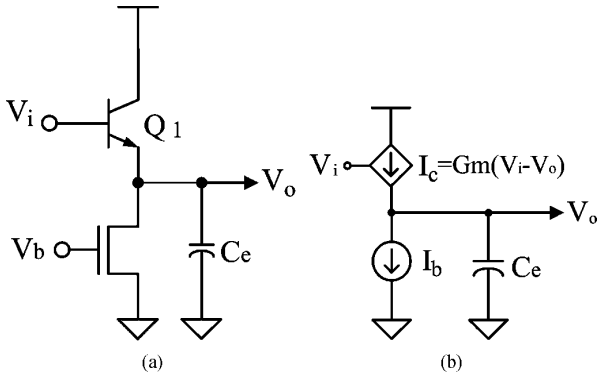


Fig. 6. (a) Schematic of the envelope detector. (b) Simplified model for the envelope detector.

does not have a large grounded metal on its top surface. The simulated radiation pattern is elliptical in shape with a maximum of 2 dBi and a minimum of −2.5 dBi. The 2-dBi gain is observed along the axis of the loop.

Samples of the antenna were fabricated separately from the transceiver chip to test the characteristics of the antenna alone, as discussed in [23]. A custom test fixture was used to measure the gain of the antenna using the two-antenna method [25]. Radiation patterns were measured in two planes, the E-plane (or elevation plane), and the H-plane (or azimuth). The Friis Transmission Equation was applied to the measured S_{21} values to calculate the gain values.

The radiation efficiency of an antenna is equal to the maximum gain divided by the directivity, but only the maximum gain can be measured directly with the test fixture. Therefore, the radiation efficiency of an antenna had to be extracted using the measured maximum gain values and the simulated directivity values from HFSS. The measured performances of the bond-wire antennas integrated with the transceiver will be shown in Section V.

IV. Circuit Implementation

A. Low-Noise Amplifier

A inductively degenerated cascode topology was chosen for the LNA. The schematic of the LNA is shown in Fig. 4. An emitter follower is added at the output of the cascode amplifier to increase the load impedance of the first stage so that the LNA has better gain and noise figure. To further improve the performance of the LNA, an inductor L2 is added between the CE and CB stages. L2 enhances the bandwidth by separating the parasitic capacitance at the collector of Q1 from the one at the emitter of Q2 [26]. By properly choosing the size of the transistor Q2, the base-emitter capacitance, $C_{\pi 2}$, can be tuned out to reduce the signal leakage to the base of Q2. Thus, the gain of the LNA can be increased [27]. Fig. 5 shows the simulated gain, noise figure, and return loss of the LNA.

B. Envelope Detector

A traditional diode-connected ED is not suitable for high-speed serial link applications due to its high voltage drop and limited switching speed. Therefore, the PN junction of a bipolar transistor is employed to replace the diode, as shown in Fig. 6(a). The simplified model of the ED is shown in Fig. 6(b). From this model, we get

$$\Delta V_o \approx \frac{(V_i - V_o) \times G_m - I_b}{C_e} \tag{1}$$

indicating that the bandwidth of the envelope detector is determined by I_b and C_e. The current source I_b operates as a reference and the transistor Q1 works as a charge pump. If the average current injected into the capacitor through the transistor Q1 is larger than I_b, the output voltage V_o increases. Otherwise, V_o decreases [28]. The pattern of the incoming data affects the bias voltage of the output V_o. Since this type of data-dependent

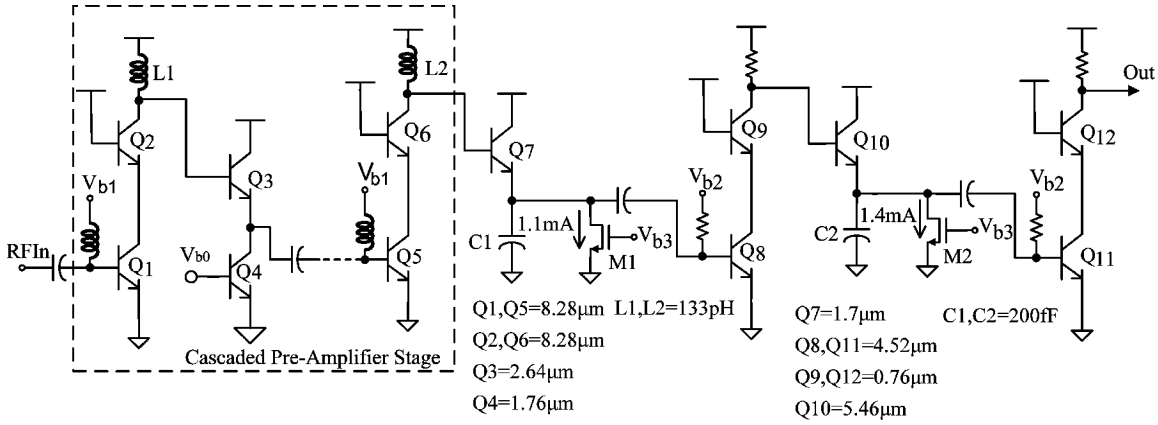


Fig. 7. Schematic of the cascaded pre-amplifiers and envelope detectors.

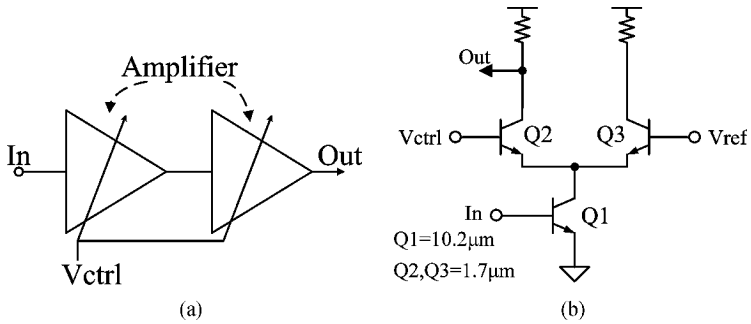


Fig. 8. Two-stage variable gain amplifier. (a) Block diagram. (b) Circuits of amplifier.

fluctuation in DC bias voltage is detrimental for the system performance, Manchester coding is used to balance the numbers of ones and zeros and suppress long consecutive signals in the same value.

Because the sensitivity of the receiver is determined by the minimum detectable voltage of the ED and the gain in the previous stages, the envelop detector chain cascades four pre-amplifiers and two ED and baseband amplifier pairs to increase the minimum detectable input signal, as shown in Fig. 7. The four pre-amplifiers (only two are shown in the figure to simplify the schematic) located in front of the ED chain provide 22.7-dB gain increasing the sensitivity of the receiver chain while the cascaded ED and amplifier pair further increases the dynamic range of the receiver chain. When the amplitude of the input signal is large enough to be recovered by the first ED, the following stages work as amplifiers and the second ED has a negligible effect on the signal. If the output of the first ED is weak and contains a significant level of the residual carrier signal, the baseband portion of the signal is amplified and the residual carrier signal is suppressed by the following amplifier. This improves the sensitivity of the ED chain by helping the operation of the second ED. The minimum detectable signal of the envelop detector chain is 10 mV peak to peak. Combining with the gain provided by the LNA and pre-amplifiers, the sensitivity of the receiver is about 0.32 mV, or -66-dBm, which is slightly better than the required sensitivity of the receiver derived in the link budge analysis in Section II.

C. Variable Gain Amplifier

The VGA is constructed by cascading two cascode amplifiers to improve its dynamic range, as shown in Fig. 8(a). Fig. 8(b) shows the schematic of the gain-control amplifier. The signal current in Q1 is the combination of the current in Q2 and Q3, so the power of the signal is split into two transistors. Therefore, the gain of the amplifier can be adjusted by controlling the current ratio between Q1 and Q2. The current ratio between Q1 and Q2 can be described as

$$\frac{I_{Q2}}{I_{Q1}} = \frac{1}{1+\exp\left(\frac{V_{\mathrm{ctrl}}-V_{\mathrm{ref}}}{V_T}\right)} \tag{2}$$

where V_T is the threshold voltage of the transistor. The relationship between the gain and V_{ctrl} is shown in Fig. 9. As depicted in (2), the gain is an exponential function of the control voltage. This type of VGA provides wide gain control range at the expense of low linearity and high sensitivity to the noise on the control signal [29]. The large gain in the previous stages diminishes the concern on the noise, and an extra shunt capacitor is added to suppress the noise on the control signal.

D. Comparator

A wideband comparator is added to detect the small transitions around the threshold voltage in a noisy environment and convert the analog signals into digital signals. It also transfers the single-ended analog signal to a differential digital signal by

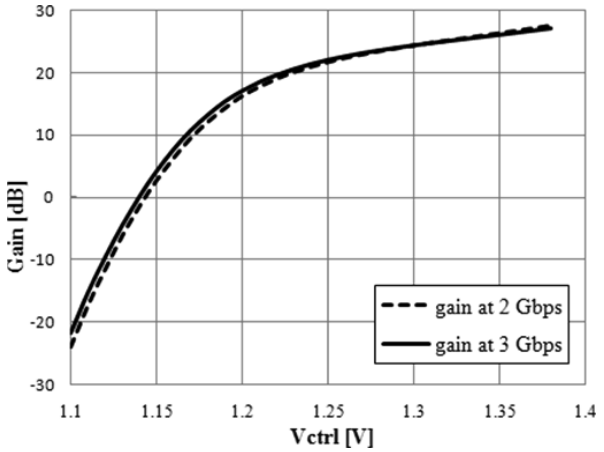


Fig. 9. Simulated VGA gain versus different control voltages for 2 Gb/s and 3 Gb/s.

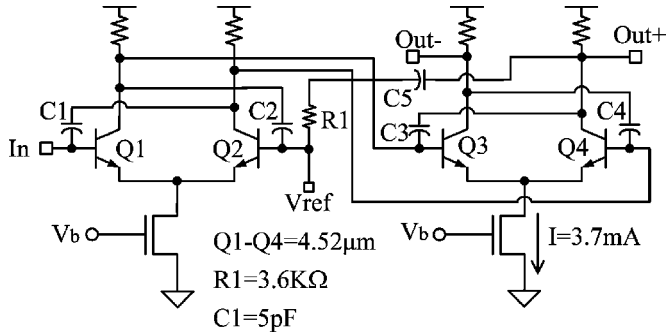


Fig. 10. Schematic of the comparator.

comparing the input signal with a reference voltage. Two differential amplifiers with four feed-forward capacitors, C1, C2, C3 and C4 are cascaded to form the wideband comparator, as shown in Fig. 10. One of the main concerns in comparator design is preventing unwanted output transitions caused by the noise around the threshold voltage. Therefore, two passive components, R1 and C5, are added to the feedback path from the output to $V_{\rm ref}$ creating a hysteresis region around the threshold. The hysteresis is set to 60 mV.

E. Modulator

The schematic of the modulator is shown in Fig. 11. A current steering switch controlled by input data is employed to perform ASK modulation and convert the differential input to a single-ended signal. When the data goes high, the transistor Q1 turns on whereas Q2 turns off. The current generated by Q3 flows through Q1 and the carrier signal appears at the output. On the contrary, when the data is low, Q1 turns off and Q2 turns on, the current flows through Q2, so no signal appears at node *B*. The inductor L1 is tuned to form a single-stage LC resonator with the parasitic capacitances at node *B* to increase the gain.

Because of the high data rate and carrier frequency, it is necessary to improve the bandwidth of the switch. Note that without a load at the collector of the transistor Q2, the right branch works as an emitter follower and the left branch works as a common base amplifier. Since the bandwidth of the emitter follower is higher than that of common base amplifier, the voltage at node

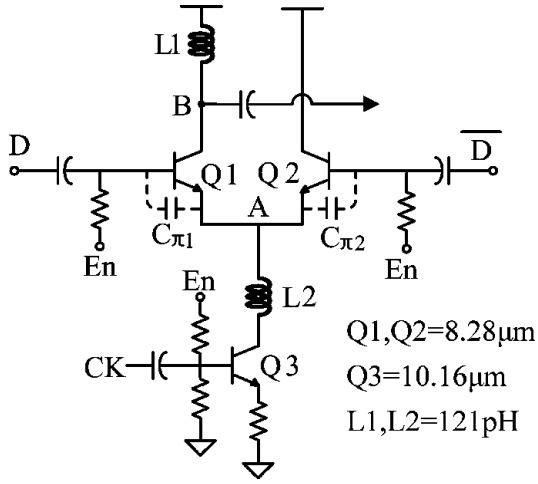


Fig. 11. Schematic of the current steering modulator.

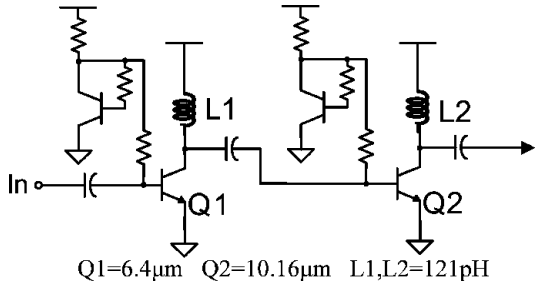


Fig. 12. Schematic of the two-stage power amplifier.

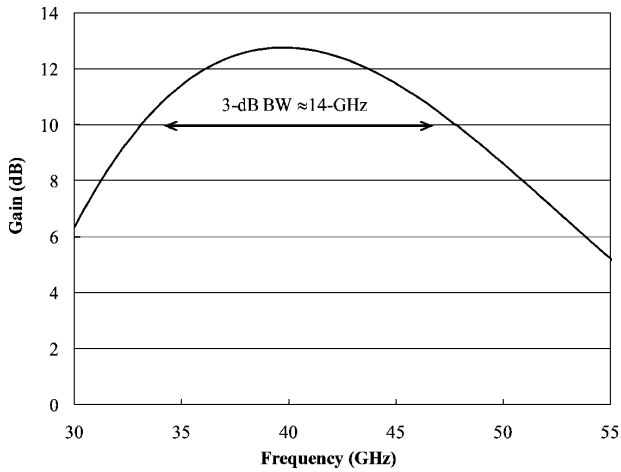


Fig. 13. Bandwidth of the transmitter.

A follows $\overline{D}$. With the differential input signal, the switching speed of the analog switch is higher than a single common base amplifier. To improve the switching speed further, the inductor L2 is added to increase the impedance at node *A* , so the internal parasitic capacitances of Q1 and Q2, named $C_{\pi 1}$ and $C_{\pi 2}$ respectively, are discharged faster through the inductor L2 during the switching operations.

F. Power Amplifier

The schematic of the PA is shown in Fig. 12. Two type-A amplifiers with common source configuration are cascaded

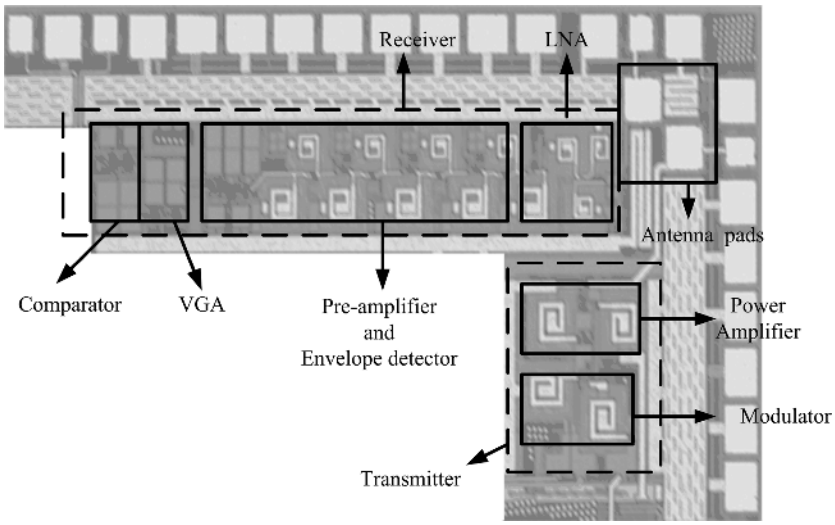


Fig. 14. Transceiver microphotograph.

[30]. Although type-A amplifiers have lower power efficiency compared to other power amplifier types, its superior frequency response is important in high-frequency wideband applications. The first stage of the amplifier works as a driver that isolates the PA from the modulator and the second stage is designed for driving the antenna with maximum efficiency. Each stage has its own bias circuit that is placed nearby for good thermal matching. The bias circuit uses a current mirror structure to reduce the base impedance and hence increase the breakdown voltage $\mathrm{BV_{CEO}}$ [31]. Both of the two transistors have single emitter stripe with minimum width of 0.2 μm. Instead of using a transmission line matching network, a single-stage L-network including a load inductor and a metal–insulator–metal (MIM) capacitor is employed for the inter-stage and output stage impedance matching, as in the modulator part. This simple matching network minimizes the parasitic impedance which is crucial in U-band or higher frequency circuit design [32]. The maximum output power of the PA is 0 dBm in good matching condition with the ON/OFF ratio of 28 dB. The output transistor draws 10 mA from the power supply with 1-mA collector current per 1-μm emitter length in which the maximum f_T is achieved.

Fig. 13 shows the gain simulation result of the transmitter, including the modulator and the PA. The 3-dB bandwidth is about 14 GHz and the gain at 43 GHz is around 12 dB.

V. Measurement Results

The transceiver is fabricated in Jazz 180-nm SiGe BiCMOS technology with an f_T of 155 GHz for the bipolar transistor. The die photo of the transceiver is shown in Fig. 14. The total area is approximately 0.62-mm^2. The ICs were mounted on FR4 test boards using a standard chip-on-board packaging technique. Two types of PCBs were designed to test the transceiver. The first PCB has both the transmitter and receiver on it, where the distance between them is fixed to 0.5 cm. This is used to characterize the antenna performance in a more realistic condition. In the second setup, the transmitter and receiver are mounted on two separate PCBs. The two-board setup are used to measure the performance of the wireless link at different communication distances. The power supplies of the transmitter and receiver boards are completely separated to prevent signal leakage through wired paths. Fig. 15 shows a close look of the transceiver ICs and the antennas on the board. The same bonding technique is used to form the bond-wire antennas. The length of the bond-wire antenna is set to 3.5 mm, which is approximately the half wavelength of the 43-GHz carrier.

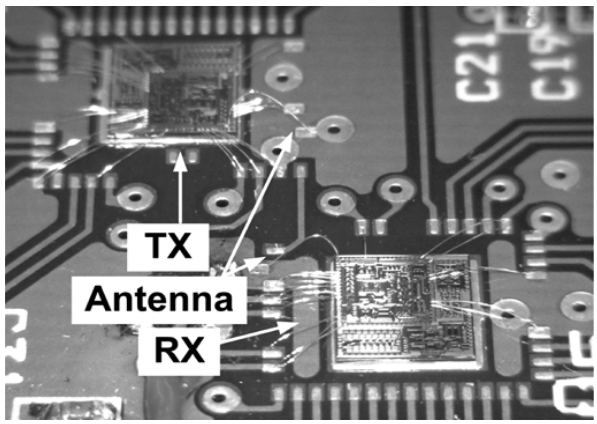


Fig. 15. A close look for the transceiver ICs and bond-wire antennas on the PCB.

Fig. 16 illustrates the setup for measuring the performance of the wireless inter-chip link. The 43-GHz carrier is provided by the network analyzer and is fed to the transmiter through a 67-GHz GSG probe. The input random pattern is generated by an Agilent 71612 PRBS generator/BER analyzer. This PRBS generator does not support any coding methods, so the test pattern with Manchester coding is generated in a computer and loaded into the pattern generator. Because of the limited RAM size in the BER analyzer, the maximum length of the PRBS code we are able to load is $2^{15}-1$. The receiver output data is sent back to the BER analyzer for comparison through a GSG probe

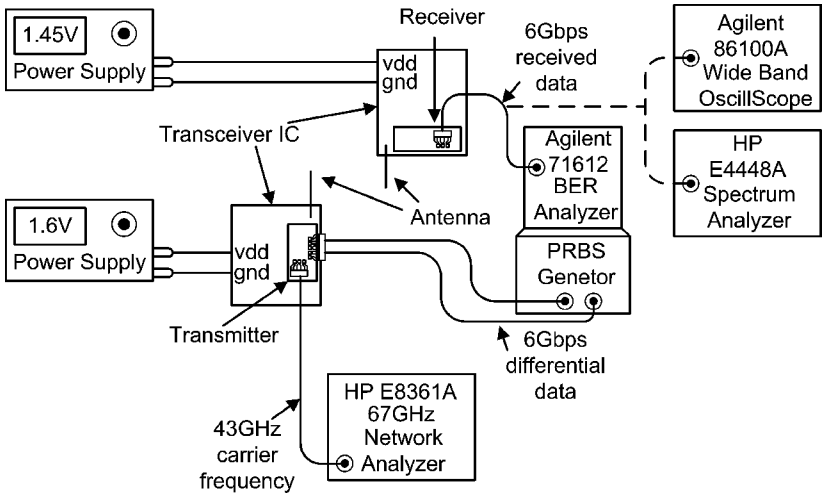


Fig. 16. Wireless data link test setup.

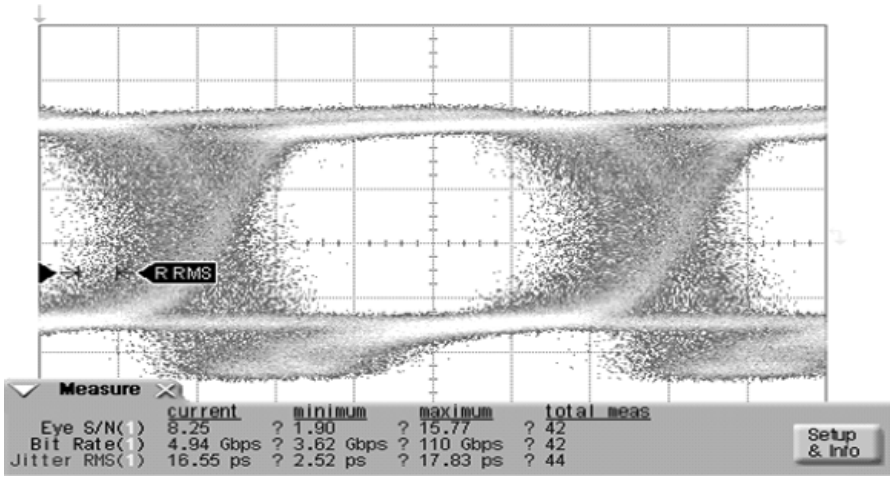


Fig. 17. Measured eye diagram of the recovered data when the data rate is 5 Gb/s at 2 cm.

and a SMA cable. All of the high-speed signals are provided or measured through high-speed probes.

The performance of the wireless data link is evaluated by eye diagram and BER measurements in different communication distances, from 0.5 cm to 4 cm. Fig. 17 shows the eye diagram of the receiver output at 5 Gb/s when the distance is set to 2 cm. The SNR is about 24 dB with 17.8 ps of rms jitter and the BER is about 2.6×10^{-11}. The measured BER with respect to transmitting data rate and distance is shown in Fig. 18. At 0.5 cm, the error rate is as low as 4×10^{-13} with 2 Gb/s and increases to 4×10^{-10} at 6 Gb/s. When the distance is shorter than 2 cm, the transceiver provides a BER of 10^{-11} with 5 Gb/s or lower data rate. For a BER of 10^{-3}, the data rate reaches about 6 Gb/s at 3 cm and about 5 Gb/s at 4 cm. When measuring the performance of the transceiver, the VGA was tuned to the optimal value to get the best result.

As depicted in Fig. 18, in some cases, the BER of a lower data rate is worse than that of a higher data rate for a fixed communication distance. This is closely related with a multi-path effect. Due to the limited space on the probe station, one RF probe was hanging on top of the wireless channel about 1 cm away from the PCB surface, creating a multi-path environment

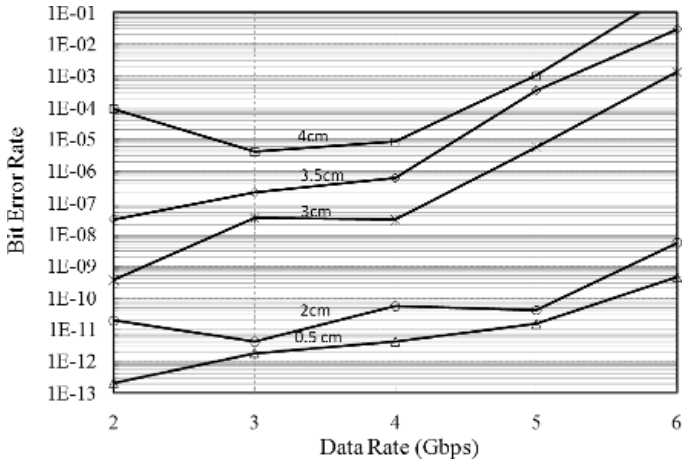


Fig. 18. Measured BER versus data rate in the face of different channel lengths.

for the signal to travel. Fig. 19 shows an eye diagram that shows the BER drop due to the multi-path effect. It has a cluster of noise around the eye center area. This noise shows the same frequency as the transmitted data and has similar shape as the

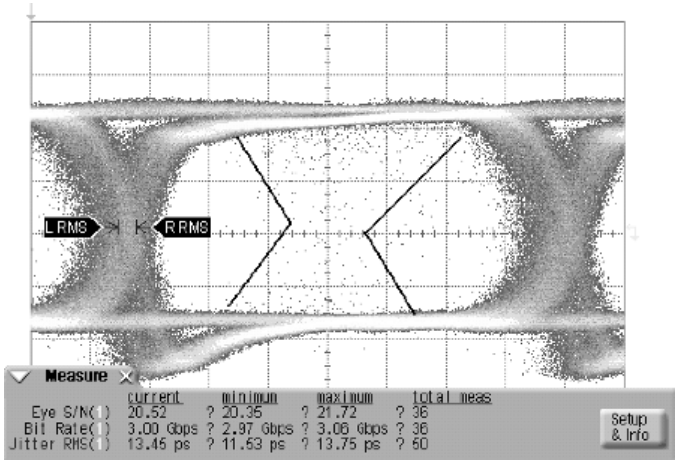


Fig. 19. Measured phase-delayed signal around the center of the eye diagram.

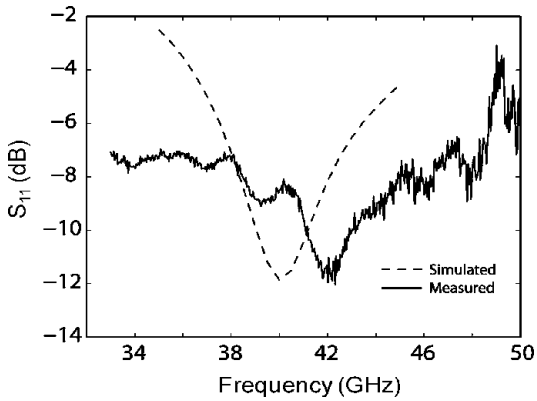


Fig. 20. Simulated and measured RL of the bond-wire antenna on the chip.

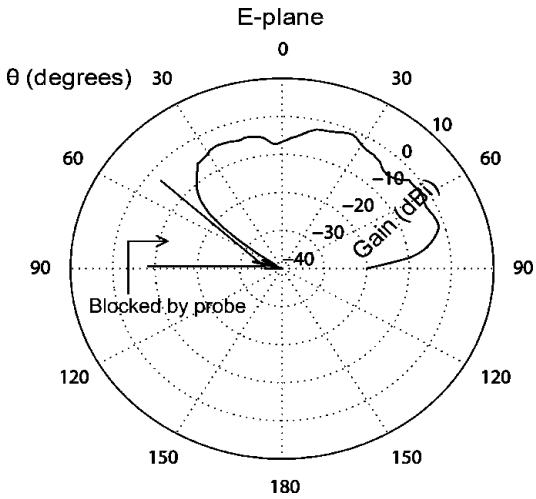


Fig. 21. Measured E-plane radiation pattern of the bond-wire antenna on the chip.

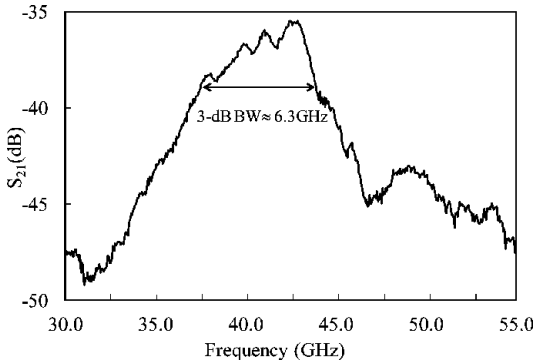


Fig. 22. Measured S_{21} of the bond-wire antenna pair when the distance is set to 0.5 cm.

crossing edge of the eye diagram. The cluster of noise around the eye center is observed in certain distances and data rate consistently, and associated with the BER drop supporting its correlation with the multi-path effect.

The semi-circle shape bond-wire antenna is formed between the pad on the chip and the pad on the PCB. Most areas underneath the antenna are filled by ground plane. The performances of the antenna in actual wireless data link setup are measured to compare with the stand alone antenna test results [23]. The return loss (RL) for the on-chip bond-wire antenna is shown in Fig. 20. The lowest S_{11} is -12 dB at 43 GHz. The measured E-plane radiation pattern for the antenna is shown in Fig. 21. The maximum gain of the antenna is -1.4 dBi, resulting in an extracted radiation efficiency of 50.9%. The reason for the drop in antenna gain at $\theta > 60^{\circ}$ is because the receiving horn antenna was behind the probe and probe holder in that angle. The measured antenna performances match well within a reasonable testing error with the stand alone antenna test results [23]. The H-plane radiation pattern measurement could not be performed because the probe feeding the antenna was no longer in the antenna far field, the probe could not be adequately covered by absorbing material to reduce reflections, and the input of the antenna was also connected to the output of the PA. The S_{21} of an antenna pair was measured when the distance was set to 0.5 cm, as shown in Fig. 22. The maximum gain was about -36 dB at 43 GHz and the 3-dB bandwidth is around 6.3 GHz.

With the measured transmitting power of -0.5 dBm and the S_{21} between antennas shown in Fig. 22, the power at the receiver input is about -45.5 dBm at 0.5 cm. Assuming the path loss increases with the square of the distance, the signal power would be -63.5 dBm at 4 cm, which is close to the minimum detectable power of the receiver, so the maximum communication distance is around 4 cm. This value matches well with the measurement results but is shorter than the anticipated distance. Comparing with the link budget analysis in Section II, the antenna gain is 3.6 dB lower and the path loss is 23.2 dB higher than the value estimated from the free space loss formula. This extra 26.8-dB power loss consumes the miscellaneous margin and reduces the communication distance. The decreased antenna gain can be explained by the non-ideal ground plane, while the reason for the extra channel loss is related to channel condition and requires further investigations

The power consumption of the transceiver is measured when the power supply was set to 1.6 V for the transmitter and 1.45 V for the receiver. The transmitter and receiver consume 57 mW and 60 mW respectively, including the input and output 50-Ω buffers that consume about 16 mW. The bit energy efficiency is 17 pJ/bit (17 mW/Gb/s), not including the power of the buffers. The bit energy efficiency is comparable with that of an optical data link, for instance, 10 mW/Gb/s in [37], yet the wireless

TABLE I
WIRELESS LINK PERFORMANCE COMPARISON

Parameters	This work	Ref. [33]	Ref. [34][1]	Ref. [35]	Ref. [36]
Technology	180-nm SiGe	180-nm CMOS	180-nm CMOS	90-nm CMOS	90-nm CMOS
Carrier [GHz]	43	3	8	60	60
Data rate [Gbps]	2 - 6	0.2	0.75	2.5	4
Antenna Type	Bond-wire	On-chip dipole	On-chip Monopole	On-board dipole	Horn antenna
Antenna Gain [dBi]	-1.4	N/A	-22	5	25
Distance [cm]	0.5 - 4	0.05	N/A	4	100
Measured BER	Up to 4×10^{-13}	N/A	N/A	1×10^{-12}	1×10^{-11}
Modulation	Binary ASK	OOK	BPM	OOK	QPSK
Area [mm^2]	0.62	2.34	0.29	1.11	6.875
Total Power [mW]	117	43	31	286	308
Energy/bit [pJ/bit]	17	215	41	114	77

1:Transmitter only.

TABLE II
PERFORMANCE SUMMARY

Receiver	
Total Gain[1]	50∼85-dB
Supply Voltage	1.5-V
3 dB Bandwidth[1]	9-GHz
Sensitivity[2]	-66-dBm
LNA Return Loss[1]	-7-dB
LNA NF[1]	7.68-dB
LNA Gain[1]	7.26-dB
Pre-Amplifier Gain[1]	22.7-dB
ED min input swing[1]	10-mV_{p-p}
ED Gain[1]	20-dB
ED PSRR[1]	-12-dB
VGA Gain[1]	0∼35-dB
Comparator Hysteresis[1]	60-mV
Transmitter	
Small-Signal Gain[1]	12-dB
Supply Voltage	1.5∼1.7-V
Output Power	-0.5-dBm
1 dB compression Point	-1.5-dBm
PAE[1]	5%
3 dB Bandwidth[1]	14-GHz

1:Simulation result.
2:Calculated result.

TABLE III
POWER BREAKDOWN

Receiver	60-mW
LNA	6.2-mW
Pre-Amplifiers	20-mW
Envelope Detector	9.3-mW
VGA	7.7-mW
Comparator	9.3-mW
Output Buffer	7.5-mW
Transmitter	57-mW
Modulator	5-mW
Power Amplifier	44-mW
Input Buffer	8.5-mW

*:The power consumption of individual blocks are calculated values.

link does not require any extra devices or post process steps. Table I compares the performances of the presented work with the state-of-the-art wireless high-speed data links. As shown in the table, the proposed transceiver has the lowest energy-per-bit value[33]–[36]. Comparing with [33], which uses on-chip antennas, the transmitting data rate is thirty times higher whereas the distance is about eighty times longer. Moreover, since the on-chip antenna occupies about 75% of the die size in [33], the total chip area of the presented design is about 27% of that in [33]. Also, the communication distance and BER is comparable with that in [35] while the design in [35] uses external antennas, and consumes about 43% more power than the proposed design.

Tables II and III summarize the performance of the proposed transceiver.

VI. CONCLUSION

This work presents a low-cost low-power 43-GHz wireless inter-chip data link, which is suitable for wireless or hybrid micro multi-chip network. The wireless inter-chip link uses a low-cost high efficiency bond-wire antenna and a low-power non-coherent binary ASK transceiver. The chip is implemented in a 180-nm SiGe BiCMOS technology and a standard chip-on-board packaging on FR4 subtrate is used for the chip and the bond-wire antenna. For the 43-GHz carrier, the radiation efficiency of the antenna is about 51% with a good horizontal radiation pattern, and the antenna gain and the return loss are -1.4 dBi and -12 dB, respectively. The implemented wireless data link was able to transmit up to 6-Gb/s data rate over a 4-cm channel, and the BER reaches about 10^{-11} over a distance of 2 cm. The bit energy efficiency is 17 pJ/bit, and the chip area is approximately 0.62 mm^2. The presented work shows the feasibility of high-speed wireless multi-chip communications.

ACKNOWLEDGMENT

The authors would like to thank the sponsors of the 2007–2008 SRC/SIA IC Design Challenge, especially Jazz Semiconductor for providing the design kit and chip fabrication. They also would like to thank G. Lockwood for her help on wirebonding.

REFERENCES

[1] D. A. B. Miller and H. M. Ozaktas, "Limit to the bit-rate capacity of electrical interconnects from the aspect ratio of the system architecture," *J. Parallel Distrib. Comput.*, vol. 41, no. 1, 1997.

[2] M. Forbes, J. Gourlay, and M. Desmulliez, "Optically interconnected electronic chips: A tutorial and review of the technology," *IEEE Electron. Commun. Eng. J.*, vol. 13, no. 5, pp. 221–232, Oct. 2001.

[3] H. Cho, P. Kapur, and K. C. Saraswat, "Power comparison between high-speed electrical and optical interconnects for interchip communication," *IEEE J. Lightw. Technol.*, vol. 22, no. 9, pp. 2021–2033, Sep. 2004.

[4] G. Chen *et al.*, "Electrical and optical on-chip interconnects in scaled microprocessors," in *Proc. IEEE Int. Symp. Circuits and Systems*, May 2005, pp. 2514–2517.

[5] D. V. Plant and A. G. Kirk, "Optical interconnects at the chip and board level: Challenges and solutions," *Proc. IEEE*, vol. 88, pp. 806–818, Jun. 2000.

[6] B. A. Floyd, C.-M. Hung, and K. K. O, "A 15-GHz wireless interconnect implemented in a 0.18-μm CMOS technology using integrated transmitters, receivers, and antennas," in *IEEE Symp. VLSI Circuits Dig.*, Jun. 2001, pp. 155–158.

[7] M.-C. F. Chang, V. P. Roychowdhury, L. Zhang, H. Shin, and Y. Qian, "RF/Wireless interconnect for inter- and intra-chip communications," *Proc. IEEE*, vol. 89, pp. 456–466, Apr. 2001.

[8] I. Post *et al.*, "A 65 nm CMOS SOC technology featuring strained silicon transistors for RF applications," in *Int. Electron Devices Meeting*, Dec. 2006, pp. 1–3.

[9] S. Gunnarsson *et al.*, "60 GHz single-chip front-end MMICs and systems for multi-Gb/s wireless communication," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 1143–1157, May 2007.

[10] T. Yao *et al.*, "Algorithmic design of CMOS LNAs and PAs for 60-GHz radio," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 1044–1057, May 2007.

[11] B. Razavi, "A 60-GHz CMOS receiver front-end," *IEEE J. Solid-State Circuits*, vol. 41, no. 1, pp. 17–22, Jan. 2006.

[12] A. Tomkins, R. A. Aroca1, T. Yamamoto, S. T. Nicolson, Y. Doi, and S. P. Voinigescu, "A zero-IF 60 GHz transceiver in 65 nm CMOS with $>$3.5 Gb/s links," in *Proc. IEEE Custom Intergrated Circuits Conf.*, 2008, pp. 471–454.

[13] C. Cao *et al.*, "A 24-GHz transmitter with on-chip dipole antenna in 0.13-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 43, no. 6, pp. 1394–1402, Jun. 2008.

[14] P. Popplewell, V. Karam, A. Shamim, J. Rogers, L. Roy, and C. Plett, "A 5.2-GHz BFSK transceiver using injection-locking and an on-chip antenna," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 981–990, Apr. 2008.

[15] K. K. O *et al.*, "On-chip antennas in silicon ICs and their application," *IEEE Trans. Electron Devices*, vol. 52, no. 7, pp. 1312–1323, Jul. 2005.

[16] P.-J. Guo and H.-R. Chuang, "A 60-GHz millimeter-wave CMOS RFIC-on-chip meander-line planar inverted-f antenna for WPAN applications," in *IEEE Antennas Propagat. Soc. Int. Symp.*, Jul. 2008, pp. 1–4.

[17] A. Babakhani, X. Guan, A. Komijani, A. Natarajan, and A. Hajimiri, "A 77-GHz phased-array transceiver with on-chip antennas in silicon: Receiver and antennas," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2795–2804, Dec. 2006.

[18] K. T. Chan *et al.*, "Integrated antennas on Si with over 100 GHz performance, fabricated using an optimized proton implantation process," *IEEE Microw. Wireless Compon. Lett.*, vol. 13, no. 11, pp. 487–489, Nov. 2003.

[19] Y. Koga *et al.*, "Cavity-backed MEMS patch antennas on double-layer silicon wafers," in *IEEE Antennas Propagat. Soc. Int. Symp.*, Jul. 2008, pp. 3935–3938.

[20] Y. Tsutsumi, M. Nishio, S. Sekine, H. Shoki, and T. Morooka, "A triangular loop antenna mounted adjacent to a lossy Si substrate for millimeter-wave wireless PAN," in *IEEE Antennas Propagat. Soc. Int. Symp.*, Jun. 2007, pp. 1008–1011.

[21] B. P. Gaucher, D. Liu, U. R. R. Pfeiffer, and T. M. Zwick, "Apparatus and methods for constructing antennas using wire bonds as radiating elements," U.S. 7,295,161, Nov. 13, 2007.

[22] D. C. Daly and A. P. Chandrakasan, "An energy-efficient OOK transceiver for wireless sensor networks," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 1003–1011, May 2007.

[23] R. Willmot, D. Kim, and D. Peroulis, "High efficiency wire bond antennas for on-chip radios," in *IEEE Antennas Propagat. Soc. Int. Symp.*, Dec. 2008.

[24] Ansoft HFSS FEM. [Online]. Available: http://www.ansoft.com/products/hf/hfss

[25] D. M. Campbell, "Accurate computer controlled on-wafer antenna measurement, data acquisition, and analysis," Master thesis, Sch. Electr. Eng. Technol., Purdue Univ., W. Lafayette, IN, 2008.

[26] B. Analui and A. Hajimiri, "Bandwidth enhancement for transimpedance amplifiers," *IEEE J. Solid-State Circuits*, vol. 39, no. 8, pp. 1263–1270, Aug. 2004.

[27] H.-S. Kim, X. Li, and M. Ismail, "A 2.4 GHz CMOS low noise amplifier using an inter-stage matching inductor," in *Proc. IEEE Midwest Symp. Circuits and Systems*, Aug. 1999, vol. 2, pp. 1040–1043.

[28] S. A. Sanielevici, K. R. Cioffi, B. Ahrari, P. S. Stephenson, D. L. Skoglund, and M. Zargari, "A 900-MHz transceiver chipset for two-way paging applications," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 2160–2168, Dec. 1998.

[29] C. T. Charles and D. J. Allstot, "A 2-GHz CMOS variable gain amplifier optimized for low noise," in *Proc. IEEE Int. Symp. Circuits and Systems*, 2006, pp. 2305–2308.

[30] B. A. Floyd, S. K. Reynolds, U. R. Pfeiffer, T. Zwick, T. Beukema, and B. Gaucher, "SiGe bipolar transceiver circuits operating at 60 GHz," *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 156–167, Jan. 2005.

[31] H. Veenstra, G. A. M. Hurkx, D. van Goor, H. Brekelmans, and J. R. Long, "Analyses and design of bias circuits tolerating output voltages above $\mathrm{BV_{CEO}}$," *IEEE J. Solid-State Circuits*, vol. 40, no. 10, pp. 2008–2018, Oct. 2005.

[32] T. Yao *et al.*, "Algorithmic design of CMOS LNAs and PAs for 60-GHz radio," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 1044–1057, May 2007.

[33] N. Sasaki, K. Kimoto, W. Moriyama, and T. Kikkawa, "A single-chip ultra-wideband receiver with silicon integrated antennas for inter-chip wireless interconnection," *IEEE J. Solid-State Circuits*, vol. 44, no. 2, pp. 382–393, Feb. 2009.

[34] V. Kulkarni, M. Muqsith, K. Niitsu, H. Ishikuro, and T. Kuroda, "A 750 Mb/s, 12 pJ/b, 6-to-10 GHz CMOS IR-UWB transmitter with embedded on-chip antenna," *IEEE J. Solid-State Circuits*, vol. 44, no. 2, pp. 394–403, Feb. 2009.

[35] J. Lee, Y. Huang, Y. Chen, H. Lu, and C. Chang, "A low-power fully integrated 60 GHz transceiver system with OOK modulation and on-board antenna assembly," *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, vol. 52, no. 2, pp. 316–317, Feb. 2009.

[36] C. Marcu *et al.*, "A 90 nm CMOS low-power 60 GHz transceiver with integrated baseband circuitry," *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, vol. 52, no. 2, pp. 314–315, Feb. 2009.

[37] C. Kromer *et al.*, "A 100-mW 4 $\times$ 10 Gb/s transceiver in 80-nm CMOS for high-density optical interconnects," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2667–2679, Dec. 2005.

Wu-Hsin Chen (S'05) received the B.S. and M.S. degrees from National Taiwan University, Taiwan, in 1996 and 1998.

From 2000 to 2007, he was with Sunplus Technology, Taiwan, where he was involved in the design of SRAM, ROM, RFID, and MCU. He joined Purdue University, West Lafayette, IN, in 2007, where he is currently pursuing the Ph.D degree. His research interests includes RF circuit design, phase-locked-loop and clock data recovery.

Mr. Chen won the first place in Phase One and Phase Two of the 2007–2008 SRC/SIA IC Design Challenge as a lead designer.

Sanghoon Joo (S'08) received the B.S. degree from Korea University, Korea, in 2003. He is currently pursuing the Ph.D. degree in the School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN.

His research interests include RF circuit design for wireless communication in CMOS and bipolar process.

Mr. Joo is the first place winner in Phase One and Phase Two of the 2007–2008 SRC/SIA IC Design Challenge.

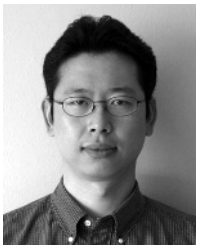
Serkan Sayılır (S'09) received the B.S. degree in electrical engineering from Boğaziçi University, Istanbul, Turkey, in 2007. He is currently pursuing the Ph.D. degree in the School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN.

His research interests focus on analog/RF circuit design for high-speed communication systems.

Mr. Sayılır was the first place winner in Phase One and Phase Two of the 2007–2008 SRC/SIA IC Design Challenge.

Russell Willmot (S'08) is currently pursuing the B.S. degree in electrical engineering at Purdue University, West Lafayette, IN, and expects to graduate in December of 2009.

His interests are in antenna design and RF MEMS. He is the author of one International Microwave Symposium conference paper.

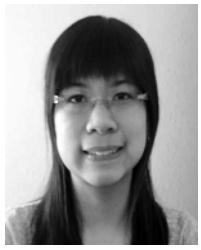


Tae-Young Choi (S'02–M'09) received the B.S. degree in electrical engineering from Seoul National University, Seoul, Korea, in 1999, and the M.S. and Ph.D. degrees in electrical engineering from the University of Michigan at Ann Arbor in 2002 and 2007, respectively. He is currently a post-doc at Purdue University, West Lafayette, IN.

His research interests are in RF integrated circuits for wireless applications.

Dowon Kim (M'08) received the M.S. and Ph.D. degrees from the Department of Electrical Engineering, Korea University, Korea, in 2004 and 2008, respectively.

Currently, she is working as a Postdoctoral Research Associate at the Birck Nanotechnology Center, Purdue University, West Lafayette, IN. Her current research interest is mm-wave SOC antennas and high-efficiency power amplifier design.



Julia Lu (S'08) received the B.S. degree in electrical engineering from National Cheng Kung University, Taiwan, in 2007. She is currently pursuing the Ph.D. degree in the School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN.

Her research interests focus on circuit design for sensor interface and multi-core communications.

Ms. Lu was the first place winner of the 2007–2008 SRC/SIA IC Design Challenge.

Dimitrios Peroulis (S'99–M'04) received the Diploma degree in electrical and computer engineering from the National Technical University of Athens, Athens, Greece, in 1998, and the M.S.E. and Ph.D. degrees in electrical engineering from the University of Michigan, Ann Arbor, in 1999 and 2003, respectively.

Since August 2003, he has been an Assistant Professor at the School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN. His research work is focused on microelectromechanical systems (MEMS) for multifunctional communications systems and sensors. His group is currently part of two research centers funded by DARPA (IMPACT center) and the National Nuclear Security Administration (PRISM center) that are focused on MEMS failure mechanisms and reliability.

Dr. Peroulis has received six teaching awards from Purdue University, including the Teaching for Tomorrow Award (2006) and Potter Award (2008). He has also been the recipient of three Student Paper Awards at IEEE MTT-S (2001 and 2002) and IEEE AP-S (2001).

Byunghoo Jung (S'00–M'05) received the B.S. degree from Yonsei University, Korea, in 1990, the M.S. degree from KAIST, Korea, in 1992, and the Ph.D. degree from the University of Minnesota, Minneapolis, in 2005.

From 1992 to 1999, he was with Samsung Electronics, Korea, where he was involved in the design of video signal driver circuits for flat-panel displays. Following receipt of his Ph.D. in January 2005, he was with Qualcomm, San Diego, CA, as a Senior RF IC Design Engineer until he joined the School of Electrical and Computer Engineering at Purdue University as an Assistant Professor in August 2005. His research interests include high-speed analog/RF circuit design for wireless and wired communications and bio-telemetry systems.

Dr. Jung is the first place winner of the 2002–2003 SRC SiGe BiCMOS Design Challenge (as a lead designer) and the 2007–2008 SRC/SIA IC Design Challenge (as a lead faculty), and holds 10 U.S. patents. He has been serving as a Co-Chair of the DAC/ISSCC Student Design Challenge (SDC) since October, 2006, as an Associate Editor of the IEEE Transactions on VLSI since January, 2009, and as a member of the Analog Signal Processing Technical Program Committee (ASPTPC) in the IEEE Circuits and System Society since May 2006.