

# A 6 GHz 60 mW BiCMOS Phase-Locked Loop

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**Abstract**— The design of a 6 GHz fully monolithic phase-locked loop fabricated in a 1  $\mu\text{m}$ , 20 GHz BiCMOS technology is described. The circuit incorporates a voltage-controlled oscillator that senses and combines the transitions in a ring oscillator to achieve a period equal to two ECL gate delays. A mixer topology is also used that exhibits full symmetry with respect to its inputs and operates with supply voltages as low as 1.5 V. Dissipating 60 mW from a 2 V supply, the circuit has a tracking range of 300 MHz, an rms jitter of 3.1 ps, and phase noise of -75 dBc/Hz at 1 kHz offset.

## I. INTRODUCTION

**H**IGH-SPEED, low-power phase-locked loops (PLL's) find wide application in optical data links, ATM systems, and frequency synthesizers. In the multigigahertz range, most of PLL's and clock recovery circuits have been implemented in III-V technologies [1], [2], with silicon designs appearing only recently [3]. From system integration standpoint, it is desirable to design such circuits in mainstream VLSI technologies so that subsequent data processing can be performed on the same chip without incurring great power or yield penalty.

This paper describes the design of a 6 GHz BiCMOS phase-locked loop [4], the fastest reported in silicon technology. Fabricated in a 1  $\mu\text{m}$ , 20 GHz process, the circuit requires no external components and dissipates 60 mW, a factor of 13 less than its counterpart in a AlGaAs/GaAs heterojunction bipolar technology [1]. Pushing the speed-power envelope of the process, the PLL employs a number of techniques to allow operation from supply voltages as low as 2 V.

The next section of the paper presents the PLL architecture and design issues. The building blocks are then described in sequence, starting with the voltage-controlled oscillator in Section III, the mixer in Section IV, and the pulse shaping circuit in Section V. Experimental results are summarized in Section VI.

## II. PLL ARCHITECTURE

Fig. 1 shows the architecture of the phase-locked loop. It consists of a pulse-shaping circuit at the front end and a loop comprising a phase detector (PD), a low-pass filter (LPF), an error amplifier  $A_L$ , and a voltage-controlled oscillator (VCO). The VCO provides the main output in the form of current, which flows through external 50  $\Omega$  termination resistors. The control voltage of the VCO is also monitored and amplified by  $A_M$  so as to obtain a demodulated output when the input is frequency modulated.

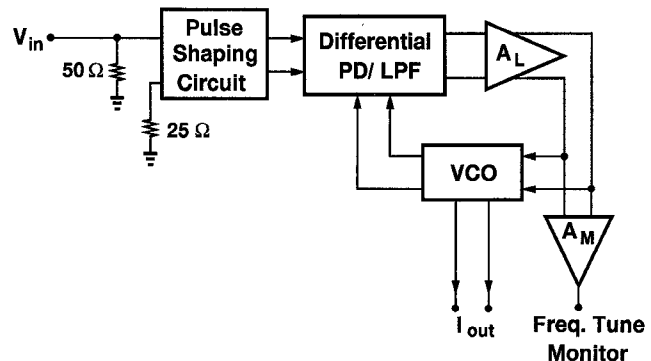


Fig. 1. PLL architecture.

The PLL utilizes differential signals in both the high-frequency path and the control of the VCO to suppress the effect of common-mode noise and also allow a robust design with low supply voltages.

The pulse shaping circuit serves two purposes. First, it converts the single-ended input to a differential signal having an amplitude equal to that of the VCO output. Second, it presents a driving impedance to the PD that is identical with the output impedance of the VCO. These precautions are necessary so as to lower the static phase error because, at 6 GHz, the mixer operates in small-signal regime and hence its phase error is sensitive to both the amplitude and the shape of its two inputs.

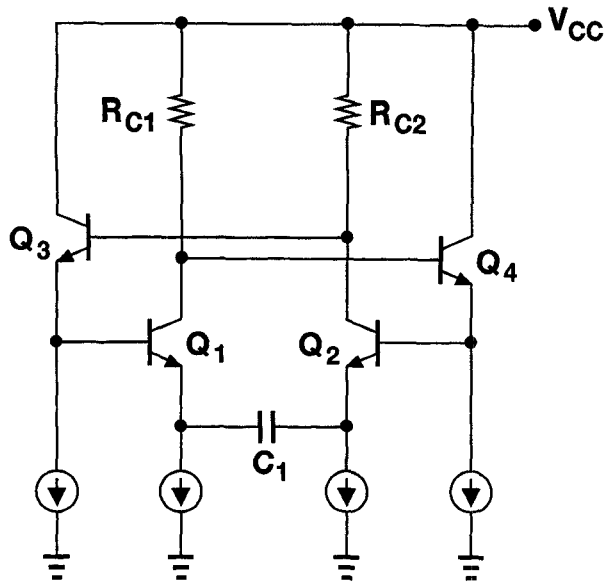
## III. VOLTAGE-CONTROLLED OSCILLATOR

Several critical parameters of the PLL, such as speed, timing jitter, spectral purity, and power dissipation, strongly depend on the performance of the VCO.

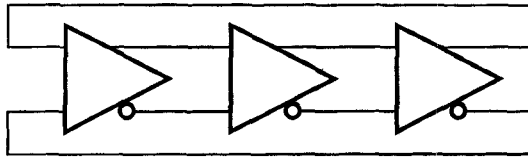
Fig. 2 illustrates two conventional approaches to building monolithic oscillators. In the emitter-coupled oscillator of Fig. 2(a), the maximum frequency depends on the minimum value of capacitor  $C_1$ . As the value of this capacitor decreases and the oscillation frequency increases, the loop gain drops, the oscillation amplitude diminishes, and the circuit eventually fails to oscillate. Simulations indicate that this configuration or its variants do not attain a frequency of 6 GHz in our 20 GHz BiCMOS process.

In the ring oscillator of Fig. 2(b), the period of oscillation is given by twice the number of gate delays. However, it is difficult to ensure reliable oscillations if the number of stages is less than three because the total phase shift around the loop will not be sufficient to allow complete switching in each stage. Even regardless of these issues, a two-stage ring oscillator does not yield a frequency of 6 GHz in the process used here.

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(a)



$$f = \frac{1}{6T_d}$$

(b)

Fig. 2. Conventional oscillator topologies. (a) Emitter-coupled oscillator; (b) ring oscillator.

The VCO topology employed in this work senses and combines the transitions in consecutive stages of a ring oscillator so as to achieve a period equal to two gate delays. Fig. 3 shows a conceptual diagram of this technique. The circuit comprises a three-stage ring oscillator and transconductance amplifiers  $G_{m1}$ - $G_{m3}$ , which sense the voltages at ports 1-3, respectively, and convert these voltages to current. The resulting currents are summed at node  $X$  and converted to voltage by  $R_L$ .

The circuit operates as follows: When the voltage at port 1 goes high (at  $t = 0$ ),  $G_{m1}$  turns on and draws current from  $R_L$ , making  $V_X$  go low. After one gate delay, at  $t = T_d$ , the voltage at port 2 goes low and  $G_{m2}$  turns off, allowing  $V_X$  to go high. Similarly, after another gate delay, at  $t = 2T_d$ , the voltage at port 3 goes high and  $G_{m3}$  turns on, pulling  $V_X$  low again. Thus, for every transition at each port of the ring oscillator, one transition is generated at node  $X$ , thereby yielding an output period of  $2T_d$  (as in a "one-stage ring oscillator"). Since the output frequency is independent of the number of inverters in the ring, three or more stages can be used to ensure sufficient phase shift around the loop.

To gain more insight into the circuit's operation, we note that if  $v_1, v_2$ , and  $v_3$  were pure sinusoids and the  $G_m$  stages perfectly linear, the output frequency would *not* be three

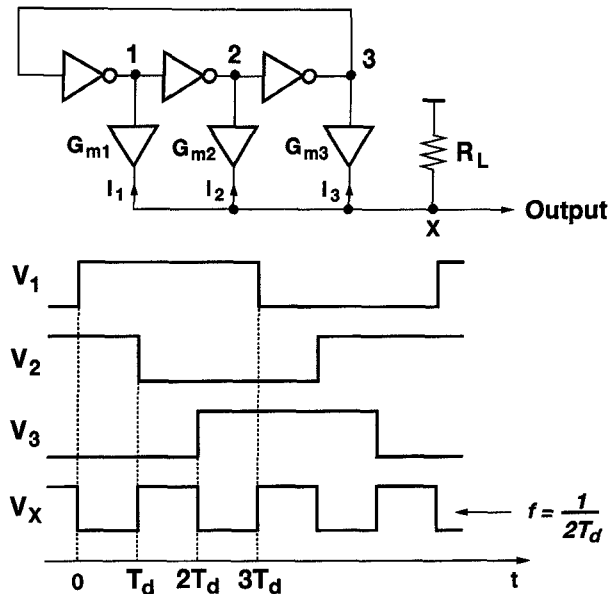


Fig. 3. Conceptual diagram of proposed VCO.

times that of the ring, because frequency multiplication is not possible in a linear system. In fact, assuming

$$v_1 = A \sin \omega t \quad (1)$$

$$v_2 = A \sin(\omega t + 2\pi/3) \quad (2)$$

$$v_3 = A \sin(\omega t + 4\pi/3) \quad (3)$$

and  $G_{m1} = G_{m2} = G_{m3} = G_m$ , we have

$$v_X =$$

$$G_m R_L A [\sin \omega t + \sin(\omega t + 2\pi/3) + \sin(\omega t + 4\pi/3)] \quad (4)$$

$$= 0. \quad (5)$$

Thus, this technique requires nonlinear operation in the ring amplifiers or the  $G_m$  stages. More specifically, if the ring amplifiers are nonlinear differential circuits, their outputs contain odd-order harmonics, e.g.,

$$v_1 = A \sin \omega t + B \sin(3\omega t + \theta) \quad (6)$$

$$v_2 = A \sin(\omega t + 2\pi/3) + B \sin(3\omega t + \theta + 2\pi) \quad (7)$$

$$v_3 = A \sin(\omega t + 4\pi/3) + B \sin(3\omega t + \theta + 4\pi), \quad (8)$$

thereby giving

$$v_X = 3G_m R_L B \sin(3\omega t + \theta). \quad (9)$$

Similarly, if  $v_1, v_2$ , and  $v_3$  are pure sinusoids but the  $G_m$  stages introduce nonlinearity, the fundamental is still suppressed while the third harmonic is enhanced. In essence, the  $G_m$  stages "sift" the third harmonic.

The VCO topology of Fig. 2 entails three design issues. First, the capacitive loading of the  $G_m$  stages tends to slow down the ring oscillator, making this technique more efficient in bipolar technology, where loading has less effect on the delay, than in CMOS. Second, the number of stages in the ring must be odd so that multiple levels do not occur in  $V_X$ . Third, any mismatch in the delay of these stages translates into

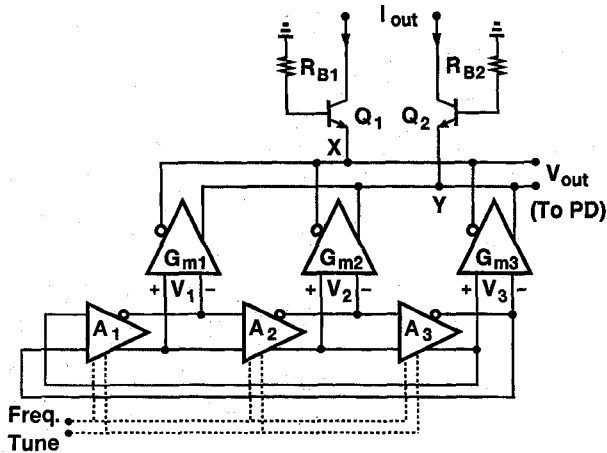


Fig. 4. VCO block diagram.

jitter at the output. Thus, it is important to equalize the wiring capacitance seen at the output of each stage.

The actual implementation of the VCO is depicted in Fig. 5. Three differential voltage amplifiers  $A_1$ - $A_3$  constitute the main ring and their outputs are sensed by three differential transconductance amplifiers  $G_{m1}$ - $G_{m3}$ . The frequency is tuned by varying the delay of each stage in the ring.

In combining the output currents of the  $G_m$  stages, the resistive load of Fig. 3 is replaced with common-base devices  $Q_1$  and  $Q_2$ . This is because the capacitance at nodes  $X$  and  $Y$  is quite significant: it includes the capacitance seen at the output of each  $G_m$  stage and the input capacitance of the phase detector. With simple resistors connected to the summing nodes, the resulting time constant substantially attenuates the amplitude of the 6 GHz signal. The common-base devices, on the other hand, introduce an *inductive* component at nodes  $X$  and  $Y$  that is approximately equal to  $(R_B + r_b)\tau_F$ , where  $R_B = R_{B1} = R_{B2}$ ,  $r_b$  is the base resistance, and  $\tau_F$  is the base transit time. The resulting inductive peaking enhances the amplitude by approximately a factor of three. The value of  $R_{B1}$  and  $R_{B2}$  can vary by a factor of two with little effect on the output amplitude.

Fig. 5 depicts the circuit details of one stage of the VCO. Each of the amplifiers  $A_1$ - $A_3$  is implemented as a differential pair  $Q_1$ - $Q_2$  and two emitter followers  $Q_3$ - $Q_4$ . Each  $G_m$  block simply consists of a current-steering pair  $Q_5$ - $Q_6$ . Differential pairs  $Q_7$ - $Q_8$  and  $Q_9$ - $Q_{10}$  adjust the bias current of the emitter followers to fine-tune the frequency of oscillation. Current sources  $I_1$  and  $I_2$  are used to avoid starving  $Q_3$  and  $Q_4$  during loop transients as well as provide a means for coarse frequency adjustment.

An important concern in the VCO design has been its low-voltage operation. Fig. 6 shows a section of the VCO along with voltage drops whose sum determines the minimum supply voltage. NMOS current sources prove useful here because, unlike their bipolar counterparts, they have negligible impact on speed even with voltage headrooms of a few hundred millivolts. Note that when the differential pair in Figure 6 switches, the common emitter node momentarily drops by about 150 mV, leaving only 250 mV across the current source and therefore precluding the use of bipolar devices here. In

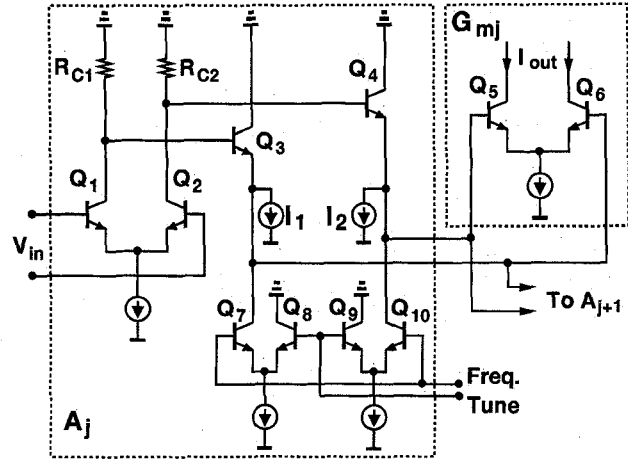


Fig. 5. Implementation of voltage and transconductance amplifiers.

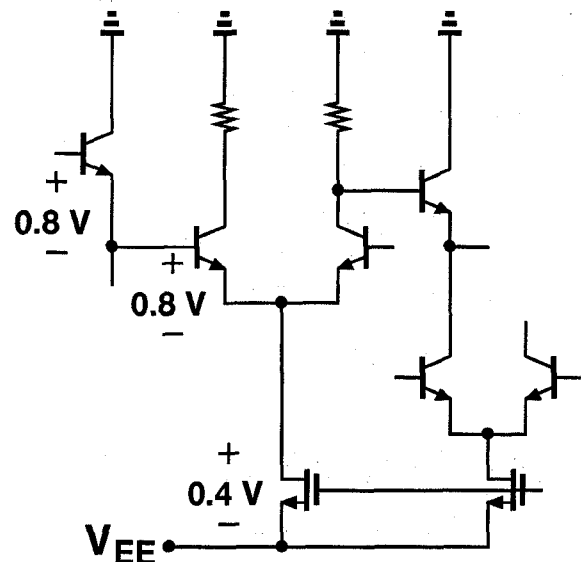


Fig. 6. Section of VCO circuit.

this design, the NMOS transistors are slightly in the triode region, but their current can still be controlled to compensate for temperature and supply variations.

#### IV. PHASE DETECTOR

Another critical building block of the PLL is the phase detector for it must mix two 6 GHz signals with reasonable gain and power dissipation. While the Gilbert cell is often utilized for mixing, it suffers from two drawbacks in this application. First, it employs stacked differential pairs, thus requiring a large voltage headroom. Second, it introduces substantial phase error at high frequencies because its input signals propagate through inherently different paths.

Fig. 7 shows a half-circuit equivalent of the phase detector/low-pass filter. The PD incorporates an exclusive OR gate comprising  $Q_1$ - $Q_6$  [5]. Since  $Q_3$  is on only if both  $A$  and  $B$  are low,  $I_{C3} \equiv \bar{A} \cdot \bar{B}$ , where  $I_{C3}$  denotes the logical value of the  $Q_3$  collector current. Similarly,  $I_{C4} \equiv A \cdot B$ . Therefore, the logical output is equal to  $A \oplus B$ .

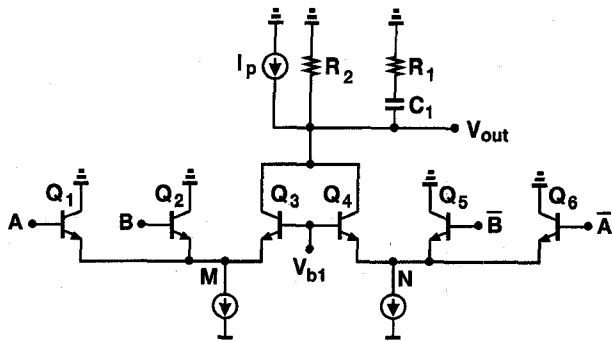


Fig. 7. Phase detector and low-pass filter.

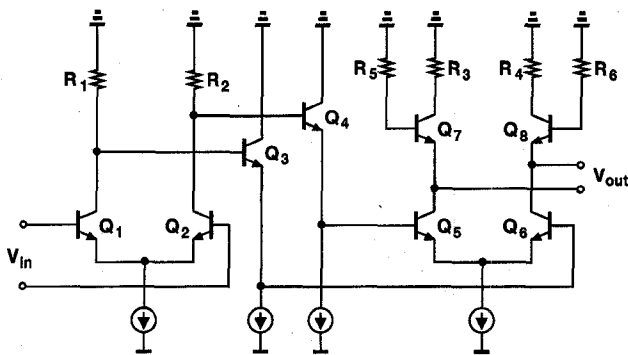


Fig. 8. Pulse shaping circuit.

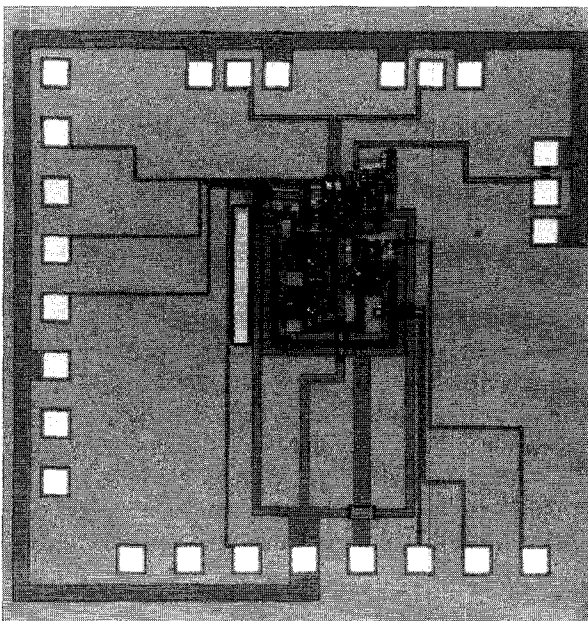


Fig. 9. PLL die photo.

In contrast with the conventional ECL XOR, the topology of Fig. 7 has two advantages: 1) it avoids stacked transistors and hence operates from a lower supply voltage, and 2) it is inherently symmetric with respect to inputs  $A$  and  $B$ , thereby providing equal phase shift for these signals and thus zero static phase error. Nevertheless, the value of  $V_{b1}$  should be accurately defined and controlled so that it tracks the common-

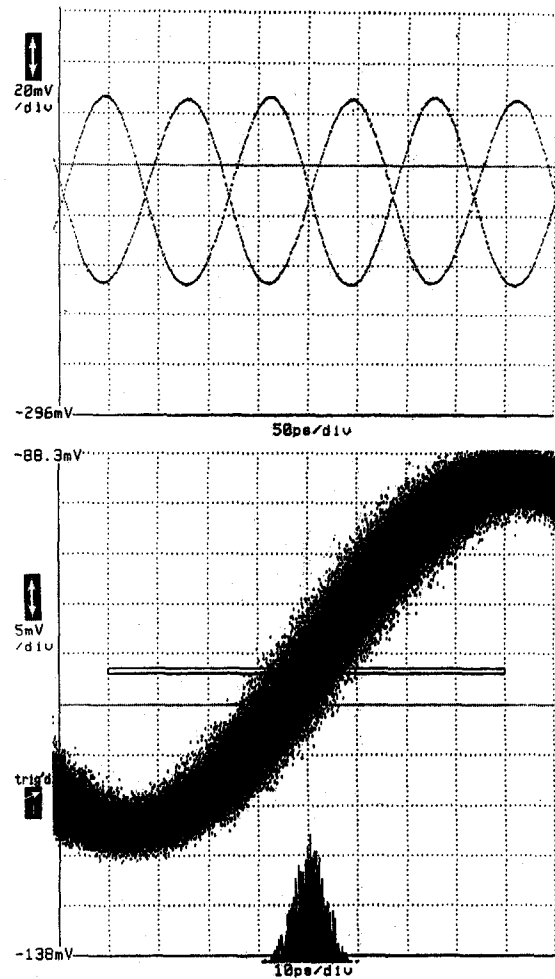


Fig. 10. Measured PLL output in time domain.

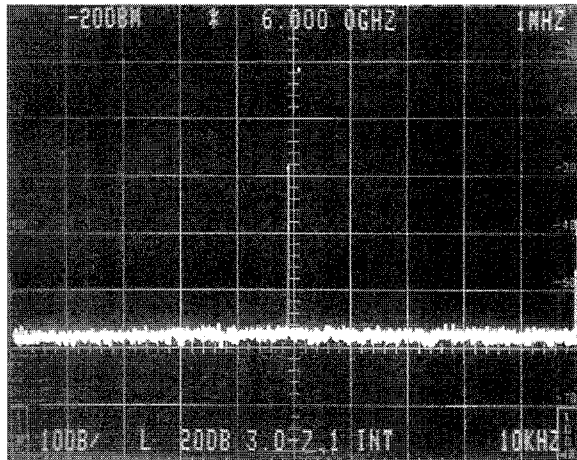
mode level of the inputs. Thus,  $V_{b1}$  is generated using a replica of the VCO output stage (i.e., common-base devices in Fig. 4).

The output current of the PD is directly low-pass filtered using the lead-network  $R_1$ ,  $R_2$ , and  $C_1$ . Current source  $I_p$  is approximately equal to  $0.75(IC_3 + IC_4)$ , where  $IC_3$  and  $IC_4$  denote the collector bias currents of  $Q_3$  and  $Q_4$ , respectively. This allows a larger  $R_2$  and hence a higher gain for a given  $IC_3 + IC_4$ . Note that  $M$  and  $N$  are the only high-speed nodes in this circuit.

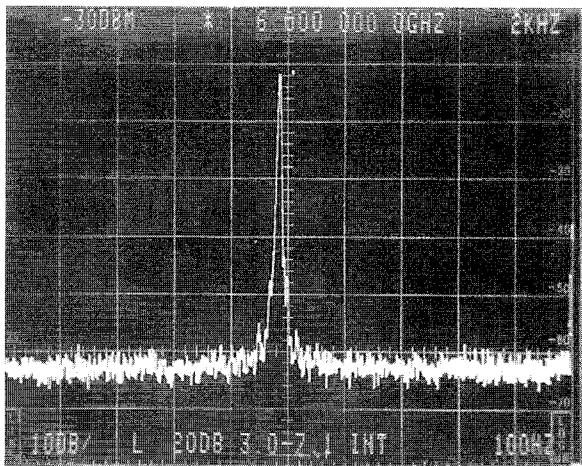
The actual PD/LPF circuit utilizes two of the half circuits shown in Fig. 7, with  $A$  and  $\bar{A}$  interchanged in one of the half circuits to generate fully differential outputs [5].

## V. PULSE SHAPING CIRCUIT

The pulse-shaping circuit is shown in Fig. 8. This circuit provides a signal path identical to one stage of the VCO (namely,  $A_j$  and  $G_{mj}$  in Fig. 5) as well as a differential load identical to the impedances seen at nodes  $X$  and  $Y$  in Fig. 4. More specifically, in the pulse shaping circuit,  $Q_1$ - $Q_6$  replicate the role of  $Q_1$ - $Q_6$  in Fig. 5, whereas  $Q_7$ - $Q_8$  and  $R_3$ - $R_6$  emulate the load devices  $Q_1$ - $Q_2$  and  $R_{B1}$ - $R_{B2}$  in Fig. 4. The devices and currents are scaled such that the output impedance is the same as that of the VCO.



Horiz. 1 MHz/div  
Vert. 10 dB/div



Horiz. 2 kHz/div  
Vert. 10 dB/div

Fig. 11. PLL output spectrum.

## VI. EXPERIMENTAL RESULTS

The phase-locked loop has been fabricated in a  $1\ \mu\text{m}$ , 20 GHz BiCMOS technology [6]. Shown in Fig. 9 is a photograph of the chip, whose active area measures approximately  $500\ \mu\text{m} \times 500\ \mu\text{m}$ . The circuit has been tested on wafer while running from a 2 V supply. High-speed Picoprobes from GGB Industries are used to apply the input and measure the output, while multicontact Cascade probes from Cascade Microtech provide power, bias, and ground connections. A ground ring on the chip establishes a low-inductance connection among the grounds of all the probes.

Fig. 10 shows the measured differential output and jitter histogram of the PLL. The circuit has a jitter of 3.1 ps rms and 30 ps peak-to-peak. The tracking range is 300 MHz and the center frequency can be varied by 700 MHz.

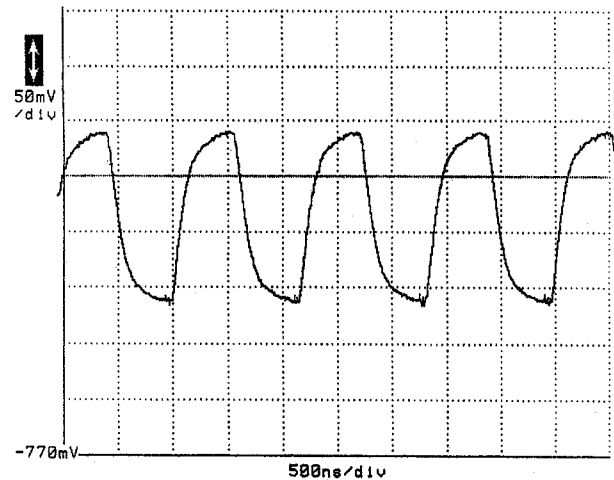


Fig. 12. Demodulated output for  $\Delta f = \pm 10\ \text{MHz}$  at input.

TABLE I  
PLL CHARACTERISTICS

Center Frequency	6 GHz
Tracking Range	300 MHz
Jitter	3.1 psec rms
Phase Noise	-75 dBc/Hz @ 1 kHz Offset
Power Dissipation	60 mW
Supply Voltage	2 V
Technology	20 GHz, 1- $\mu\text{m}$ BiCMOS

The measured output in the frequency domain is depicted in Fig. 11 with two different horizontal scales. The spectrum exhibits no coherent sidebands, and the center spectral line drops by 55 dB at 1 kHz offset when the resolution bandwidth is set to 100 Hz. This gives a phase noise of  $-75\ \text{dBc/Hz}$  at 1 kHz offset.

The response of the PLL to a frequency-modulated input has also been examined. Fig. 12 depicts the measured frequency tune monitor voltage (output of  $A_M$  in Fig. 1) for a  $\pm 10\ \text{MHz}$  modulation centered at 6 GHz. The bandwidth of this measurement is limited by the input signal generator, an HP 8341B, whose FM input amplifier has a 3 dB bandwidth of 10 MHz. The simulated closed-loop bandwidth is approximately 200 MHz. Table I summarizes the characteristics of the PLL.

## VII. CONCLUSION

High-speed, low-power circuit techniques make it possible to design high-performance phase-locked loops and clock recovery circuits in VLSI technologies. A PLL fabricated in a  $1\ \mu\text{m}$ , 20 GHz BiCMOS process has been presented that incorporates new VCO and mixer topologies. The circuit is suited to demodulation and frequency synthesis applications and can also be used in clock recovery with the addition of a frequency detector.

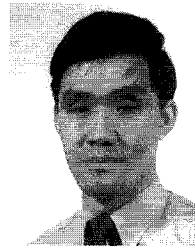
A VCO configuration has been introduced that achieves an oscillation period of two ECL gate delays by sensing and combining the transitions in a ring oscillator. Since the period is independent of the number of stages, the oscillator can be optimized for complete switching. A low-voltage exclusive OR gate has also been employed that, by virtue of its full symmetry, is free from systematic phase error. Using such techniques, the PLL operates at 6 GHz while dissipating 60 mW from a 2 V supply. It exhibits an rms jitter of 3.1 ps and phase noise of  $-75$  dBc/Hz at 1 kHz offset.

#### ACKNOWLEDGMENT

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Dr. Sung has written and co-written more than 35 papers in refereed scientific journals on the subjects of device physics, device structure, and technology. He received the 1994 ISSCC Best Editorial Paper award, and holds six U.S. patents in VLSI/ULSI technology areas.



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