A 60-dB Dynamic-Range CMOS Sixth-Order 2.4-Hz Low-Pass Filter for Medical Applications

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***Abstract*—The design and implementation of a fully integrated complementary metal–oxide–semiconductor (CMOS) sixth-order 2.4 Hz low-pass filter (LPF) for medical applications is presented. For the implementation of large-time constants both linearized operational transconductance amplifiers with reduced transconductance and impedance scalers schemes for grounded capacitors are employed. Experimental results for the filter have shown a dynamic range (DR) of 60 dB, while the harmonic distortion components are below −50 dB. The power consumption for the filter is below 10 μW, the power supply is $\pm$1.5 V, and the active area is 1 mm^2. The filter was fabricated in a double poly double metal 0.8 μm CMOS process.**

***Index Terms*—Impedance scaling, low-frequency filters, transconductance reduction techniques.**

I. Introduction

LOW-FREQUENCY filters are important building blocks for biomedical systems, wherein analog preprocessing blocks, such as low noise preamplifiers and filters for the acquisition of bioelectric signals are employed. These circuits should not introduce any form of distortion that can destroy the information contained. For this reason, the analog preprocessing blocks must present high performance over the frequency of interest.

The filters employed in such systems are used for sensing biolectrical signals which, typically, are in the range of 1 μV–100 mV while the frequencies are below 100 Hz [1], [2]. At the input, a low-pass filter (LPF) is usually employed in order to limit the frequency band.

The design of very low-frequency filters (<10 Hz) is not straightforward, especially for integrated circuit implementations where chip realization of large time constants are needed. As an example, let us consider the implementation of a 5-Hz pole. In this case, transconductances of 1 nA/V and capacitors larger than 200 pF are both required. Unfortunately, very small transconductances lead to higher noise level and practical capacitances are limited to below 50 pF due to silicon area limitations. Furthermore, the implementation of transconductances below 1 nA/V is not trivial, especially if other design specifications such as low noise level, low distortion, high dynamic range and limited silicon area must be satisfied. Several design techniques have already been proposed to overcome these design constraints [3]–[7]. The use of switched capacitor (SC) techniques [3] is not suitable for most medical applications and other approaches using complementary metal–oxide–semiconductor (CMOS) technologies are not well situated for these applications [4], [6], [7]. Besides, techniques using bipolar transistors are more expensive [5]. It has been demonstrated in [8] and [9] that CMOS transistors biased in the linear region and both current cancellation and current division techniques can efficiently be used to implement high-performance voltage to current converters. It is also well known that the integrated thermal noise level is inversely proportional to the integrating capacitor, hence it is desirable to increase the capacitors as much as possible. To this end, impedance scalers have been proposed in the literature [10] and [11].

In this paper, a 2.4-Hz low-pass filter achieving a 60-dB dynamic range is presented. Capacitors ranging from 18 to 200 pF are implemented by using 5-pF capacitors and impedance scalers. This approach allows a considerable saving of silicon area. As a result of the large capacitors emulated in the implementation a huge reduction in the filter noise is obtained. In Section II, both design specs and filter architecture are discussed. In addition, a differential pair based integrator is presented. Design guide lines for high-performance implementations (low-noise, low-distortion, and high dynamic range) of this circuit are also given. Design considerations for the implementation of a low-distortion, low-noise operational transconductance amplifier (OTA) with reduced transconductance suitable for low frequency applications are presented in Section III. In Section IV, impedance scaling schemes for the realization of large capacitor values are discussed. Trade-offs for an optimal implementation of this circuit are given in this section as well. In Section V some experimental results are presented. Finally, in Section VI the conclusions are given.

II. Characteristics and Filter Architecture

A typical data acquisition system for biomedical signals is shown in Fig. 1. The preamplifier must amplify the input signal to a higher level with low distortion and low noise. Typical amplifier gains are in the range of 10–1000 and the noise density should be below 10 nV/$\sqrt{\text{Hz}}$ (noise current should be below

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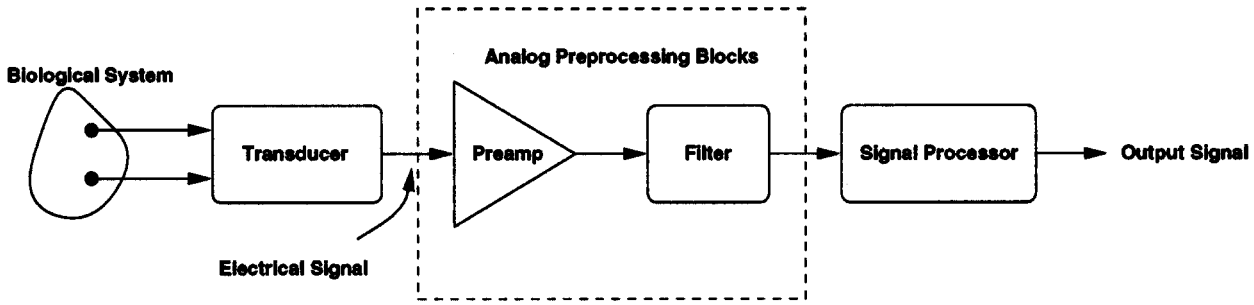

Fig. 1. Block diagram of a general purpose bioelectric signal acquisition system.

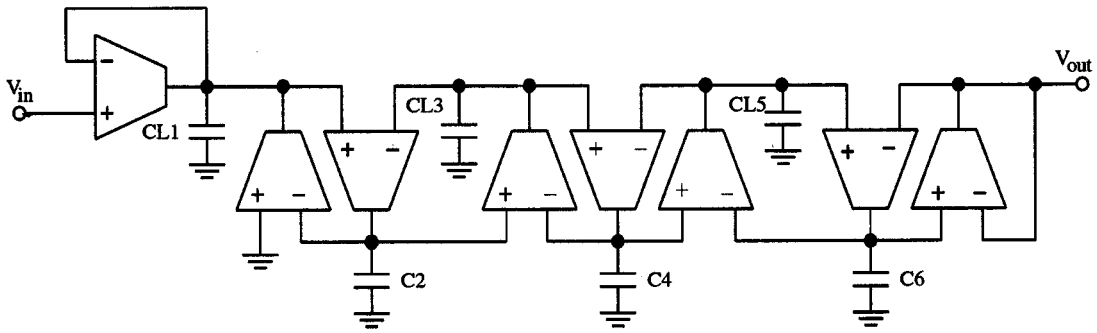

Fig. 2. OTA-C implementation of the single-ended low-pass filter.

1 pA/$\sqrt{\text{Hz}}$) [1]. For electrocardiograph (ECG) applications where the magnitude of the signal is around 1 mV–25 mV, and considering a preamplifier gain of ten, the magnitude of the signal to be processed by the low-pass filter (LPF) is around 10–250 mV [1]. To sense the T wave signal, a cutoff frequency as low as 2.4 Hz is required. Moreover, system requirements lead to the following filter constraints:

1) sixth-order Bessel filter;
2) total harmonic distortion (THD) <-50 dB;
3) dynamic range (DR) >60 dB;
4) integrated noise level <100 μV;
5) minimum power consumption (<50 μW).

For the implementation of high-performance low-frequency filters, SC design techniques have commonly been preferred over continuous-time design techniques (OTA-C, Mosfield-effect transister (MOSFET-C), and active RC filters). This is mainly due to their high accuracy (0.5%), low sensitivity to parasitic capacitors, and reduced harmonic distortion components (e.g., THD <-70 dB) [12]. However, SC implementations require a precise on-board clock and phase generators. Moreover, for very large time constants, large capacitor ratios are mandatory. The above limits are such that the design constraints cannot be satisfied. This paper presents an alternative solution to the SC implementation. It describes the design of a sixth-order 2.4-Hz low-pass filter implemented by using OTA-C techniques. This technique avoids the pre- and post-filtering required by SC filters. Moreover, it is a continuous-time technique which avoids noise switching problems. To minimize passband sensitivity to transistors mismatches, the filter is based on a double-terminated RLC ladder prototype. The implemented single-ended filter is shown in Fig. 2. Eight linearized 2-nA/V transconductance OTAs are employed. The effective capacitors are in the range of 18–200 pF.

To satisfy the above-mentioned design specs, several design considerations have to be taken into account. In this section, we will give guidelines for the optimal design of the LPF. For easier analysis and better understanding, the OTA based integrator is first considered. Among other parameters, the most important parameters for the OTA based integrator are THD and DR. THD is related to the linearity of the input stage of the voltage to current transducer. DR is dependent on the linear range of the OTA and the input referred noise.

For an integrator based on a differential pair input stage, see Fig. 3, the third harmonic distortion (HD3) can be computed as

$$\text{HD3} = \frac{1}{32}\left(\frac{V_D}{V_{D\text{SAT}}}\right)^2 \tag{1}$$

where V_D is the magnitude of the differential input signal and $V_{D\text{SAT}}$ is the saturation voltage of the input transistors. If the thermal noise is accounted, the input referred thermal noise power density is given by

$$\begin{aligned} v_{\text{in,th}}^2 &= \left[2\left(1+\frac{g_{mMP}}{g_{mMN}}\right)\right]\frac{8kT}{3g_{mMN}} \\ &= 2\text{NF}\,\frac{8kT}{3g_{mMN}} \end{aligned} \tag{2}$$

where g_{mMP} and g_{mMN} are the small signal transconductances of transistors MP and MN, respectively. NF $(=1+(g_{mMP}/g_{mMN}))$ is the noise factor. Factor $8kT/3g_{mMN}$ is the equivalent noise density of a single transistor with a small signal transconductance equal to g_{mMN}. Parameters $k[J/^\circ K]$ and $T[^\circ K]$ are the Boltzmann constant and the temperature, respectively. In theory, $8kT/3g_m$ is the minimum achievable noise density for a voltage to current converter implemented

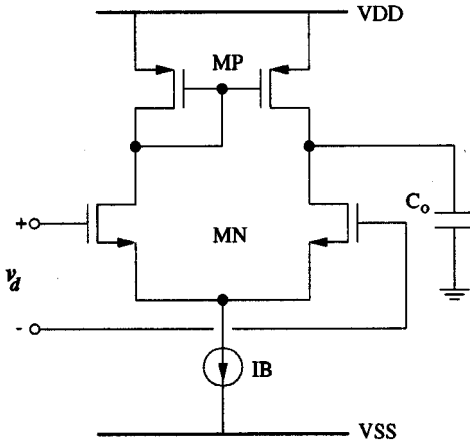

Fig. 3. Integrator based on a differential pair input stage.

with transistors biased in the saturation region and a small signal transconductance equal to g_{mMN}.

If the input referred thermal noise density is integrated over the frequency range of interest or filter bandwidth BW then the noise level can be computed as

$$v_{\text{int,th}}^2 = \int_{\text{BW}} v_{\text{in,th}}^2\, df = 2\text{NFBW}\,\frac{8kT}{3g_m}. \tag{3}$$

If the flicker noise components are considered, the input referred flicker noise density is given by

$$v_{\text{in},f}^2 = \frac{I_B}{L^2 C_{\text{ox}} f g_m^2}\,(K_{Fn}k_n' + K_{Fp}k_p'). \tag{4}$$

Integrating the noise density over the bandwidth leads to

$$\begin{aligned} v_{\text{int},f}^2 &= \int_{\text{BW}} v_{\text{in},f}^2\, df \\ &= \left[\frac{I_B}{L^2 C_{\text{ox}} g_{mMN}^2}\,(K_{Fn}k_n' + K_{Fp}k_p')\right] \ln\frac{1}{\text{BW}}. \end{aligned} \tag{5}$$

In (4) and (5), K_{Fn} and K_{Fp} are the flicker noise constants for the (n-channel) NOS and POS (p-channel) transistors, respectively, while $k_n'\,(=\mu_n C_{\text{ox}})$ and $k_p'(=\mu_p C_{\text{ox}})$ are the transconductance parameters for NMOS and PMOS transistors, respectively. I_B is the bias current, L the channel length, and C_{ox} the oxide capacitance.

Accounting for thermal and flicker noise components, the total input referred noise can be computed as

$$\begin{aligned} v_{\text{int},t}^2 =& 2\text{NF}\,\frac{8kT}{3g_{mMN}}\,\text{BW} \\ &+ 2\left[\frac{I_B}{L^2 C_{\text{ox}} g_{mMN}^2}\,(K_{Fn}k_n' + K_{Fp}k_p')\right] \ln\frac{1}{\text{BW}}. \end{aligned} \tag{6}$$

Typically, for low-frequency applications, the flicker noise is the dominant one. According to (6), it can be seen that a significant reduction in the total noise level of the integrator can be obtained if low values for the bias current are used. Further reductions in the noise level can be achieved if both large transistors and large transconductance gains are employed.

The lossless integrator's dynamic range, defined as the signal to noise ratio, can be approximately computed as

$$\text{DR} \approx \frac{0.3V_{D\text{SAT}}}{v_{\text{int},t}} \tag{7}$$

where $0.3V_{D\text{SAT}}$ is the linear range of the OTA [13]. Equations (6) and (7) are the most important tools for the design of high-performance OTA based integrators. To increase the dynamic range, both $V_{D\text{SAT}}$ for the differential pair and the transconductance gain must be increased. Therefore, large capacitors should be used.

III. Linearized OTA for Low-Frequency Applications

In OTA-based filters, voltage-to-current converters can generate huge harmonic distortion components, hence it is mandatory to employ linearized OTAs. It has already been demonstrated that transistors with large saturation voltages can efficiently be used for the design of very low distortion voltage-to-current converters. If further transconductance reductions are required, both current division and current cancellation techniques can also be employed. The OTA used in this paper, shown in Fig. 4, combines these techniques. In this OTA, the transistor biased in triode region is split into two transistors (MR) and their source–gate voltage is controlled by $MC1$. As a result, the small signal transconductance is little sensitive to the common-mode input voltage. $VB2$ and $VB3$ are used to tune the OTA.

In accordance with Fig. 4, if the small signal transconductances of transistors MM, $M1$, and MN are such that these transistors operate as source followers, then the differential input voltage $(v_1 - v_2)$ is converted to current by transistors MR which are operated in triode region. The drain current of MR is split by transistors MM, $M1$, and MN. Most of the current flows to ground through transistors MM because we designed the dimensions so that $g_{mMM} \gg g_{mM1}, g_{mMN}$. Note that the drain currents of $M1$ and MN are partially cancelled at the output of the OTA, leading to huge transconductance reductions. It can be shown that the resulting small signal transconductance becomes

$$G_m = \frac{i_o}{v_1 - v_2} = \frac{N-1}{M+N+1}\,g_{oMR} \tag{8}$$

where g_{oMR} is the small signal drain–source conductance of transistor MR, given by

$$g_{oMR} = \mu_p C_{\text{ox}}\,\frac{W_{MR}}{L_{MR}}\,(V_{SGMR} - V_T). \tag{9}$$

In the above equations, M is defined as the ratio of transconductances between MM and $M1$, while N is the ratio of transconductances between MN and $M1$. Parameters μ_p and V_T are the mobility of the carriers in the channel and the threshold voltage of the MR transistor, respectively. V_{SGMR} is the source–gate voltage of MR, and W_{MR} and L_{MR} are the gatewidth and the gate length of MR, respectively.

From (8) and (9), huge reductions of the ac small signal transconductance, desirable for low frequency applications, can be obtained by adjusting the M and N ra-

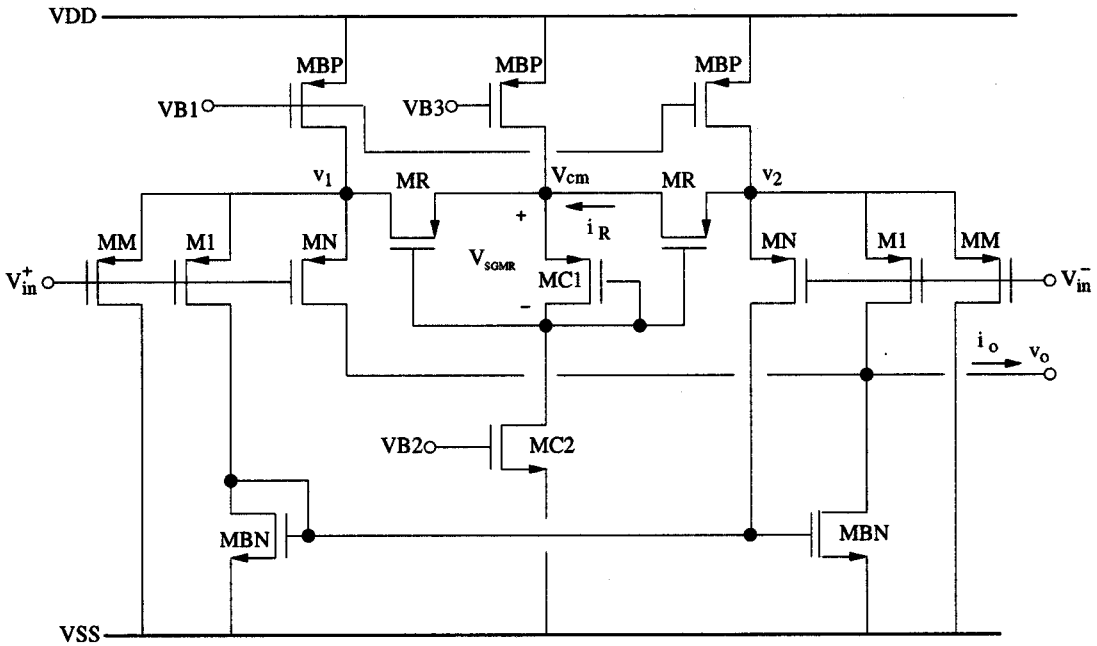

Fig. 4. Single-ended OTA for low frequency applications.

tios and reducing g_{oMR}. Reducing g_{oMR} implies small $V_{DSATMR} (= V_{GSMR} - V_T)$ and large L_{MR} values.

A. Design Considerations for the Linearized OTA

1) Distortion: To reduce harmonic distortion components, it is convenient that MR transistors realize the voltage to current conversion. For proper conversion it is desirable to keep $g_{mMM} \geq 5g_{oMR}$. It is well known that the harmonic distortion components for a MOS transistor biased in linear region are inversely proportional to V_{DSAT} [14]–[16]. Therefore, for low distortion applications, V_{DSAT} cannot be further reduced as was remarked in the last section. A rule of thumb for low distortion applications is to keep $V_{DSAT} > 2V_{DMAX}$, where V_{DMAX} is the maximum differential input voltage. It can be demonstrated that, under these conditions, HD3 is around -60 dB [15]. In this specific application, the maximum differential input voltage is around 250 mV, hence V_{DSAT} for MR transistors should be fixed around 500 mV.

2) Noise: The noise contributions of transistors MBP, MM, and MR are very small due to the current division effect, most of the noise current flows to ground through transistors MM. It can be noted that the most important noise contributions are due to transistors $M1$, MN, and MBN because their noise current is not reduced by the current divider. If $M \gg 1$ and $g_{mMM} \gg g_{oMR}$, then the output referred noise density current is approximately given by

$$i^2_{o,\mathrm{th}} = 2(i^2_{oM1} + i^2_{oMN} + i^2_{oMBN}). \tag{10}$$

From the above expression, the integrated input referred thermal noise power can be computed as

$$v^2_{\mathrm{int,th}} = \int_{\mathrm{BW}} v^2_{\mathrm{in,th}}\, df \cong \frac{16kT}{3G_m}\,[\mathrm{NF}]\,\mathrm{BW} \tag{11}$$

where NF is defined as the noise factor and is given by $(g_{mM1} + g_{mMN} + g_{mMBN})/G_m$ and G_m is given by (8). In (11), $16kT/3G_m$ represents a fundamental limit for the thermal noise level.

If flicker noise components for the MOS transistor biased in strong inversion are considered, the output referred noise current and the input referred noise voltage can approximately be computed by the following equations

$$i^2_{o,f} \cong \frac{2\,\dfrac{I_B}{M}}{C^2_{\mathrm{ox}}L^2 f}\,(k'_n K_{Fn} + 2k'_p K_{Fp}) \tag{12}$$

$$v^2_{\mathrm{int},f} = \int_{\mathrm{BW}} v^2_{\mathrm{in},f}\, df \cong \frac{2\,\dfrac{I_B}{M}}{L^2 C^2_{\mathrm{ox}} G^2_m}\,(k'_n K_{Fn} + 2k'_p K_{Fp})\,\ln\left[\frac{1}{\mathrm{BW}}\right]. \tag{13}$$

In these equations, we have assumed that the dimensions of $M1$ and MN are of the same order of magnitude. Accounting for thermal and flicker noise components, the total noise power is computed as

$$v^2_{\mathrm{int},t} \cong \frac{16kT}{3G_m}\,[\mathrm{NF}]\,\mathrm{BW} + \frac{2\,\dfrac{\mathrm{I_B}}{\mathrm{M}}}{\mathrm{L^2 C^2_{ox} G^2_m}} \cdot (k'_n K_{Fn} + 2k'_p K_{Fp})\,\ln\left[\frac{1}{\mathrm{BW}}\right]. \tag{14}$$

In accordance with these results, it can be noted that the noise level can be reduced if L is increased. If the flicker noise component is dominant I_B should be reduced as much as possible; but keeping large G_m values.

In this design, transistors MM, $M1$, and MN are biased near the weak inversion region where, low levels of bias current (<100 nA) with moderate transistor dimensions can easily be driven. Since the circuits are designed for very-low-frequency applications, the flicker noise components can be reduced to a few microvolts by using P-channel transistors and increasing the

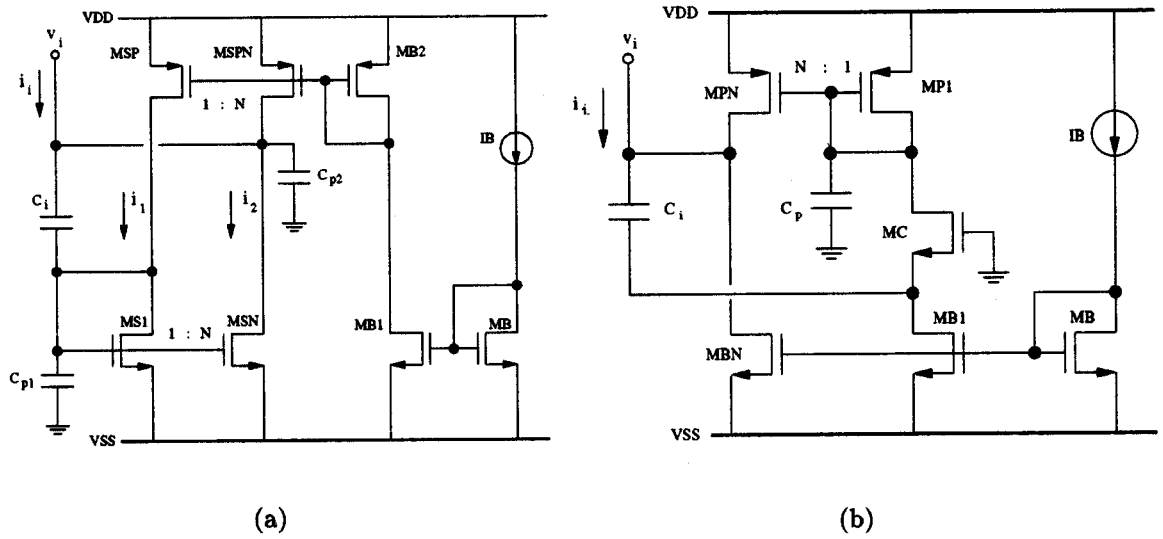

Fig. 5. Scaling up a grounded capacitance. (a) Basic circuit. (b) Capacitance scaler using a cascode transistor.

gate area of the most critical ones. As a result, thermal noise could be even more important than flicker noise components.

IV. Implementation of Effective Large Capacitors

In OTA-C filters the pole's frequency is given by

$$f_o = \frac{G_m}{2\pi C_L} \tag{15}$$

then by making C_L larger, large small signal transconductances can be used leading to reductions in the noise level. An efficient technique for the design of large capacitors will now be presented.

The effective impedance of an element is inversely proportional to the input current, if more current is generated by the same input voltage the equivalent input impedance is reduced. In the case of capacitive impedances, the equivalent capacitance is increased. If the input current is sampled, amplified, and fed back to the input, then the equivalent impedance is scaled down by the current amplification factor. The resulting impedance will depends on both the current gain factor and the original impedance. A capacitive scaler based on this principle is shown in Fig. 5(a).

By using typical circuit analysis techniques it can be shown that the equivalent input impedance becomes

$$Z_i = \frac{v_i}{i_i} = \frac{1}{s(N+1)C_i} \tag{16}$$

or $C_L = (N+1)C_i$, where N is the scaling factor of the impedance scaler, defined as the ratio of the small signal transconductances of MSN and $MS1$, and C_i is the basic capacitor.

A. Design Considerations for the Impedance Scaler

1) Pole Frequency and Finite Impedance: When designing the capacitor scaler, the following design considerations must be taken into account. According to Fig. 5(a), C_i is connected in series with the impedance due to the diode connected transistor. Parasitic capacitances are represented by C_{p1}. Capacitor C_{p2} accounts for the parasitic capacitors associated with node v_i. The output conductance of MSN should be considered because it limits the low frequency response of the equivalent capacitor. After taking into account these elements, the equivalent circuit is shown in Fig. 6.

By using typical circuit analysis techniques it can be shown that the small signal admittance becomes

$$\frac{i_{\text{in}}}{v_{\text{in}}} = g_{oMSN} + g_{oMSP} + sC_{p2} + s(N+1)C_i \frac{1 + s\dfrac{C_i}{(N+1)g_{mMS1}}}{1 + s\dfrac{C_i + C_{p1}}{g_{mMS1}}}. \tag{17}$$

From (17), the following three facts can be concluded.

1) $g_{oMSN} + g_{oMSP}$ is dominant at low frequencies, limiting the quality factor of the equivalent capacitor.
2) The precision of the equivalent capacitor is limited by both transistor mismatches (N-factor) and parasitic capacitors, which are accounted in C_{p2}.
3) The frequency response is limited by the parasitic pole located at $g_{mMS1}/(C_i + C_{p1})$. For proper operation, this pole must be placed at higher frequencies than the pass-band frequency, e.g., $g_{mMS1}/(C_i + C_{p1}) > 10\omega_o$. The zero is located at higher frequencies, and typically does not play an important role in the circuit.

Neglecting the pole-zero pair, the equivalent admittance can be approximated as

$$\frac{i_{\text{in}}}{v_{\text{in}}} = g_{oMSN} + g_{oMSP} + s[C_{p2} + (N+1)C_i]. \tag{18}$$

2) Noise: If $N \gg 1$ and accounting for the noise sources, it can be found that the scaler's output referred noise is approximately given by

$$i_{o,t}^2 = i_{o,\text{th}}^2 + i_{o,f}^2 \cong \frac{8kTN^2}{3}(g_{mMS1} + g_{mMSP}) + \frac{2I_{MSP}N^2}{C_{\text{ox}}^2 L^2 f}(k_n' K_{Fn} + 2k_p' K_{Fp}). \tag{19}$$

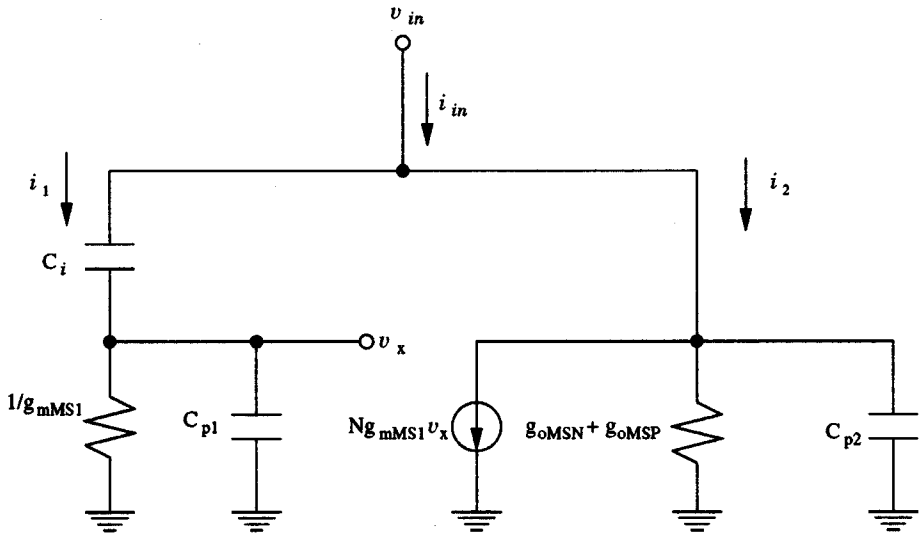

Fig. 6. Small signal circuit for the capacitor scaler.

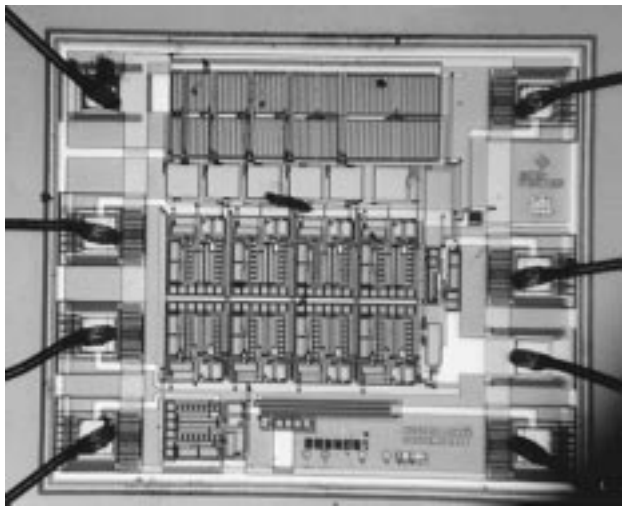

Fig. 7. Microphotograph of the chip.

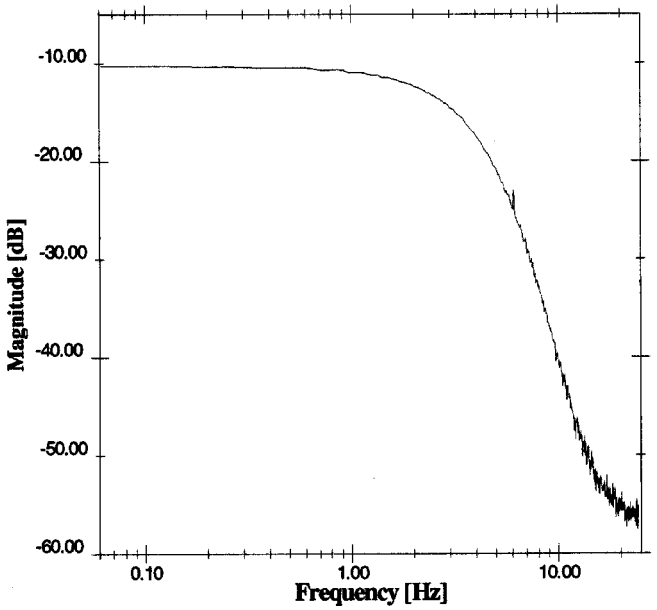

Fig. 8. Experimental frequency response for the filter.

If these noise components are reflected to the integrator's input and are integrated over the filter's BW the integrated noise power due to the scaled capacitors becomes

$$v_{\text{int},t}^2 \cong \frac{8kTN^2}{3G_m}\left[\frac{g_{mMS1}+g_{mMSP}}{G_m}\right]\text{BW} + \frac{I_{MSP}N^2}{G_m^2L^2C_{ox}^2}\left(k_n'K_{Fn}+2k_p'K_{Fp}\right)\ln\left[\frac{1}{\text{BW}}\right]. \quad (20)$$

From (20), it can be noted that thermal noise components could be the dominant ones because flicker noise components can be reduced by increasing L and reducing I_{MSP}. For this design, channel lengths of 100 μm are employed. Because of its lower flicker noise constant, P channel transistors are used in the most critical parts of the design. The basic capacitor value is $C_i = 5$ pF. To obtain a significant reduction in the noise level introduced by the impedance scalers, the transistors employed in this scheme are biased close to weak inversion where low bias current values (≈50 nA) are used [17]. The major drawback of this scheme is that for proper frequency operation of the impedance scaler, the parasitic pole must be placed at higher frequencies than the passband frequency, as discussed in Section IV-A. To this end, g_{mMS1} must be increased as much as possible. However, to mantain low noise levels in the impedance scaler the factor g_{mMS1} should be further reduced [see (20)]. This drawback is overcome if a cascode structure is used as shown in Fig. 5(b). In this architecture, C_i is connected to the cascode transistor MC instead of to the current mirror. It is well-known that noise contribution of cascode transistors is negligible. As a result of this, the noise performance is similar for both structures. Transistor MC can be optimized for frequency response. The scaling factor is controlled by $MP1$ and MPN. The current mirror should be optimized for both precision and noise. Thus, noise performance and frequency of operation for the impedance scaler of Fig. 5(b) are almost independent. In this paper, the impedance scaler was implemented using the circuit shown in Fig. 5(a).

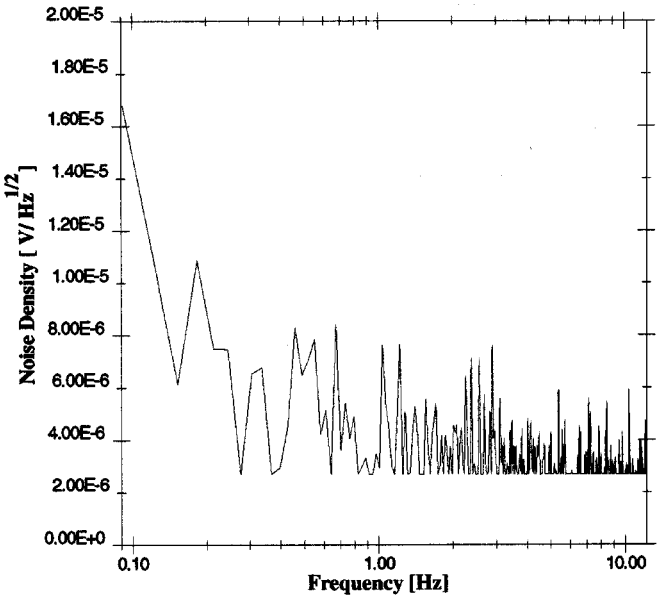

Fig. 9. Measured output referred noise voltage density for the sixth-order low-pass filter.

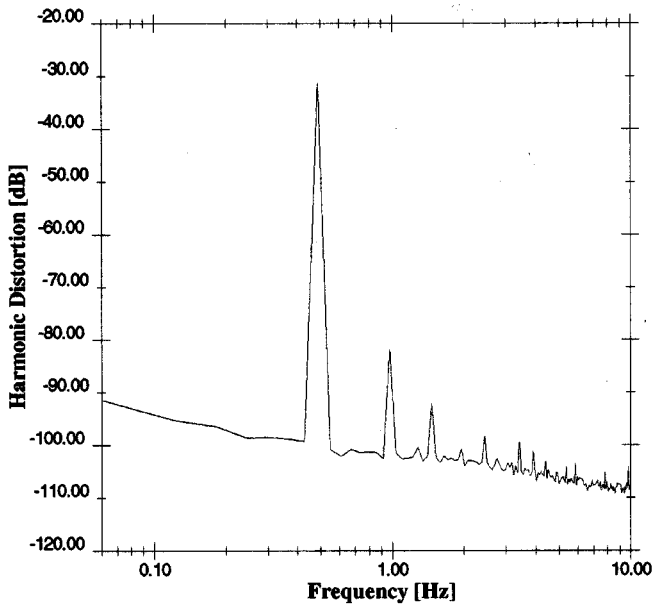

Fig. 10. Measured harmonic distortion components for the single-ended filter.

V. Experimental Results

The filter was fabricated in a double-poly double-metal 0.8-μm CMOS process; a micro photograph of the chip is shown in Fig. 7. The active area is around 1 mm^2 without considering pads and an extra OTA.

The measured magnitude response for the filter is shown in Fig. 8. It can be observed in this plot that the -3-dB frequency is around 2.4 Hz. The dc gain is around -10 dB, instead of the ideal -6 dB, passband gain. This is due to the effects of the finite output resistance of the transistors. To overcome this drawback either larger channel lengths or cascode structures could be employed.

TABLE I
Experimental Results for the Single-Ended Sixth-Order 2.4-Hz Filter

Parameter	Measured
Filter order	6th
Bandwidth	2.4 Hz
Integrated Noise @ $0.1 - 2.4$ Hz	$< 50\,\mu$V
HD3 @ $V_{in} = 100$ mV	< -60 dB
Dynamic Range @ THD < -50 dB	> 60 dB
PSRR, VDD @ 2.4 Hz	-65 dB
PSRR, VSS @ 2.4 Hz	-66 dB
Power Consumption	10 μW
Power Supply	± 1.5 V
Active area	≈ 1 mm^2

The output referred noise density is shown in Fig. 9. Integrating the passband noise from 0.1–2.4 Hz gives us an input referred noise voltage below 50 μV.

The measured harmonic distortion components for a 100-mV/500-mHz input signal are shown in Fig. 10. It can be noted, in this figure, that the harmonic distortion components are below -50 dB. Note that the dominant harmonic distortion is HD2, which can be further reduced by using fully differential structures. HD3 is around -70 dB and the dynamic range with the THD below -50 dB is approximately 60 dB.

The experimental results are summarized in Table I.

VI. Conclusion

It has been shown that linear voltage-to-current tranducers combined with current division and current cancellation techniques can be efficiently used for the implementation of low-noise low-distortion OTAs suitable for low-frequency applications. The efficiency of an impedance scaler scheme based on a simple current mirror has been experimentally demonstrated. It has been shown that high-performance very-low-frequency filters can be efficiently implemented in CMOS technologies.

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