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A 60-GHz CMOS VCO Using Capacitance-Splitting and Gate–Drain Impedance-Balancing Techniques

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***Abstract*—The design and measurement of a 60-GHz 90-nm CMOS voltage-controlled oscillator is presented. To reduce the power consumption and to improve the phase-noise performance, a capacitance-splitting and a gate–drain impedance-balancing techniques, which are realized with an inductive divider, are proposed. With these techniques, the size of the cross-coupled pair is reduced. Analysis of the proposed techniques shows that the transistor g_m generation efficiency is improved and the oscillator noise factor is reduced. Moreover, the tank loaded quality factor is increased by balancing impedance levels across the transistor terminals. The 60-GHz oscillator was fabricated in a 90-nm CMOS technology. Under 0.6-V supply, the oscillator achieved a tuning range from 61.1 to 66.7 GHz, consuming only 3.16 mW. At 64 GHz, the phase noise is −95 dBc/Hz at 1-MHz offset.**

***Index Terms*—LC oscillator, millimeter-wave oscillators, phase noise, quality factor, voltage-controlled oscillator (VCO).**

I. Introduction

As A critical element of a frequency synthesizer, the oscillator phase noise has in many aspects a large impact on the system performance. Signal selectivity and the bit-error rate worsen significantly when the oscillator phase noise increases. Also, the oscillator power consumption is important when used in wireless applications. Recently, the 60-GHz wireless personal area network (WPAN) standard IEEE 802.15.3c was proposed. This new standard is very suitable for future indoor network applications [1]. This standard uses advanced modulation schemes, like orthogonal frequency division multiplexing quadrature amplitude modulation (OFDM-QAM), to achieve network speed in the range of gigabits per second. Unfortunately, these modulation schemes bring forth stringent phase-noise requirements for the oscillator [2].

Due to technology scaling, f_T and f_{MAX} of advanced CMOS devices are now around 200 GHz or even higher. Therefore, many millimeter-wave circuits can be fabricated using a nanoscale CMOS technology with the advantages of low-cost and high integration levels [3]–[5]. Recently, a number of fundamental-frequency CMOS oscillators working around 60 GHz have been reported [6]–[13]. However, as mentioned in [13], millimeter-wave oscillator design has many challenges caused by the high operating frequency and the large required tuning range. These challenges are summarized as follows: 1) the varactor quality factor is very low at 60 GHz, it is thus very difficult to meet the system phase noise requirements; 2) the linearity of the LC tank suffers from the nonlinear capacitance contributed mainly by the active device and the varactor; and 3) the tuning range has to be very large to cover the wide frequency band around 60 GHz [1]. A very large voltage-controlled oscillator (VCO) gain K_{VCO} is therefore required. To linearize the LC tank and to reduce the K_{VCO}, a switched capacitance technique can be used, but only if switch loss can be tolerated. Or to reduce the AM noise effect on the phase noise, a switch tuning technique can be used if the layout routing can be solved [13]. Combined with the bad reactive linearity of the LC tank, the stringent K_{VCO} requirement makes it very difficult to improve the phase noise. How to achieve low phase noise while consuming low power is therefore still very challenging for millimeter-wave oscillators.

To address the oscillator challenges, this paper presents a capacitive splitting and a gate–drain impedance-balancing techniques, which are realized using an inductive divider [15]. In this way, the active device size can be reduced by half, and therefore, the power consumption is also reduced. Analysis also shows that, with the proposed techniques, the g_m generation efficiency of the differential cross-coupled pair is improved, whereas the oscillator noise factor, and thus, the phase noise, are reduced. Moreover, the tank loaded quality factor is increased.

Section II first reviews millimeter-wave oscillator phase-noise generation mechanisms. The criteria to build a good oscillator are then defined and the performance limitations of millimeter-wave oscillators are identified. In Section III, a capacitance-splitting technique is used to enhance the g_m generation efficiency at millimeter-wave frequencies. Regarding the transistor terminal resistance difference, Section IV introduces a gate–drain impedance-balancing technique. Its effect on the oscillator noise factor and the loaded quality factor is then analyzed. In Section V, a prototype oscillator is implemented using an inductive divider, and the transistor biasing point selection is discussed. In Section VI, the oscillator measurement results are presented. Final conclusions are drawn in Section VII.

II. Design Issues in CMOS Millimeter-Wave Oscillators

A. Phase-Noise Generation Mechanisms

As shown in Fig. 1, a simple cross-coupled oscillator consists of three parts, which are: 1) an LC tank for frequency selection; 2) an active differential cross-coupled pair to compensate the tank losses; and 3) buffer amplifiers to provide output driving and isolation purposes. The capacitive loading from the

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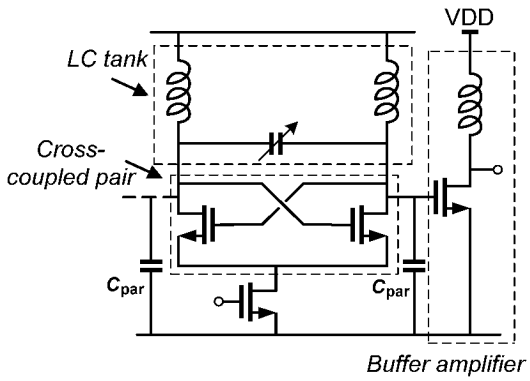

Fig. 1. Simple cross-coupled oscillator.

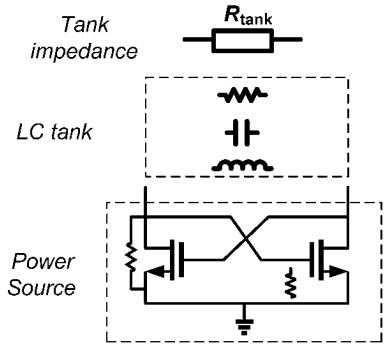

Fig. 2. Simple cross-coupled oscillator without tail current.

buffer amplifiers, the cross-coupled pair, and interconnection lines makes it very difficult to achieve a large tuning range [13].

Two important mechanisms contribute to the phase noise in an oscillator [14], [16]–[19]. One source of phase noise is coming directly from the negative g_m transistors and the resistive losses of the LC tank. These phase-noise generation mechanisms are described by the Leeson formula (1) [16]

$$L(\Delta\omega) \propto F\frac{4KTR_{\rm tank}}{V_0^2}\left(\frac{\omega_0}{2Q_{\rm tank}\Delta\omega}\right)^2 \qquad (1)$$

with F being the noise factor, K being the Boltzmann constant, T being the temperature, V_0 being the signal amplitude, ω_0 being the center frequency, and $Q_{\rm tank}$ being the tank loaded quality factor. According to (1), to achieve a good phase noise, the tank loaded quality factor needs to be maximized. The signal amplitude across the tank also needs to be maximized, but this is limited by the transistor reliability issues.

A second source of phase noise comes indirectly via the control lines, power supply, and biasing circuitry. The AM noise will be converted into phase noise by modulating the effective capacitance and the level of the harmonics [17], [19], [20]. Moreover, this phase-noise generation depends not only on the tank quality factor, but also on the harmonic level [13], [17], [21]. Since the LC tank quality factor is very low at millimeter-wave frequencies, this naturally sets some requirements on the achievable linearity of the active device, i.e., a larger $V_{\rm gs} - V_t$ is required [22].

To summarize, the design of an LC oscillator is generally divided into two aspects: one is to maximize the LC tank frequency selectivity, i.e., to maximize the tank loaded quality factor $Q_{\rm tank}$; the other is to reduce the phase-noise contribution of the active devices. The latter can usually be done through improving the cross-coupled pair linearity and preventing the tail current noise from entering the tank with a filter or a capacitor [14], [23]. Here, to suppress the noise upconversion and to improve the linearity of the cross-coupled pair, the tail current is removed, leading to Fig. 2. This structure is usually called a voltage biased oscillator [13], [14], whose main disadvantage is that the oscillator is very sensitive to the power supply (typically called frequency pushing). As pointed out in [13], a low-noise low-dropout voltage regulator can solve this problem.

B. Performance Limitations in Millimeter-Wave Oscillators

The investigation below will show that, in high-frequency oscillators, the effect of the active device on the passive LC tank and the phase noise is very important. Before doing such investigation, let us firstly define a criterion for a good oscillator. An oscillator can be generally split into a power source and a frequency-selection tank. In a good oscillator, a power source supplies the power periodically and efficiently to a frequency-selection tank. As shown in Fig. 2, the power source is an amplifier (i.e., a cross-coupled pair), and the frequency selection tank is realized with an LC-circuit, whose impedance is $R_{\rm tank}$ at the target operating frequency. Periodicity is essential in the oscillator design, and the efficiency shows how well the oscillator is constructed.

Generally, the active device working speed is the same as that of the output signal, but to overcome the active device speed limit, special techniques can be used to achieve an oscillation signal with a frequency higher than the active device working speed. For example, in oscillators using a push–push technique [4], [5] or a linear superposition technique [24], the active device working speed is lower. However, in these techniques, special attention has to be paid to the oscillator working efficiency since the output power is low.

Besides maximizing the tank quality factor, the efficiency of oscillators can be improved by careful design of the amplifier in the oscillator. To be more specific, as the driving part of the LC tank, the amplifier (in this case, the cross-coupled pair) should compensate the losses of the LC tank efficiently without introducing too much loading on the LC tank. Besides the loading, the active device also affects the phase noise through the oscillator noise factor F [14], [17], [25], given in (2) as follows:

$$F = (1 + \gamma g_m R_{\rm tank}). \qquad (2)$$

Due to the excess loop gain $g_m R_{\rm tank}$, the noise factor and noise multiplication are increased [25]. γ depends on the transistor biasing, and is typically 2–3-in-deep submicrometer technologies [26].

At high frequency, the cross-coupled differential pair performance is not good. This can be clearly seen in Fig. 3, which plots the differential negative transconductance g_m versus frequency. Fig. 4(a) depicts a simplified g_m simulation setup. The negative g_m of the cross-coupled pair, calculated as $\mathrm{Re}(1/Z_{\rm in})$,

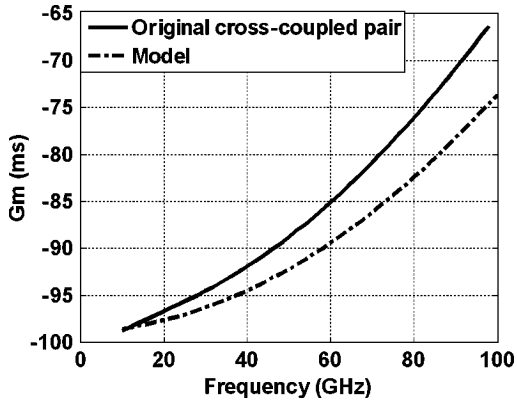

Fig. 3. Negative g_m versus frequency (the original differential cross-coupled pair and its model).

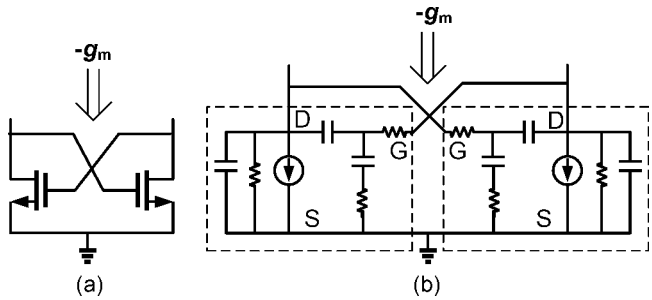

Fig. 4. Negative g_m simulation setup. (a) Original differential cross-coupled pair. (b) Model.

decreases more than 30% from 20 to 100 GHz in a 90-nm technology. A first-order transistor model, given in Fig. 4(b), allows to derive the negative g_m as a function of frequency. The result of this analysis is plotted in Fig. 3 for comparison. Although Fig. 4(b) depicts a first-order model, the model and simulation show the same trend. The decrease of the negative g_m with frequency is thus due to the RC bandwidth limitation of the cross-coupled pair and the transistor resistive loading effect.

This loading effect is caused by the transistor terminal resistive impedance $R_{\rm ds}$ and $R_{\rm gate}$. Fig. 5 shows the real parts of the equivalent parallel input and output impedances of a transistor. At 60 GHz, the output resistance $R_{\rm ds}$ is about 500 Ω and the parallel input gate resistance $R_{\rm gate}$ is about four times larger, i.e., 2.4 kΩ. This is caused by the gate resistance loss and the nonquasi-static effect. The output impedance decreases with frequency due to $C_{\rm gd}$ shunt feedback. Both $R_{\rm ds}$ and $R_{\rm gate}$ will introduce more loading on the LC tank when the frequency increases.

Since the transistor g_m is decreasing with frequency, a larger transistor size is needed for oscillation startup at millimeter-wave frequency. Suppose that the transistor size is increased, its terminal parallel impedances will be reduced proportionally. Analysis shows that a larger power will be consumed and more resistive loading will be introduced into the LC tank, thereby reducing the tank loaded quality factor; hence, reducing the phase noise performance. These phenomena show that regarding the tank impedance $R_{\rm tank}$, the sizing and biasing of the active devices is very critical in millimeter-wave oscillator design.

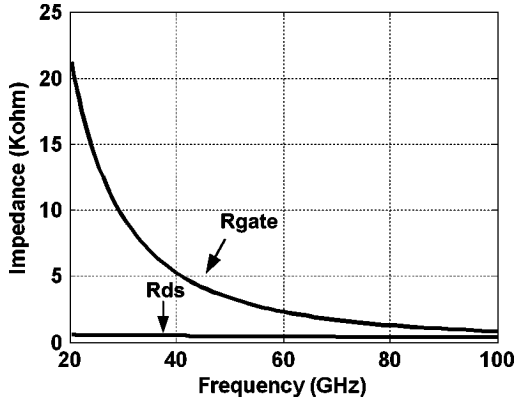

Fig. 5. Transistors' real parts of parallel input and output impedances.

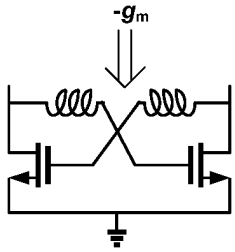

Fig. 6. Modified differential cross-coupled pair.

The discussion above clearly indicates that both the oscillator noise factor and the tank loaded quality factor are a function of the active devices. After arranging (1) into (3), one can easily see that in order to reduce the phase noise for a certain signal swing, an efficient loss compensation scheme is required while minimizing the $F/Q_{\rm tank}^2$

$$L(\Delta\omega) \propto \frac{F}{Q_{\rm tank}^2}\frac{4KTR_{\rm tank}}{V_0^2}\left(\frac{\omega_0}{2\Delta\omega}\right)^2. \tag{3}$$

III. Capacitance-Splitting Technique

A capacitance-splitting technique is introduced to solve the bandwidth limitation of the cross-coupled pair, resulting in a modified cross-coupled pair (see Fig. 6). An inductor is inserted between the drain of one transistor and the gate of the other transistor. With help of the inductor, the cross-coupled pair parasitic capacitances are split. It can be understood intuitively that the differential cross-coupled pair becomes distributed from a lumped g_m generation cell.

In this way, the performance of the modified cross-coupled pair is improved a lot, which can be clearly seen in Fig. 7. Compared to the original cross-coupled pair with the same size, the negative g_m at 60 GHz has been improved by about 30%, meaning the transistor g_m generation efficiency is improved. Since the g_m generation efficiency of the modified cross-coupled pair is much higher than the original one, the size of the cross-coupled pair can be smaller, resulting in a lower power consumption. The operating frequency of the oscillator using the modified cross-coupled pair can also be higher when compared to the original cross-coupled pair.

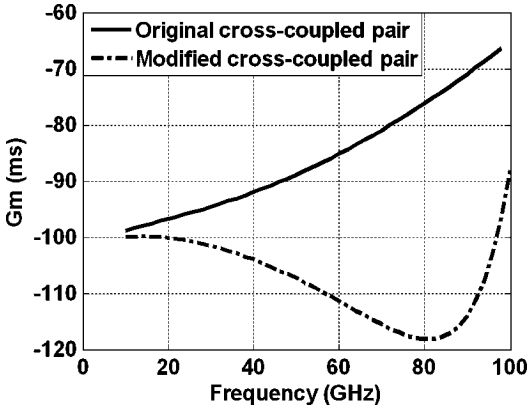

Fig. 7. Negative gm versus frequency (the original and modified differential cross-coupled pair).

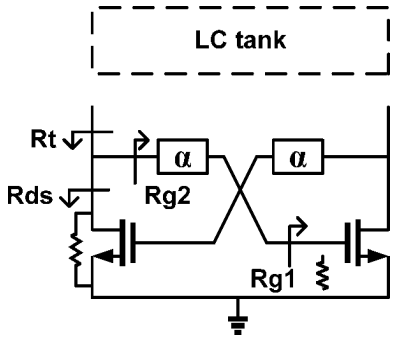

Fig. 8. Cross-coupled pair with the impedance-balance technique.

IV. Gate–Drain Impedance-Balancing Technique for Millimeter-Wave Oscillators

The resistive impedances at the transistor gate and drain terminal will reduce the LC tank loaded quality factor. To solve this problem, a gate–drain impedance-balancing technique is proposed. This is motivated by taking into account the difference between the transistor's equivalent parallel input (gate) and parallel output (drain) resistances. The proposed technique is shown in Fig. 8. An impedance-transformation block with a voltage gain α is introduced between the gate and drain. From Fig. 8, the small-signal loop gain of the oscillator can be written as

$$\text{Loop gain} = g_m R_{\text{tank}} \alpha. \tag{4}$$

First suppose $\alpha = 1$, i.e., the gate and drain of the cross-coupled pair are directly connected, as shown in Fig. 2. Cross-coupled transistors with a certain size are required for the oscillation startup. Simulations find the transistor's parallel input R_{g1}, and parallel output resistances R_{ds} to be about 1.2 kΩ and 250 Ω, respectively. Now suppose the tank parallel impedance R_{tank} is designed to be constant. If an extra gain stage with the voltage gain α is inserted between the gate and drain, according to (4), the transistor sizes can be scaled down. Therefore, the terminal parallel resistances of the transistors are scaled up proportionally. R_{g1} becomes 1.2 α kΩ and R_{ds} becomes 250 α Ω. With the impedance-transformation block, the gate parallel resistance R_{g1} is transformed into R_{g2}, i.e., $R_{g2} = R_{g1}/\alpha^2 = 1.2/\alpha$ kΩ, and the transistor total parallel resistance R_t, the parallel resistance of the transistor terminal impedance R_{g2} and R_{ds}, can be written as

$$R_t = \frac{R_{\text{ds}} R_{g2}}{R_{\text{ds}} + R_{g2}} = \frac{250 \times 1200}{250\alpha + 1200/\alpha}. \tag{5}$$

Calculations find that, when $\alpha = 2.2$, transistor terminal impedance R_t is largest, which is the optimum condition for the tank loaded quality factor.

In this design, for layout convenience, α is set to 2. Since the gate terminal parallel resistance R_{g1} is about four times larger than the drain parallel resistance R_{ds}, the impedances between the drain and gate side are now balanced

$$R_{g2} = R_{g1}/\alpha^2 = R_{g1}/4 \approx R_{\text{ds}}. \tag{6}$$

When compared to the case where $\alpha = 1$, it is found that, when $\alpha = 2$, the total transistor terminal resistance R_t is about 32% higher. Therefore, the tank loaded quality factor Q_{tank} is higher. In addition, according to (4), compared to the case where $\alpha = 1$, when $\alpha = 2$, the power consumption can be decreased by half.

Now let us look at the noise factor F. The noise factor F of the cross-coupled pair oscillator, for the proposed impedance-balancing technique, can be derived as [26]

$$F = \left(1 + \frac{\gamma g_m R_{\text{tank}}}{\alpha}\right). \tag{7}$$

Interestingly, besides the reduction due to the smaller g_m, the oscillator noise factor is reduced further when $\alpha = 2$. Therefore, at least 3-dB phase-noise reduction will be expected with the proposed technique, which is verified by the test results. The phase-noise reduction can be understood as follows: with the impedance-transformation technique, the transistor size can be reduced. It means that less noise from the transistor is injected into the tank, thereby reducing the noise factor. In addition, the passive amplification gain α in front of the transistor gate suppresses the transistor noise further, thus a lower noise factor is achieved.

V. Implementation of a Prototype Low Phase-Noise Oscillator

The prototype oscillator structure is shown in Fig. 9. In this structure, to take advantage of both the capacitance-splitting and the impedance-balancing technique, an inductive divider is used. Inductors L_1 and L_2, whose values are equal to about 60 pH, are used to realize the impedance-transformation block with the voltage gain $\alpha = 2$.

The proposed oscillator structure resembles a Hartley oscillator [28]. However, the operation mechanism is different. This can be understood when looking at the negative g_m generation mechanism and the feedback network connection. In the Hartley oscillator, the negative g_m is generated with the LC tank inherent phase inversion property. This generates the positive feedback for the oscillation. In contrast, the positive feedback in the proposed oscillator is realized with the cross-coupled pair, resulting in the negative g_m. In the feedback network connection of the Hartley oscillator, the MOS transistor source terminal is

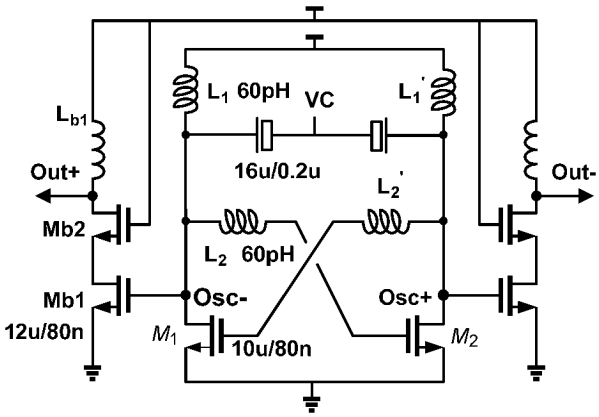

Fig. 9. Whole oscillator including the cascode buffer amplifier.

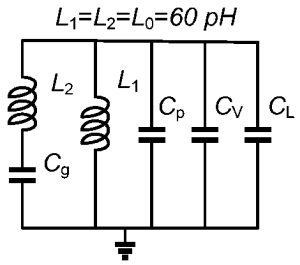

Fig. 10. *LC* tank model of prototype oscillator.

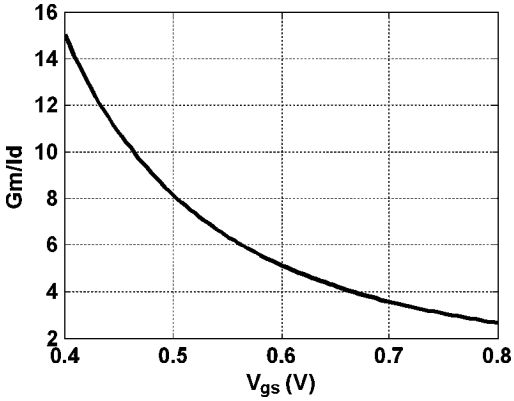

Fig. 11. g_m/Id versus $V_{\rm gs}$ @ 60 GHz.

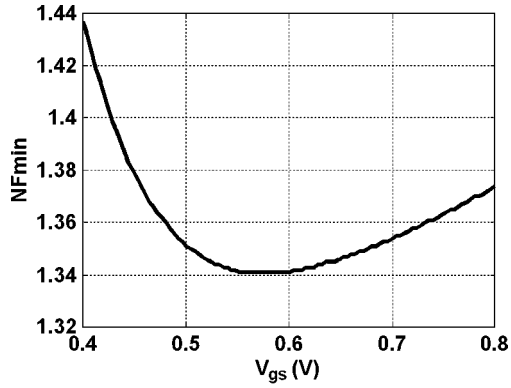

Fig. 12. $\mathrm{NF}_{\min}$ versus $V_{\rm gs}$ @ 60 GHz.

connected in between two inductors. If the coupling of the two inductors is not perfect, there will be some leakage inductance in series with the transistor source, and this leakage inductance will affect the Hartley oscillator operation [29].

The LC tank model of the prototype oscillator is given in Fig. 10, with C_V being the varactor capacitance, C_g being the gate capacitance of the cross-coupled pair, C_p being the parasitic capacitance including the cross-coupled pair drain capacitance and interconnect line capacitance, and C_L being the buffer amplifier input capacitance. For simplicity, the lossy element is neglected. The proposed oscillator is a fourth-order system, and it has two possible oscillation frequencies, shown in (8) at the bottom of this page.

Simulations show that the circuit can only work at the lower frequency because the loop gain at the higher frequency is too low. From (8), we can see that due to the impedance transformation, the impact of the transistor gate capacitance on the oscillation frequency is two times as large as the effect of other capacitances. However, if there is no impedance transformation, the transistor size would have to be doubled. This means that, when compared to the case where $\alpha = 1$, the proposed technique has no negative impact on the tuning range. Furthermore, according to (8), since the capacitance is split by the inductor L_2, the proposed circuit can achieve a higher operating frequency. Moreover, the series L_2 and C_g help to suppress to a certain extent the AM noise effect on the phase noise, which is caused by inductive and capacitive power imbalance [21].

As mentioned before, the biasing of transistors is very critical for the millimeter-wave oscillator design. In the prototype oscillator, the transistor biasing point is selected with respect of the g_m generation efficiency, noise, speed, and linearity requirement. With an S-parameter simulation at 60 GHz, g_m/I_d and $\mathrm{NF}_{\min}$ versus the gate voltage $V_{\rm gs}$ are generated. As shown in Fig. 11, g_m/I_d reduces when $V_{\rm gs}$ increases. This is a well-known tradeoff between linearity and g_m generation efficiency. $\mathrm{NF}_{\min}$ is a bathtub curve, shown in Fig. 12. Based on this curve, the voltage region around 0.6 V is a good biasing region. As discussed in Section II, the degradation of g_m with frequency requires biasing towards high $f_{\rm MAX}$. According to the $f_{\rm MAX}$ versus $V_{\rm gs}$ curve in Fig. 13, the region from 0.6 to 0.8 V looks like an inverse bathtub, and it is very flat. Therefore, combining the requirements on the noise, the g_m efficiency, linearity, and

$$\omega_{1,2}^2 = \frac{2}{L_0\left(2C_g + (C_p + C_V + C_L) \pm \sqrt{(2C_g)^2 + (C_p + C_V + C_L)^2}\right)} \tag{8}$$

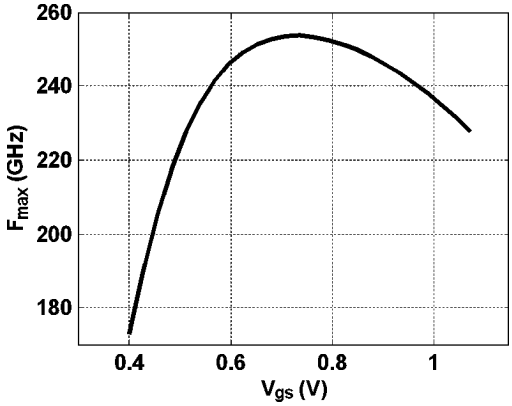

Fig. 13. F_{MAX} versus V_{gs} curve.

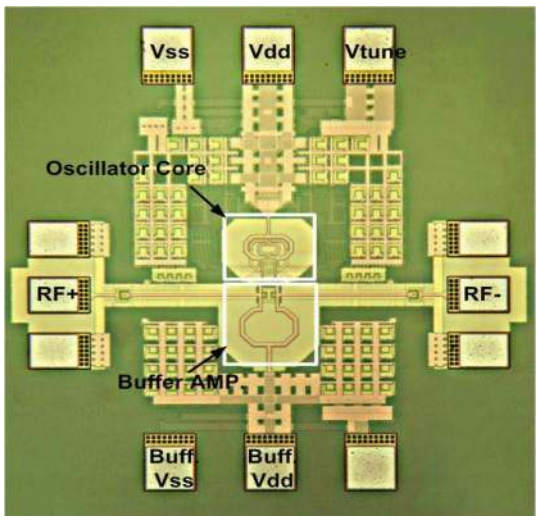

Fig. 14. Chip micrograph.

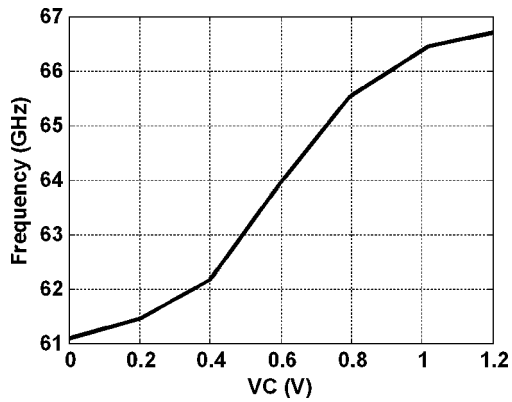

Fig. 15. Tuning curve.

speed, it can be concluded that, in this design, 0.6 V is an optimum bias point.

The prototype oscillator was fabricated in a 90-nm CMOS technology, and the chip micrograph is shown in Fig. 14. In this figure, the differential inductors L_1 and L_2 are realized using a three-turn inductor. The winding of this inductor is designed to make use of the positive magnetic coupling, thus making the LC tank area very compact. The area of the core LC oscillator and the buffer amplifier are both about $110 \times 80\ \mu\mathrm{m}^2$. During the process of designing the inductor, special attention was paid to the balance between the self-resonance frequency and the losses of the internal inductors L_2. The reason is that the parasitic capacitance limits the tuning range, while the loss will reduce the tank quality factor.

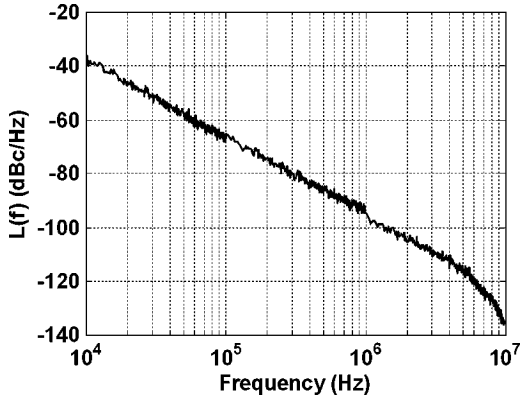

Fig. 16. Phase noise @ 64 GHz.

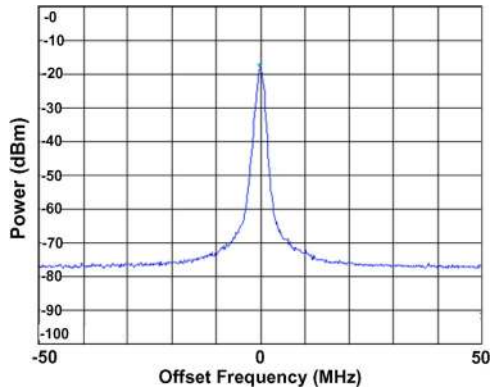

Fig. 17. Measured spectrum at 64 GHz (Frequency Span = 100 MHz, Resolution Bandwidth = 1 MHz, Video Frequency = 10 kHz).

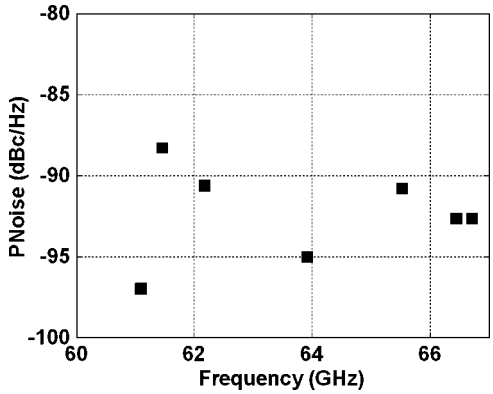

Fig. 18. Measured phase noise @ 1-MHz offset across the tuning range.

VI. Measurement Results

With a 0.6-V supply voltage, the oscillator consumes a dc power of only 3.16 mW. The output signal is tested on chip with a spectrum analyzer and a waveguide harmonic mixer. The tuning curve of the oscillator is given in Fig. 15. With the tuning voltage ranging from 0 to 1.2 V, the oscillator achieves a tuning range about 5.6 GHz (from 61.1 to 66.7 GHz). The phase

TABLE I
PERFORMANCE SUMMARY OF STATE-OF-ART MILLIMETER-WAVE OSCILLATORS

VCO[Ref]	FO (GHz)	FTR (%)	PNoise (dBc/Hz)	PDISS (mW)	Vdd (V)	FOM (dBc/Hz)	FOM_T (dBc/Hz)	Tech.
H. Wang [6]	49.5	2.21	-99.7@1 M	13	1.3	-182.4	-169.3	0.25 μm CMOS
M. Tiebout [7]	51.2	1.39	-85@1 M	1.0	1	-179.2	-162.	0.12 μm CMOS
F. Ellinger [8]	56.5	14.7	-92@1 M	21.0	1.5	-173.8	-177.3	90 nm SOI
C. Cao [9]	56.5	10.27	108@10 M	9.8	1.5	-173.1	-173.4	0.13 μm CMOS
D. D. Kim [10]	70.2	9.55	-106.1@10 M	5.4	1.2	-175.8	-175.4	65 nm SOI
H.-K. Chen [11]	69.8	4.5	-98.8@1 M	4.32	0.6	-188.9	-182	0.13 μm CMOS
			-115.2@10 M	4.32	0.6	-185.7	-178.8	
Borremans [12]	62.1	10	-95@1 M	3.9	1	-185	-185	0.13 μm CMOS
	59.1	10.2	-91@1 M	3.9	1	-180.5	-180.7	
L. Li [13]	58.4	9.32	-90@1 M	8.1	0.7	-176	-176	90 nm CMOS
	61.7	4.81	-90@1 M	1.2	0.43	-185	-178.6	
This work	**64**	**8.75**	**-95@1 M**	**3.16**	**0.6**	**-186**	**-185**	**90 nm CMOS**

a. $\mathrm{FOM} = \mathrm{PNoise} - 20\log(f_0/\Delta f) + 10\log(P_{\mathrm{DISS}}/1\ \mathrm{mW})$
b. $\mathrm{FOM}_T = \mathrm{PNoise} - 20\log((f_0/\Delta f)^*(FTR/10)) + 10\log(P_{\mathrm{DISS}}/1\ \mathrm{mW})$

noise is measured using a PN9000 phase-noise measurement equipment. This equipment employs a delay line method, which is an accurate and reliable phase-noise measurement method for free-running oscillators [25], [30]. The phase-noise curve at 64 GHz is shown in Fig. 16. The oscillator demonstrates −95 dBc/Hz at 1-MHz offset. Test results above 5-MHz offset are not accurate due to a pole effect of the delay line. From Fig. 16, it is clear that the $1/f^3$ slope continues up to 1 MHz. The reason for this could be understood from the phase-noise generation process of the $1/f$ noise. As discussed in [17], [19], [20], and [22], by modulating the harmonic level and effective capacitance of the LC tank, the $1/f$ noise effect will become more pronounced when both the tank quality factor and the linearity of the tank capacitance are low. As mentioned in Section II, in millimeter-wave oscillators, the linearity of the tank capacitance is worse. Moreover, the tank quality factor is low. Therefore, the phase noise at low-frequency offset is dominated by $1/f$ noise. Fig. 17 shows the measured output spectrum at 64 GHz.

Fig. 18 shows the phase-noise results at 1-MHz offset across the tuning range. The fluctuation of the phase noise across the tuning range is due to the worse reactive linearity issues of the LC tank, especially the varactor C–V curve nonlinearity [17], [19], [20]. The good phase-noise results at the lowest frequency and the highest frequency are caused by the varactor capacitance saturation in these two regions, whereas the good phase noise at the center region is due to the symmetry of the varactor C–V curve. In these regions, there is less AM noise conversion to phase noise. This phenomenon has also been observed in [19]. Across the tuning range, the output power is about −14 dBm after calibrating the loss of the cable and the probe with a vector network analyzer (VNA).

Table I offers a performance summary of the state-of-art millimeter-wave fundamental-frequency oscillators. To compare the oscillator performance in phase noise and tuning range, two figure-of-merits (FOMs) are used. At 64-GHz carrier, the oscillator achieves an FOM and FOM_T of −186 and −185, respectively, which advances the state-of-art. Compared to the previous oscillator designed by the authors, thanks to the capacitance-splitting and gate–drain impedance-balancing techniques, the oscillator presented in this paper reduced the dc power consumption by more than half and the phase noise is reduced by about 5 dB. This 5-dB phase-noise reduction can be attributed to two sides: one is the reduction of the oscillator noise factor; the other is the improvement of the tank loaded quality factor and the transistors' optimum biasing point.

VII. CONCLUSION

To achieve low-voltage and power-efficient millimeter-wave oscillators, an inductive divider has been used to realize a capacitance-splitting and a gate–drain impedance-balancing techniques. With these techniques, the transistor g_m generation efficiency is improved and the transistor size is reduced. By balancing the transistor terminal resistive impedances, the loaded quality factor of the LC tank is improved. Moreover, the oscillator noise factor F is also reduced. Therefore, compared with previous reported results, a lower phase noise has been achieved in combination with a lower power consumption.

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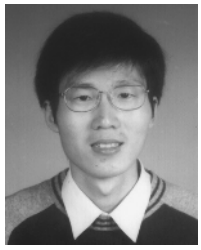

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