A 60 GHz Phase Shifter Integrated With LNA and PA in 65 nm CMOS for Phased Array Systems

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Abstract—**This paper presents the design of a 60 GHz phase shifter integrated with a low-noise amplifier (LNA) and power amplifier (PA) in a 65 nm CMOS technology for phased array systems. The 4-bit digitally controlled RF phase shifter is based on programmable weighted combinations of I/Q paths using digitally controlled variable gain amplifiers (VGAs). With the combination of an LNA, a phase shifter and part of a combiner, each receiver path achieves 7.2 dB noise figure, a 360° phase shift range in steps of approximately 22.5°, an average insertion gain of 12 dB at 61 GHz, a 3 dB-bandwidth of 5.5 GHz and dissipates 78 mW. Consisting of a phase shifter and a PA, one transmitter path achieves a maximum output power of higher than +8.3 dBm, a 360° phase shift range in 22.5° steps, an average insertion gain of 7.7 dB at 62 GHz, a 3 dB-bandwidth of 6.5 GHz and dissipates 168 mW.**

Index Terms—**Active phase shifter, digitally controlled, I/Q signals, low-noise amplifier (LNA), mm-wave, power amplifier (PA), receiver, RF beamforming, RF phase shifting, transmitter, variable gain amplifier (VGA), 60 GHz, 65 nm CMOS, 90° transmission line.**

I. INTRODUCTION

THE 7 GHz unlicensed band around 60 GHz offers exciting opportunities for applications such as high-speed short-range wireless personal area network (WPAN) and real time video streaming at rates of several Gb/s [1]–[3]. Continuous scaling of the CMOS technology results in significant performance improvement, and enables 60 GHz front-ends to be implemented at low cost [4]–[7].

A major issue in designing such a high data rate 60 GHz radio is the limited link budget over indoor distances, especially for the non-line-of-sight (NLOS) situations, due to the high path loss during radio propagation, high noise figure of the receiver and low output power of the transmitter [8], [9]. Due to the relative small size of 60 GHz antennas, the phased array technique is an attractive solution to compensate the path loss

and alleviate the requirements of the RF transceiver front-ends. In addition to providing electronic controlled beam forming, phased arrays offer larger effective isotropic radiated power (EIRP) in the transmitter and higher signal-to-noise ratio (SNR) in the receiver [10]–[15]. This leads to higher system capacity and larger range which is highly beneficial to a 60 GHz wireless system.

Phase shifters are essential components in a phased array for adjusting the phase of each antenna path and steering the beam [16], [17]. Placing the phase shifters in the LO path [18]–[20] or IF path [21]–[24] requires separate frequency converters for each of the antennas, while each frequency converter consists of separate mixers, LO buffers and LO distribution. By placing the phase shifters in the RF path of a receiver/transmitter, the signals from/to each of the antennas are combined/split at RF [Fig. 1(a) and (b), respectively], which shares the frequency converter among the multiple antennas and results in simple system architecture [25]–[28]. An RF phase shifter may require a higher dynamic range as compared to an LO phase shifter. On the other hand, an RF phase shifting approach keeps the floor plan of the LO circuitry simple, i.e., there is only a single mixer (or two in an I/Q scheme) to be driven by the LO signal. This also means that the core circuitry of the receiver and transmitter (up to the mixer) can be reused for different array configurations, without the need to add additional mixers to the circuitry when, for example, increasing the number of antennas. At the end, the number of physical circuit elements is smaller in an RF phase shifting scheme than in an LO phase shifting scheme, leading to a smaller chip area. Another aspect of RF phase shifting is that in the receiver, because of the spatial filtering of interferers at RF, the dynamic range and therefore the power dissipation of the mixers and subsequent stages can be reduced.

The main challenge associated with RF phase shifting is the implementation of low-loss high-resolution RF phase shifters at 60 GHz. This work proposes a 4-bit digitally controlled RF phase shifter that is based on programmable weighted combinations of I/Q paths with digitally controlled variable gain amplifiers (VGAs) [29]. Compared to the passive designs [30]–[34], this phase shifter achieves high gain, small area, large phase shift range (360°) and high phase shift resolution (22.5°). Instead of using an all-pass polyphase filter [35], [36] or quadrature coupler [34], the I/Q signals are generated using a 90° transmission line that enables low loss and sufficient I/Q accuracy. The gain settings of the VGAs are achieved through digitally controlled current steering by turning on or off a certain number of unit transistors in parallel. The fully digitally controlled phase shifter allows for a simple control and better immunity to the
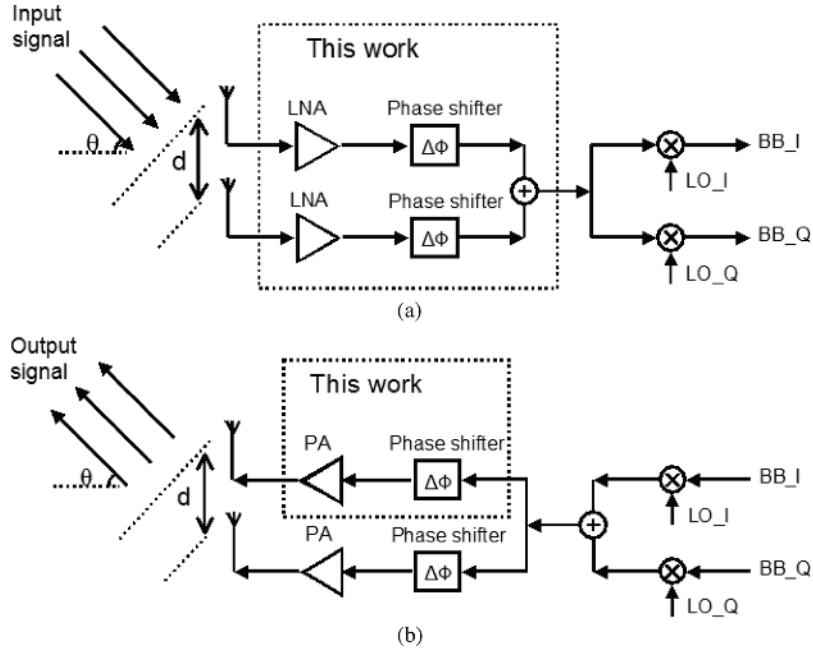
Fig. 1. Block diagram of a 60 GHz phased array (a) receiver and (b) transmitter front-end using RF-path phase shifting.

noise in the control lines. With the use of the proposed 4-bit RF phase shifter, this work designs a 60 GHz two-path receiver in which each path consists of a low-noise amplifier (LNA), a phase shifter and part of a combiner [Fig. 1(a)], and a 60 GHz transmitter path that consists of a power amplifier (PA) and a phase shifter [Fig. 1(b)], both in a 65 nm CMOS technology.

This paper is organized as follows. In Section II, the principle of the proposed RF phase shifter is presented first, followed by the the circuit design of the RF phase shifter as well as LNA and PA for 60 GHz phased array systems. The measurement results of the receiver path and the transmitter path are presented and discussed in Section III.

II. CIRCUIT DESIGN

A. Principle of the Phase Shifter

In this work, the RF phase shifter has a phase resolution of 22.5° (4-bit resolution) and a phase control range of 360°. The propagation time delay in a phased array system is approximated to a constant phase shift over the signal bandwidth, which may lead to distortion in a system that uses a broadband high order modulation scheme or uses an instantaneously wide bandwidth [37], [38]. System simulation shows that the use of a 4-bit constant phase shifter meets the requirements including error vector magnitude (EVM) and array patterns of a 60 GHz 8-path phased array transceiver, which employs shaped QPSK modulation ($\beta = 0.5$) and has bit rates of 10 Gb/s [9]. The phase shifter has low insertion loss (or even gain), low variation in loss, in this way it is not required to implement an LNA or PA with very high gain, programmable gain settings, and large power dissipation in order to compensate the loss and loss variations. Furthermore, the phase shifter requires sufficient linearity. This is because in the receiver path, the LNA and phase shifter
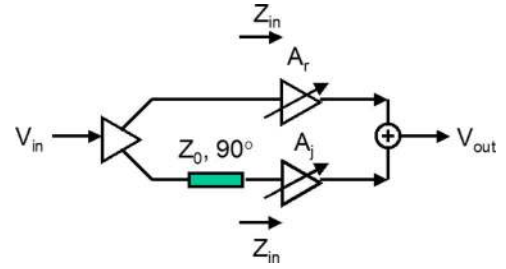
Fig. 2. Block diagram of a phase shifter.

may need to process the desired signals along with strong interferers, whereas beamforming and possible "nulling" of jammer are achieved after signal combining. In the transmitter path the phase shifter should not limit the linearity and output power of the transmitter.

Fig. 2 shows the block diagram of the proposed phase shifter. The input signal (V_{in}) is fed through two paths with or without a 90° phase shift, respectively, which generates I/Q signals. These I/Q signals are weighted by separate VGAs (A_r, A_j) and combined at the output (V_{out}). If the input impedance of each VGA (Z_{in}) is equal to the characteristic impedance (Z_0) of the transmission line, and if there are no gain and phase errors in the I/Q signals, the output signal of the phase shifter can be expressed as

$$V_{out} = (A_r + jA_j)V_{in}. \tag{1}$$

The phase shift achieved is given by

$$\phi = \arctan(A_j/A_r). \tag{2}$$

The gain of the phase shifter can be expressed as

$$A = \sqrt{A_r^2 + A_j^2}. \tag{3}$$

Here A_r and A_j are the gains of the two VGAs in the I/Q paths, respectively, which are given by

$$A_r = A_0 \cos(\phi) \tag{4}$$
$$A_j = A_0 \sin(\phi) \tag{5}$$

in which ϕ is the desired phase shift and A_0 is a constant representing the gain of the phase shifter. In this way, the phase shifter achieves a phase shift of ϕ with a constant gain of A_0.

However, there are often gain errors and phase errors in the weighted I/Q signals before signal combination. This is because, first, the 90° transmission line itself has gain and phase errors. Second, there can be impedance mismatch (and therefore reflection) between the input impedance of each VGA (Z_{in}) and the transmission line (Z_0). In the 60 GHz broadband system, this impedance mismatch is often more severe due to the variation of impedance (Z_{in} and Z_0) within the band of interest. Third, gain and phase errors can also be contributed by the weighting of the two VGAs. If we model the overall gain errors and phase errors in the weighted I/Q signals as ϵ and θ, respectively, the output signal (V_{out}) of the phase shifter can be expressed as

$$V_{\text{out}} = \left[A_r + A_j(1 - \epsilon)e^{j\left(\frac{\pi}{2} - \theta\right)} \right] V_{\text{in}}$$
$$\approx \left[(A_r + \theta A_j) + j A_j(1 - \epsilon) \right] V_{\text{in}}$$
$$= \left[\cos(\phi) + \theta \sin(\phi) + j \sin(\phi)(1 - \epsilon) \right] A_0 V_{\text{in}}. \tag{6}$$

The phase shift achieved due to the gain and phase errors in the weighted I/Q signals is given by

$$\phi' = \arctan \frac{\sin(\phi)(1 - \epsilon)}{\cos(\phi) + \theta \sin(\phi)}. \tag{7}$$

As compared to the ideal phase shift in (2), the phase error of the phase shifter due to the gain and phase errors in the weighted I/Q signals can be written as

$$\Delta \phi = \phi' - \phi$$
$$= \arctan \left[\frac{-\frac{\theta}{2} - \frac{\epsilon}{2} \sin(2\phi) + \frac{\theta}{2} \cos(2\phi)}{1 - \frac{\epsilon}{2} + \frac{\theta}{2} \sin(2\phi) + \frac{\epsilon}{2} \cos(2\phi)} \right]$$
$$\approx -\frac{\theta}{2} - \frac{\epsilon}{2} \sin(2\phi) + \frac{\theta}{2} \cos(2\phi). \tag{8}$$

The RMS phase errors (in radians) of the phase shifter [26], as compared to an ideal phase shifter, can be expressed as

$$\Delta \phi_{\text{RMS}} = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} (\phi' - \phi)^2 d\phi}$$
$$\approx \sqrt{\frac{3}{8}\theta^2 + \frac{1}{8}\epsilon^2}. \tag{9}$$

The gain of the phase shifter with the gain and phase errors in the weighted I/Q signals is given by

$$A' = A_0 \sqrt{(\cos(\phi) + \theta \sin(\phi))^2 + \sin^2(\phi)(1 - \epsilon)^2}$$
$$\approx A_0 \sqrt{1 - \epsilon + \theta \sin(2\phi) + \epsilon \cos(2\phi)}. \tag{10}$$

As compared to an ideal phase shifter, the RMS gain errors (in dBs) [26] of the phase shifter can be expressed as

$$\Delta A_{\text{RMS,dB}} = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} \left(A'_{\text{dB}} - A_{0,\text{dB}} \right)^2 d\phi}$$
$$\approx 8.7 \sqrt{\frac{1}{8}\theta^2 + \frac{3}{8}\epsilon^2}. \tag{11}$$

From (9) and (11), for example, in order to design a 4-bit phase shifter with RMS gain and phase errors of less than 1.7 dB and 11.25°, respectively, we have $\epsilon \leqslant 0.28$ and $\theta \leqslant 0.28$. In other words, in comparison to an ideal phase shifter with perfect I/Q signal generation and weighting, the gain and phase errors in the weighted I/Q signals before signal combination are less than 2.8 dB and 16°, respectively. It is worth pointing out that a 90° transmission line contributes less than 9° phase error within 20% bandwidth at 60 GHz. Therefore, it is used, instead of using a true time delay scheme, to generate the broadband I/Q signals.

In order to generate 4-bit phase shifts, the gain ratio of the two VGAs in the I/Q paths (A_j/A_r) are programmed in certain discrete settings such as 0/3, 1/3, 2/2, 3/1, or 3/0, in this way the phase shift can vary between 0° to 90° in a step of approximately 22.5°. By changing the polarity of A_r and A_j independently, a phase control range of 360° can be achieved, which can be done by swapping the positive and negative paths in the differential circuits of the two VGAs. Note that the gain ratio settings of A_j/A_r are set to 1/3 or 3/1 in order to achieve phase shift of 22.5 or 67.5°, since these ratio settings are simpler to be implemented as compared to the exact gain ratios of 1/2.4 or 2.4/1 for these phase shifts. The resulted gain and phase errors in the phase shifter due to these simplified gain ratio settings are well acceptable. As compared to an ideal 4-bit phase shifter, this phase shifter achieves a peak-to-peak gain variation of less than ±0.5 dB and a peak-to-peak phase error of less than 4° across different phase settings in simulation, when used in combination with ideal I/Q signals. The phase shifter can be extended to achieve higher phase resolution, for example, 5 bits, by programming A_j/A_r in more discrete settings.

As shown in Fig. 3(a), the 90° transmission line is implemented using a differential coplanar transmission line in a ground-signal-ground-signal-ground (GSGSG) configuration. The signal lines are using the top metal layer (metal-7). The ground lines are using the top metal layer (metal-7) that are connected to the bottom metal layer (metal-1) through vias, and form a solid ground plane using the bottom metal layer (metal-1) underneath the signal lines. The width and spacing of the signal lines and ground lines are all 4 μm at the top metal layer (metal-7). This transmission line has a measured differential impedance $Z_{\text{diff}} = 100 \ \Omega$, a relative dielectric
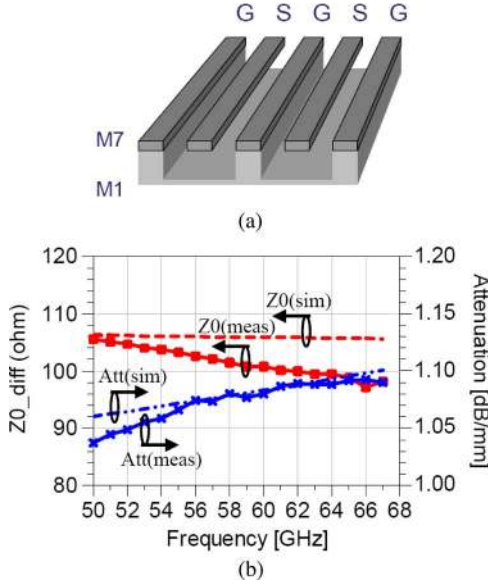
Fig. 3. (a) A differential coplanar (GSGSG) transmission line, in which the signal lines use the top metal layer (metal-7), and there is a solid ground plane using the bottom metal layer (metal-1) underneath the signal lines, and (b) its measurement results.

Fig. 4. Schematic of a 60 GHz 4-bit phase shifter in the receiver.

Each unit transistor: 5μm /0.06μm.

Fig. 5. Schematic of a VGA in the phase shifter of the receiver.

constant (ϵ_r) of 3.8, an attenuation of 1.08 dB/mm at 60 GHz which match the simulated results [Fig. 3(b)]. The difference between simulated and measured Z_{diff} is probably due to the accuracy of de-embedding, since there are open and short stubs used as test structures [31], whereas load and through structures are not available. The 90° transmission line has a width of 36 μm, a total length of 650 μm, and an insertion loss of 0.7 dB at 60 GHz.

B. Design of the Phase Shifter for the Receiver

Fig. 4 shows the schematic of the phase shifter for the receiver. The input transconductance stage, 90° line, and two digitally controlled VGAs are merged in a common-source cascode configuration for low power, high gain, and stability considerations. The input transconductance stage (M1–M4) converts the signal ($V_{\text{in}+}$ and $V_{\text{in}-}$) into separate currents. I/Q signals are generated by feeding these currents through two paths with and without a 90° transmission line, respectively. Two digitally controlled VGAs weigh these I/Q signals separately and generate the required phase at the combined output ($V_{\text{out}+}$ and $V_{\text{out}-}$). The shunt transmission line (L_p) cancels the impedance contributed by the input capacitance of the VGA at 60 GHz. The real part of the input impedance of each VGA (Z_{in}) is chosen to be equal to the characteristic impedance of the 90° transmission line (Z_0).

The VGAs in the phase shifter are implemented using a common-gate configuration as shown in Fig. 5. The gain is programmed by switching on or off a certain number of unit transistors, which are connected to $V_{\text{out}+}$, $V_{\text{out}-}$, or V_{dd}, respectively. The connections of these transistors are based on the digital control at their gates. In this way, the desired portion of the input currents of each VGA is diverted to the output, while the remaining portion is fed into the supply. For example, if 1/4 of the input current of the I-path VGA and 3/4 of the input
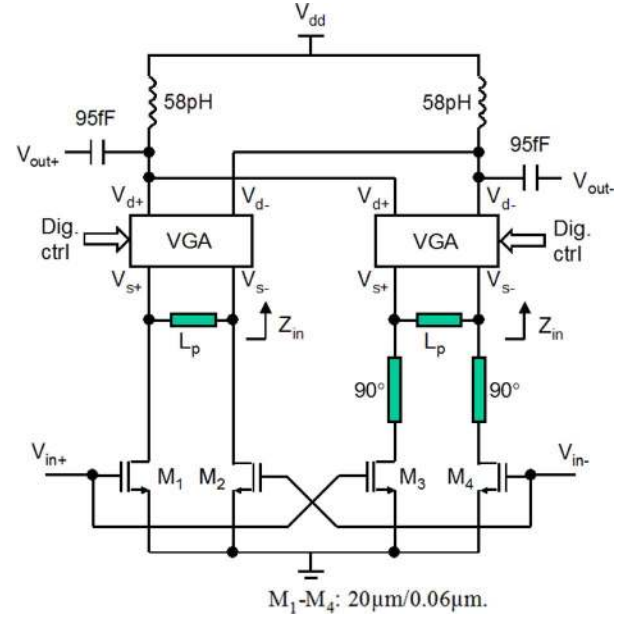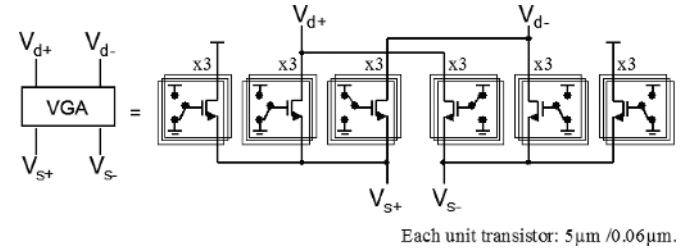
current of the Q-path VGA are diverted to the output, the gain ratio of the two VGAs (A_j/A_r) is 3/1, therefore the phase shift achieved is approximately 67.5°. By programming A_j/A_r to 0/3, 1/3, 2/2, 3/1, or 3/0 as well as changing the polarity of A_r and A_j, the phase shifter achieves a phase control range of 360° in steps of approximately 22.5°. This current steering approach provides a phase shift that is in the first order insensitive to the variations in technology, supply voltage, and temperature (PVT), since the phase shift is set by the gain ratio and therefore the number of unit transistors that connects to the output of the two VGAs. Moreover, by using the dummy transistors that connect to V_{dd}, the total number of unit transistors switched on is constant. In this way, the variations of the VGA input impedance are minimized, which provides the broadband load impedance required at the output of the 90° transmission line.

In simulation, the phase shifter in the receiver (Fig. 4) has an average insertion gain of 0 dB, an output referred 1dB-compression point (P_{1dB}) of −9 dBm at 60 GHz and consumes 19.5 mW.

C. Design of the LNA and Combiner for the Receiver

Thanks to the phase shifter with low loss, the requirements of the LNA are low noise figure, reasonable gain, and low power consumption. The two-stage differential LNA is shown in Fig. 6. The common-source cascode configuration offers low noise,
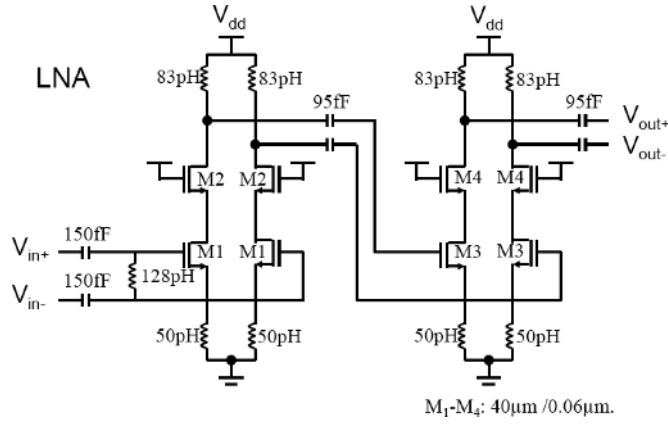
Fig. 6. Schematic of a 60 GHz LNA.
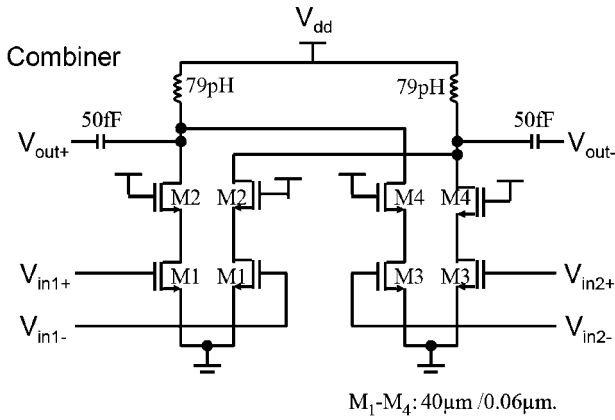
Fig. 7. Schematic of a 60 GHz combiner.

high gain and stability. The input of the receiver is matched to $100\,\Omega$ differential antennas [39]. There is inductive degeneration at the source of the input transistors to provide broadband power and noise matching. Measured results shows that a stand-alone LNA has a measured minimum noise figure of 5.5 dB and a power gain of 8.4 dB at 61 GHz [29]. The 3 dB bandwidth is 10.4 GHz. The LNA consumes 39 mW.

The combiner that follows the phase shifters is shown in Fig. 7. The RF signals from the two antenna paths are fed into two common-source cascode amplifiers. Subsequently, the signals are combined at the outputs of these amplifiers. The output of the combiner is matched to $100\,\Omega$ differentially for measurement purpose. The common-source cascode configuration provides isolation between the two paths. It achieves a simulated insertion gain of 4 dB (from V_{in1} or V_{in2} to V_{out}) at 60 GHz and consumes 19.5 mW. This implementation of power combiner has a higher gain than the use of a passive power combiner (such as a Wilkinson power combiner [26]). It is worth pointing out that by connecting more amplifiers in parallel, this combining method can be scaled to more paths. However, for a large number of paths, the output impedance of the combiner may be reduced significantly. Therefore, it becomes difficult to drive the load impedance of the combiner (i.e., the input impedance of the mixer). The loading problem can be solved by using multiple combiner stages in a tree

structure to combine a large number of paths while maintaining sufficient output impedance [24].

The spiral inductors in this work use the top two metal layers (metal-7 and metal-6) as signal paths and the bottom metal layer (metal-1) as a patterned ground shield, and are implemented using single-turn differential inductors with center tap. Simulations using the LSIM 3.1 tool [40] shows that the quality factors of the inductors are higher than 20 at 60 GHz. The capacitors are implemented using the intermediate metal layers stacking from metal-2 to metal-5, with minimum-spacing interdigitated fingers fringe capacitor configuration. In the simulation these capacitors have quality factors of around 10 at 60 GHz.

To achieve optimal noise figure and power gain, the finger width of the MOS transistors is chosen to be $1\,\mu m$ and the DC current density is approximately 0.15 mA per μm-gate-width. Wideband matching networks are adopted in order to provide broadband performance with low sensitivity to modeling inaccuracies and process variations. Extensive parasitic extractions have been performed on the layouts and taken into account during the circuit simulation. Long on-chip interconnect lines are implemented as transmission lines. The supply voltage in the receiver path is 1.5 V in order to provide voltage headroom in the cascode topologies. Since the gates of the cascode transistors are all connected to 1.5 V, within the 1 dB compression point the voltage swings at the inductive loads are less than the threshold voltage (V_{TH}) of the transistors. The cascode structures help to reduce the voltage stress on each transistor well below the specified breakdown voltage.

D. Design of the Phase Shifter for the Transmitter

The phase shifter in the transmitter has high linearity requirement, so that it is the output stage of the power amplifier rather than the phase shifter that saturates first, otherwise the overall efficiency of the transmitter is decreased.

The schematic of the phase shifter in the transmitter is depicted in Fig. 8. Its operating principle is similar to that in the receiver (Fig. 4). The RF signal (V_{in+} and V_{in-}) is converted into separate currents by a transconductance stage (M1–M4). I and Q signals are generated by feeding these currents through two paths with or without a 90° line, and weighted by the digitally controlled VGAs separately. The required phase is generated at the combined output (V_{out+} and V_{out-}). As compared to the implementation in the receiver that merges the transconductance stage and the VGAs in a common-source cascode configuration, the phase shifter in the transmitter cascades the transconductance stage and the VGAs in two separate stages, in order to achieve a larger voltage swing and higher output P_{1dB}. Furthermore, there is inductive degeneration at the source of the input transconductance stage in order to provide input impedance matching ($100\,\Omega$ differentially) for measurement purposes. The VGAs that are used in the phase shifter are shown in Fig. 9. They are similar to those in the receiver (Fig. 5) that program the gain by switching on or off a certain number of unit transistors. The only difference between the VGAs in the receiver and in the transmitter lies in the DC bias voltage at the gate of the transistors in order to work properly: in Fig. 9 the gate bias of each transistor is either V_b

Fig. 8.   Schematic of a 60 GHz 4-bit phase shifter in the transmitter.

Fig. 9.   Schematic of a VGA in the phase shifter of the transmitter.

(DC bias voltage, which is 0.7 V) or 0, instead of being either V_{dd} or 0 in Fig. 5.

In simulation the phase shifter in the transmitter (Fig. 8) achieves an average insertion gain of -6 dB, an output P_{1dB} of -2 dBm at 60 GHz and consumes 25 mA from a 1.2 V supply. It features a higher output P_{1dB} than that in the receiver. In this way the power amplifier instead of the phase shifter limits the linearity of the transmitter. The insertion gain of the phase shifter is lower than that in the receiver, mainly because of its inductive source degeneration that achieves input matching for measurement purposes.

E. Design of the PA for the Transmitter

Thanks to the phased array system that can increase the effective isotropic radiated power (EIRP) of a transmitter by spatial power combining, the output power of an individual power amplifier is less critical.

A power amplifier is often designed using a common-source or common-source cascode configuration. In a common-source configuration, the Miller capacitance (C_{gd}) reduces the gain, reverse isolation and stability. Therefore, the common-source topology is conditionally stable, which is prone to instability because of the limited accuracy in the transistor model and in the matching network at this high frequency. A common-source cascode structure improves the devices stability but has the disadvantage of reduced voltage headroom and drain efficiency. In this work, the Miller capacitance of a common-source configuration is compensated using neutralization capacitors cross-connected between the drains and gates of the pseudo-differential transistors. As compared to a common-source cascode

configuration, this common-source configuration provides a large output swing. The neutralization capacitors in this work use MOS transistors with the gate as one capacitor terminal and the drain and source connected together as the other capacitor terminal. By properly sizing the MOS transistors, these MOS-transistor-based neutralization capacitors match the Miller capacitors of the common-source amplifiers and are less sensitive to the variations in PVT. In this way, the Miller effect is compensated and stability is ensured. This is an advantage compared to neutralization by the use of fixed parallel-plate metal capacitors as in [41].

Fig. 10 shows the three-stage power amplifier in this work. The output of the power amplifier connects to $100\,\Omega$ differential antennas [39], and the output matching network of the power amplifier is designed through large-signal load-pull simulation to achieve large output power and high power efficiency. The inductors at the drains and gates of the transistors connect to the supply voltage (V_{dd}) and bias voltage V_b, respectively. These inductors, together with the series fringe capacitors and the shunt transmission line $(300\,\mu m$ at the output), form the input, output, and inter-stage matching networks. The total gate width of the transistors in each stage of the power amplifier doubles progressively, which ensures that the output stage saturates first if each stage has at least 3 dB power gain. To achieve an optimal power gain performance, the gate finger width of the MOS transistors is chosen to be $1\,\mu m$ with gate contacts at both sides and the DC current density is approximately 0.2 mA per μm-gate-width. In simulation the power amplifier achieves an insertion gain of 15 dB and a maximum output power (P_{max}) of $+11$ dBm at 60 GHz.

M1: 40μm/0.06μm, M2: 80μm/0.06μm, M3: 160μm/0.06μm.
Cc1: 18μm/0.06μm, Cc2: 36μm/0.06μm, Cc3: 160μm/0.06μm using NMOS transistors..
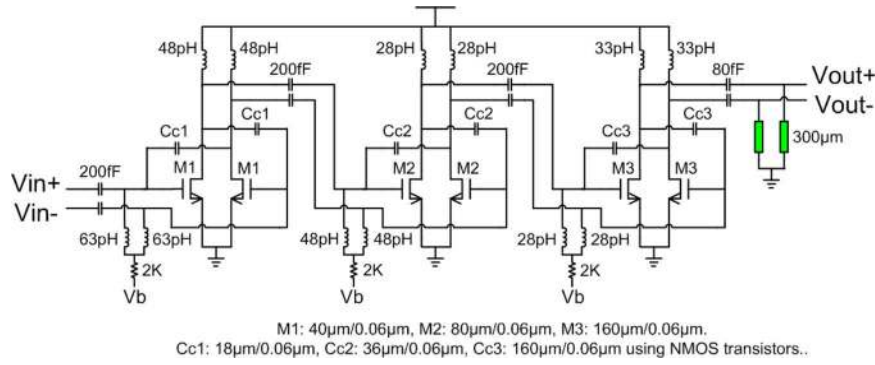
Fig. 10. Schematic of a 60 GHz three-stage power amplifier.
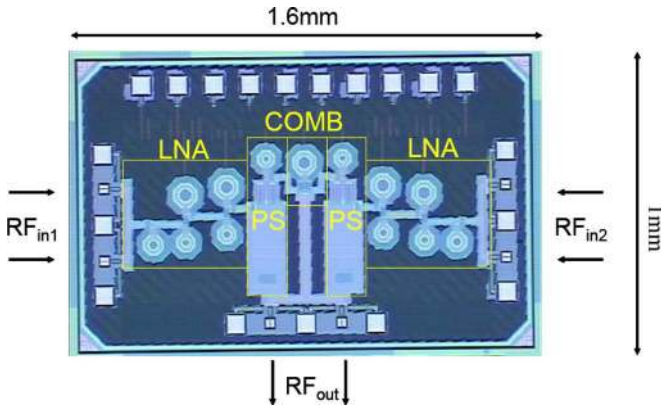

Fig. 11. Chip photo of a two-path 60 GHz receiver in which each path consists of an LNA, a phase shifter, and part of a combiner.
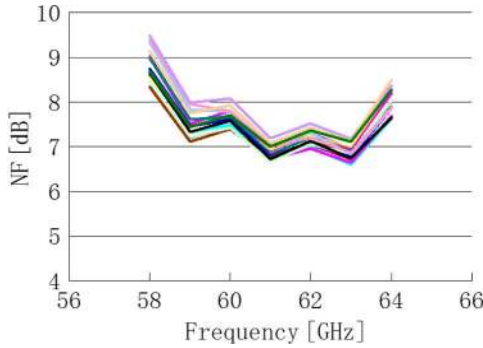

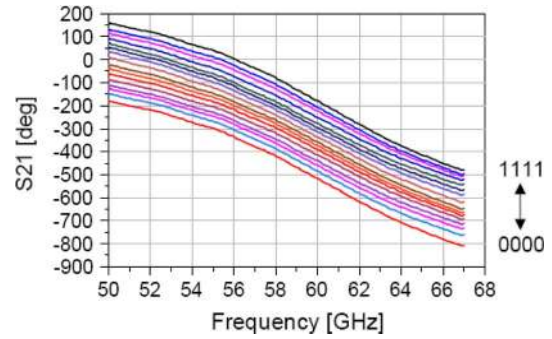Fig. 12. Measured noise figure of one receiver path for 16 phase settings.

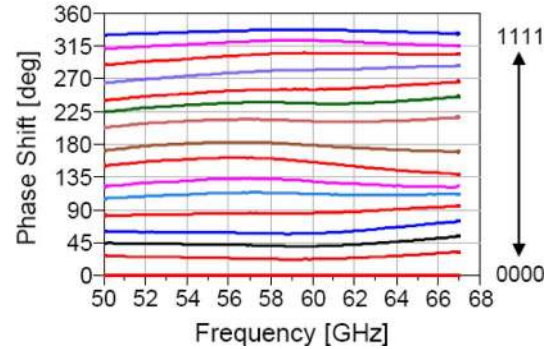Fig. 13. Measured insertion phase of one receiver path for 16 phase settings.

Fig. 14. Measured relative phase shift of one receiver path for 16 phase settings.
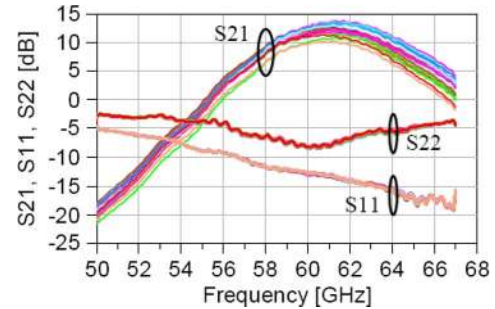

Fig. 15. Measured insertion gain, input and output matching of one receiver path for 16 phase settings.

III. MEASURED RESULTS AND DISCUSSIONS

A. Measurements of the Receiver Path

As shown in Fig. 1(a), a two-path 60 GHz receiver is implemented in a 65 nm CMOS technology, in which each path consists of an LNA, a 4-bit RF phase shifter, and part of a combiner (a common-source cascode amplifier). Each phase shifter is controlled independently using digital inputs that are loaded to the phase shifter by a serial peripheral interface (SPI). Fig. 11 shows the die photo. The die area is 1.6 mm^2 and the active circuit occupies 0.9 mm^2. The layout is symmetrical between the two receiver paths.

Each receiver path consumes 52 mA from a 1.5 V supply, in which the LNA, phase shifter, and part of a combiner consumes 26 mA, 13 mA, and 13 mA, respectively.

Fig. 12 shows the measured noise figure of one receiver path for 16 digitally controlled phase settings. The noise figure is
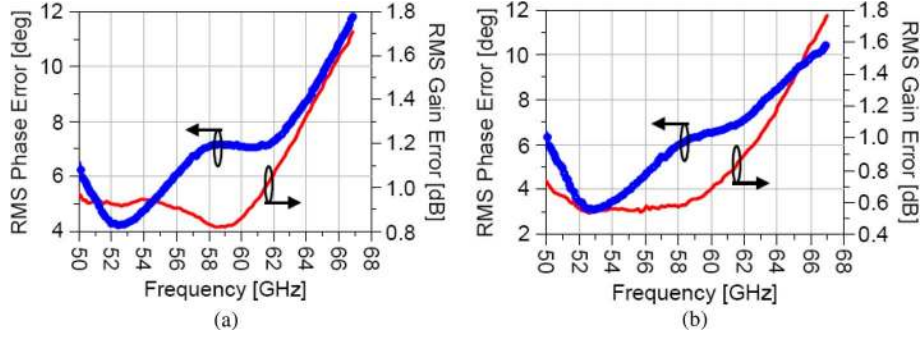
Fig. 16.   Measured RMS gain and phase errors: (a) of the 16 phase states and (b) of the I and Q signals in the receiver as compared to an ideal 4-bit phase shifter.

between 6.7 to 7.2 dB across all phase settings at 61 GHz, which is mainly contributed by the LNA with a measured noise figure of 5.5 dB.

The measured insertion phase [phase(S21)] of one receiver path for 16 phase settings is depicted in Fig. 13. The phase step is approximately 22.5° (4-bit resolution) and the phase control range is 360° in the 60 GHz band.

Fig. 14 highlights the relative phase shifts of one receiver path for 16 phase settings by setting the phase state 0000 as a reference. This shows that the 4-bit phase shifts achieved are relatively constant over a wide frequency range, which is due to the broadband I/Q signal generation and the frequency insensitive gain ratio of the two VGAs that weigh these I/Q signals.

Fig. 15 presents the measured insertion gain (S21), input and output return loss (S11 and S22) of one receiver path for 16 phase settings. At the center frequency of 61 GHz, the average insertion gain is 12 dB, and the peak-to-peak gain variation is 3.4 dB across all phase settings. The 3 dB bandwidth is 5.5 GHz. This insertion gain is contributed separately by the LNA that has measured gain of 8.6 dB, the part of the combiner that has a simulated gain of 4 dB, and the phase shifter that has a simulated average gain of 0 dB. The measured S11 and S22 of one receiver path for 16 phase settings are −13 dB and −8 dB, respectively, at 61 GHz, which are determined by the input matching of the LNA and the output matching of the combiner separately and do not change for different phase settings.

Derived from the measured insertion gain and phase shifts, Fig. 16(a) shows the RMS gain and phase errors of the 16 phase states. They are 0.9 dB and 7° at 61 GHz, respectively, as compared to an ideal 4-bit phase shifter with a uniform gain. As highlighted in Fig. 16(b), the RMS gain and phase errors of the I/Q signals, which are measured indirectly using phase state 0°, 90°, 180°, and 270°, are 0.8 dB and 6.8°, respectively, at 61 GHz. These frequency dependent gain and phase errors are contributed by the 90° transmission line, the impedance mismatch between the input of each VGA (Z_{in}) and the transmission line (Z_0), as well as the layout mismatch in the pseudo-differential paths.

Fig. 17 shows the measured nonlinearity of one receiver path. The power gain and output power are plotted as a function of the RF input power at 61 GHz. The measured input referred P_{1dB} of one receiver path is observed to be −16 dBm at 61 GHz. This P_{1dB} is limited by the input transconductance stages of
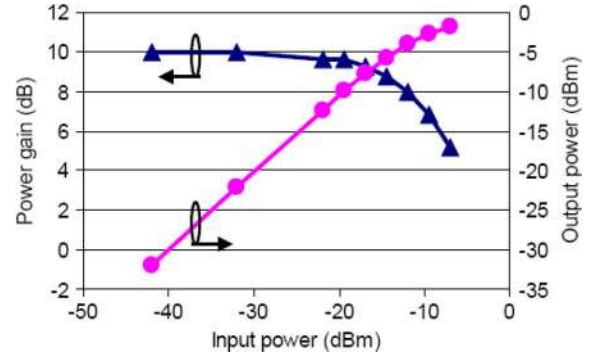

Fig. 17.   Measured power gain and output power of one receiver path at 61 GHz versus the RF input power.

the phase shifter and can be improved by, i.e., using source degeneration at the cost of reduced gain and/or increased power consumption.

The measured isolation between the two input ports of the receiver is −43 dB, thanks to the pseudo-differential cascode topologies with differential inductors used in the LNA, phase shifter and combiner.

The mismatches of the two receiver paths are measured through two-port S-parameter measurements in either of the two paths over different phase settings. By comparing the S-parameters of the two paths for the same phase settings, the insertion gain and phase mismatches of the two paths are quantified as RMS gain mismatch and RMS phase mismatch [26]. The measured RMS gain and phase mismatch of the two paths are 0.4 dB and 2.1°, respectively, at 61 GHz. Since the layout of the two receiver paths are symmetrical to each other, these mismatch results are mainly due to the measurement inaccuracies brought by probe placement and cable stability when measuring one of the two paths at a time.

Table I summarizes the measured performance of the receiver path in comparison with reported prior work of mm-wave RF-path phase shifting receivers.

B. Measurements of the Transmitter Path

Consisting of a 4-bit digitally controlled RF phase shifter and a power amplifier, a 60 GHz transmitter path is implemented in a 65 nm CMOS technology [Fig. 1(b)]. Expansion of one path to multiple antenna paths can be straightforward, in which the RF

TABLE I
BENCHMARK OF mm-WAVE RF-PATH PHASE SHIFTING RECEIVERS

Specifications	[26]	[36]	[34]	[25]	This work
Frequency (GHz)	12	77	60	60	61
Phase shifting @	RF	RF	RF	RF	RF
Number of paths	8	1	1	4	2
Key building blocks	LNA + phase shifter + combiner	LNA + phase shifter	phase shifter	LNA + phase shifter + combiner	LNA + phase shifter + combiner
Power Gain of each path (dB)	24.5	≤ 17	-2	≥ 8	12 (average)
Phase shift step (°)	Digital, 22.5	Analog (+DAC)	Analog (+DAC)	Analog	Digital, 22.5
NF of each path (dB)	4.2	4 (LNA only)	17	≤ 6.9	≤ 7.2
Input P_{1dB} of each path (dBm)	-33	-	-7	-33.5	-16
Power consumption (mW)	660 (8 paths)	128 (1 path)	32 (1 path)	265 (4 paths)	156 (2 paths)
Technology	0.18μm SiGe Bi-CMOS	0.13μm SiGe Bi-CMOS	0.13μm SiGe Bi-CMOS	0.12μm SiGe Bi-CMOS	65nm CMOS
Chip area (mm²)	5.39	0.46	1.48	4.6	1.6

signal from a shared frequency up-converter can be split, phase shifted, amplified and fed into the multiple antennas. Fig. 18 shows the chip photo. The chip area is 1.3 mm × 1.3 mm and the active area is only 0.8 mm × 0.4 mm. The transmitter path draws 140 mA from a 1.2 V supply, in which the phase shifter and PA draws 25 mA and 115 mA, respectively.

The measured insertion phase [phase(S21)] of one transmitter path for 16 digitally controlled phase settings is depicted in Fig. 19. It achieves a phase step of approximately 22.5° and a phase control range of 360° in the 60 GHz band.

Fig. 20 shows the measured insertion gain (S21), input and output reflection coefficients (S11 and S22) of one transmitter path for 16 phase settings. It has an average insertion gain of 7.7 dB at 62 GHz and a 3 dB bandwidth of 6.5 GHz, which

match the simulated S21 of phase state 0000. This insertion gain is contributed separately by the phase shifter that has a simulated insertion gain of −6 dB, and the power amplifier that has a simulated gain of 15 dB. The measured S11 and S22 are all better than −8 dB at 62 GHz, which are determined by the input matching of the phase shifter and the output matching of the power amplifier, respectively, and do not change for different phase settings. Besides, the measured reversed isolation (S12) of the transmitter path is −44 dB.

Based on the measured insertion gain and phase shifts, the RMS gain and phase errors of one transmitter path are shown in Fig. 21. They are 1.2 dB and 9.2° at 62 GHz, respectively, as compared to an ideal 4-bit phase shifter with a uniform gain. The phase accuracy meets the 4-bit requirement.

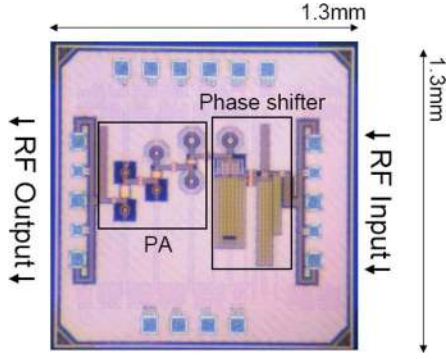Fig. 18.   Chip photo of a 60 GHz transmitter path that combines a phase shifter and a PA.
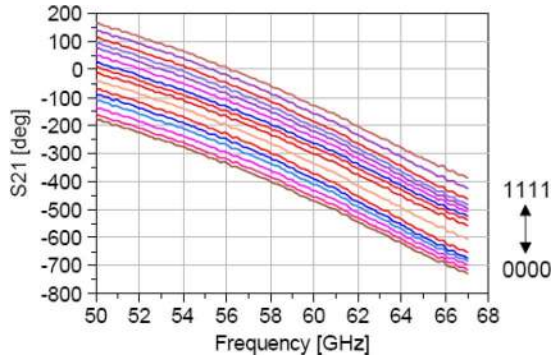

Fig. 20.   Measured insertion gain, input and output matching of one transmitter path for 16 phase settings.

Fig. 19.   Measured insertion phase of one transmitter path for 16 phase settings.

Fig. 21.   Measured RMS gain and phase errors of the 16 phase states in the transmitter as compared to an ideal 4-bit phase shifter.

Fig. 22 presents the measured nonlinearity of one transmitter path and compares to the simulated result. The measured output P_{1dB} is +4 dBm at 62 GHz. The measured maximum output power (P_{max}) of one transmitter path is observed to be higher than +8.3 dBm (limited by the test equipment) with a corresponding power-added efficiency (PAE) of 2.4%. Considering that the phase shifter has a simulated loss of 6 dB and consumes 30 mW, the power amplifier has a corresponding gain of approximately 10 dB and a PAE of 4.4% when transmitting this output power. The power gain, output power and efficiency of the power amplifier can be further improved using a transformer coupled input, interstage and output matching network [41], [42], as the insertion loss of the matching network can be reduced without the use of lossy passive components including spiral inductors, fringe capacitors, and long interstage interconnects.

Table II summarizes the measured performance of the transmitter path in comparison with previously published works. Although the comparison is not totally fair in the sense that we describe a single channel, it is still useful.

Fig. 22.   Measured power gain and output power of one transmitter path at 62 GHz versus the RF input power.

IV. CONCLUSION

In this work we have presented a 60 GHz phase shifter integrated with LNA and PA in 65 nm CMOS for phased array systems. The operation of the 4-bit RF phase shifter is based on programmable weighted combinations of I/Q paths using digitally controlled VGAs. T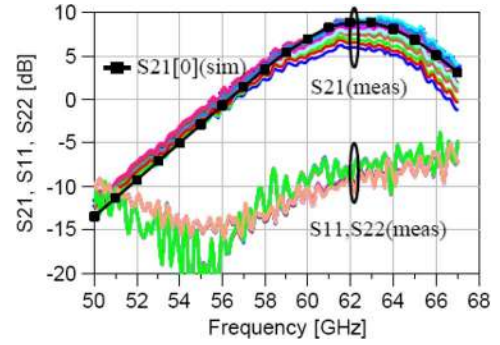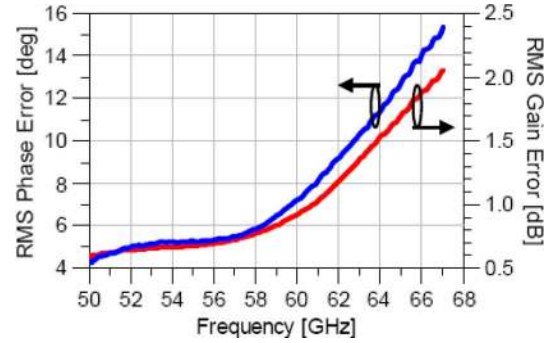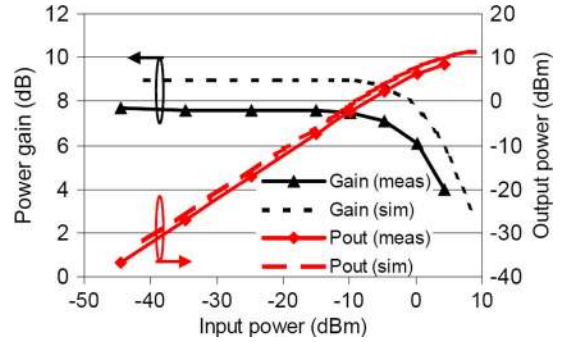he RF phase shifter achieves a 360° phase shift range in approximately 22.5° steps for both the 60 GHz receiver and transmitter. Consisting of an LNA, a phase shifter, and part of a combiner, each receiver path achieves 7.2 dB noise figure and an average insertion gain of 12 dB at 61 GHz. With the combination of a phase shifter and a PA, one transmitter path achieves a maximum output power of higher than +8.3 dBm and an average insertion gain of 7.7 dB at 62 GHz. This work has demonstrated that RF phase shifting is an appealing technique for 60 GHz phased arrays: it achieves sufficient phase resolution (4-bit), large phase range (360°), full integration in CMOS, low supply voltage, and low power consumption, consumes small chip area, and possesses further scalability towards larger phased arrays without modification of the existing frequency converter and LO distribution network.

TABLE II
BENCHMARK OF mm-WAVE PHASED ARRAY TRANSMITTERS

Specifications	[18]	[27]	[28]	[20]	This work
Frequency (GHz)	77	42.5	60	60	62
Phase shifting @	LO	RF	RF	LO	RF
Number of paths	4	16	16	4	1
Key building blocks	PA + mixer + VCO + phase shifter + frequency divider, etc.	PA + phase shifter + signal divider, etc.	PA + phase shifter + mixer + RF power distribution + frequency synthesizer, etc.	PA + mixer + phase shifter + LO tripler, etc.	PA + phase shifter
Power Gain of each path (dB)	40.6 (@baseband)	12.5	35 (max @baseband)	20 (@baseband)	7.7 (average)
Max. output power of each path (dBm)	+12.5	-2.5	+9 ($P_{out\backslash dB}$)	+11	$\geq$ +8.3
Phase shift step (°)	Analog	Digital, 22.5	Digital, 11.25	Analog	Digital, 22.5
Supply voltage (V)	2.5&1.5	5&3.3	2.6	1	1.2
Power consumption (mW)	1828 (4 paths)	3600 (16 paths)	3800 (16 paths)	590 (4 paths)	168 (1 path)
Technology	0.12μm SiGe Bi-CMOS	0.18μm SiGe Bi-CMOS	0.12μm SiGe Bi-CMOS	65nm CMOS	65nm CMOS
Chip area (mm²)	17	8.3	43.9	4.1	1.7

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