A 60-GHz Sub-Sampling Frequency Synthesizer Using Sub-Harmonic Injection-Locked Quadrature Oscillators

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***Abstract* — This paper presents a 60-GHz sub-harmonic injection-locked quadrature frequency synthesizer with sub-sampling operation. This allows the proposed synthesizer to achieve relatively lower in-band phase noise through the use of sub-sampling operation, as well as good out-of-band phase noise through the use of sub-harmonic injection. The proposed synthesizer has been implemented in a standard 65-nm CMOS technology. It can support all 60-GHz channels and achieves a phase noise of -115dBc/Hz at 10MHz offset. The sub-sampling operation helps reducing an integrated jitter from 12ps to 2.1ps. It consumes 20.2mW and 14mW from a 20GHz sub-sampling phase-locked loop (SS-PLL) and a quadrature injection-locked oscillator (QILO), respectively.**

***Index Terms* — millimeter-wave, CMOS, PLL, sub-sampling, in-band, low-phase-noise, low-power, injection-locking, sub-harmonic, 60GHz, synthesizer, channel bonding.**

I. Introduction

Due to an unlicensed 9-GHz bandwidth, 60GHz has potentials to cope up with an increasing demand for multi-gigabit-per-second data rates. To be able to inter-operate among various 60GHz wireless standards, *i.e.,* IEEE802.11ad/WiGig, IEEE802.15.3c, wirelessHD, ECMA-387 and ISO/IEC13156, 60GHz frequency synthesizers should be able to generate standard four channels, *i.e.,* 58.32GHz, 60.48GHz, 62.64GHz, 64.8GHz, as well as those in between, *i.e.*, 59.4GHz, 61.56GHz, 63.72GHz for channel bonding capability [1]. Moreover, in order to cope with different symbol rates specified in above standards, an integer-N PLL should support dual reference clocks, *e.g.*, 36MHz and 40MHz. The design of 60GHz frequency synthesizer plays an important role in the 60GHz transceiver system [2]-[3] including both RF and baseband ends as shown in Fig.1. The out-of-band phase noise of the RF local oscillator (LO) sets the limit on achievable modulation scheme and data rate, *i.e.*, 16QAM requires -90dBc/Hz at 1MHz offset. Moreover, the in-band phase noise has to be improved depending on the loop bandwidth of baseband carrier-and-timing recovery loop [2].

Among previously reported 60GHz PLLs [1]-[8], sub-harmonic injection-locked technique using 20GHz PLL and 60GHz QILO relaxes the requirements for tuning range and deterioration of quality factor of LC-tank at mm-wave frequency. As a result, it achieves the lowest out-of-band phase noise for all specified frequency channels [1]. However, due to the use of 36MHz/40MHz reference clocks (REF), the mm-wave charge-pump-based integer-N PLL in [1] suffers from poor in-band phase noise performance as the charge pump (CP) and phase/frequency detector (PFD) noise is multiplied by the square of a high division ratio *N* [9].

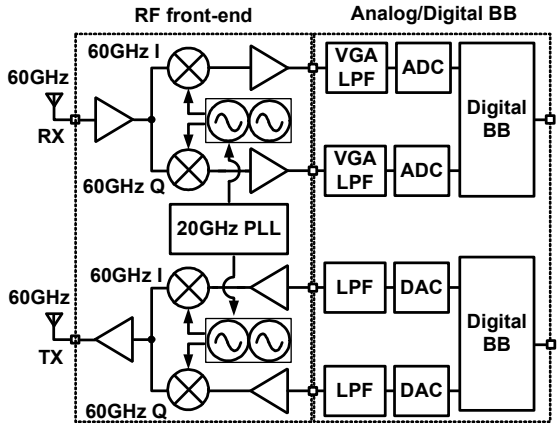


Fig.1. Block diagram of the 60GHz transceiver system [2]

In this paper, a 60-GHz sub-harmonic injection-locked quadrature frequency synthesizer using sub-sampling operation in the 20GHz PLL is proposed to suppress an in-band phase noise and also meet the requirements to inter-operate over various 60-GHz standards. Moreover, design optimization and considerations are applied in the design of a 20GHz class-C VCO, 20GHz buffer, and a high-division-ratio injection locked frequency divider (ILFD), which significantly lower the power consumption and area comparing to [1],[8] making it suitable for portable devices. This paper is organized as follows. Section II presents the proposed architecture. The following section describes circuit implementations. Section IV describes experimental results. Finally, a conclusion is in section V.

II. Design of the Proposed Architecture

60-GHz sub-harmonic injection-locked PLLs can achieve relatively lower out-of-band phase noise [4]-[8].

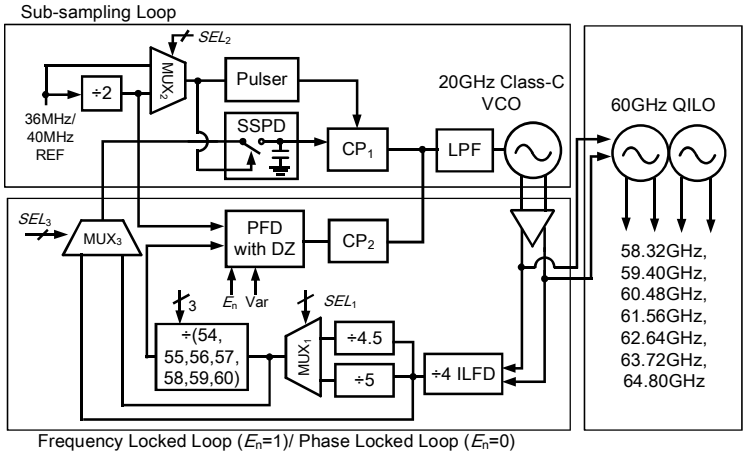


Fig.2. Proposed architecture for 60GHz sub-harmonic injection-locked sub-sampling quadrature frequency synthesizer.

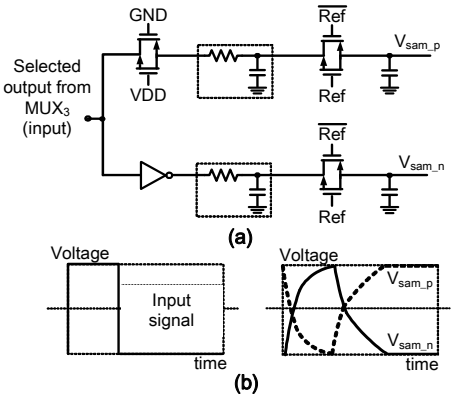


Fig.3.(a) Schematic of the wave shaper with sampling switches and (b) waveforms of digital input and sampled outputs.

However, for mm-wave PLLs, a large division ratio N is required to down-convert the VCO output for phase comparison with the reference clock. This puts a challenge to achieve low in-band phase noise in mm-wave PLLs with 36 or 40MHz reference clocks [1] as the noise of PD and CP multiplied by the square of high value of N. This is because the PLL in-band phase noise contributed by PFD/CP can be approximated as $L_{\text{in-band}} \approx (S_{\text{i,n}} \cdot N^2)/(2 \cdot K_D^2)$ [9], where $S_{\text{i,n}}$ is power spectral density of PD/CP current noise, N is a division ratio in a PLL and K_D is the CP gain. To reduce the in-band phase noise, an approach in [9] has eliminated the N factor by directly subsampling the VCO output by reference clock and by-passing all the frequency dividers. In the proposed sub-sampling operation for a mm-wave integer-N PLL, high-divide-ratio digital dividers have been omitted in the feedback path to reduce in-band phase noise while being compatible with 36MHz and 40MHz reference clocks to generate required 4 channels and support channel bonding. The proposed synthesizer includes a sub-harmonic 20GHz sub-sampling PLL (SS-PLL) and a 60GHz QILO as shown in Fig.2. The 20GHz PLL can perform both classical PFD/CP mode (E_n=0) and sub-sampling mode (E_n=1).

For a PFD/CP mode, E_n is set to 0. The sub-sampling loop is disabled as CP_1 is off and PFD in lower loop works without any dead zone. A divide-by-2 divider is placed after reference clock to support channel bonding but at an expense of lower reference clock. "SEL_1" bit of MUX_1 can control corresponding division ratio of input 36/40MHz reference clocks.

In sub-sampling mode, E_n is set to 1, a dead zone of PFD is created. PFD controls CP_2 until the signal is close to lock. Then, the SSPD samples the selected divider output from MUX_3 with the selected reference clock from MUX_2 and convert phase error into voltage variation. Current output from CP_1 controls VCO in the locked state with significantly less N ratio. An amount of a division ratio to be by-passed in the sub-sampling feedback path, *e.g.*, a factor of 60 or 300, can be selected by MUX_3 to alleviate in-band phase noise. The sub-sampling mode bypasses a minimum of divide-by-60 ratio and an in-band suppression in the feedback loop is calculated to be approximately 15dB when sampled by the divided reference clock.

III. Circuit Descriptions

This section describes building blocks of the proposed 60GHz frequency synthesizer, *i.e.*, operation of SSPD, design optimizations for the VCO, buffer, and prescaler for a low-power 20GHz PLL, and a 60GHz QILO.

A. Sub-sampling Phase Detector (SSPD)

As shown in Fig. 3(a), if the output from MUX_3 is chosen from MUX_1, it is fed to a transmission gate and an inverter to create a differential signal. If it is taken from the ILFD output, differential signals can directly pass to wave shaper which is composed of an RC circuit to shape rectangular waveforms into more triangular waveforms in Fig. 3(b). This helps the sub-sampling loop stays locked more robustly. Positive and negative sampled outputs control current of CP_1 until the frequency is locked.

B. Design Optimization of 20-GHz VCO, buffer and ILFD

Critical building blocks that consume most of power consumption in mm-wave PLLs are VCO and prescaler dividers [1],[8]. In this work, a low bias is applied at gates of NMOS cross-coupled pair of 20GHz LC-VCO shown in Fig.4 (a) to operate transistors in class-C operation resulting to higher DC-RF current conversion efficiency

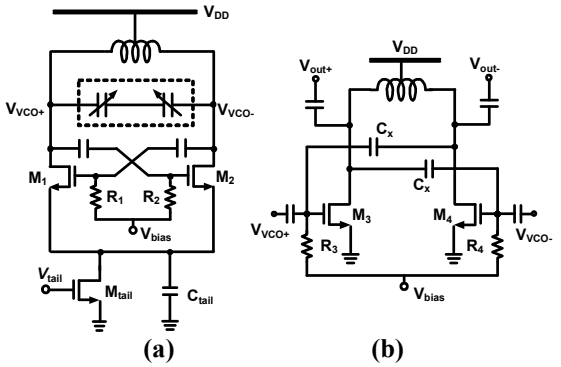


Fig.4. Schematic of (a) a low-power 20-GHz Class-C VCO and (b) a 20-GHz capacitive-cross-coupled buffer.

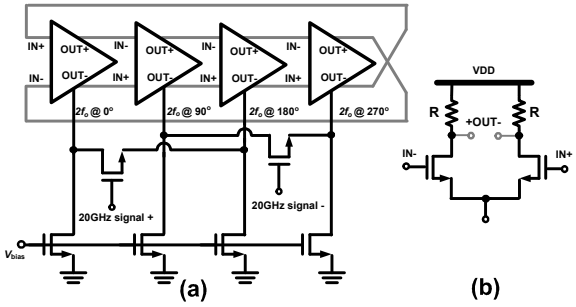


Fig.5. Schematic of (a) 20-GHz divide-by-4 ILFD using even-harmonic direct injection with its (b) delay cell.

which results to 36% power saving comparing to class-B LC-VCO [10]. The frequency can be tuned by a varactor and a 4-bit capacitor array. In Fig.4.(b), capacitive cross-coupled C_x are used in 20-GHz buffer to help cancel undesired parasitic gate-to-drain capacitances which improves reverse isolation [2]. To avoid power-consuming divide-by-2 CML dividers in cascade, a single-stage divide-by-4 ILFD is employed using dual-step-mixing technique [11]. As a result, it can obtain wide locking range and low-power operation as shown in Fig. 5.

C.60-GHz Quadrature Injection Locked Oscillator (QILO)

The schematic of 60GHz QILO [2] is shown in Fig.6. Two LC tanks are coupled to generate quadrature signals. The frequency can be adjusted by coarse and fine tuning.

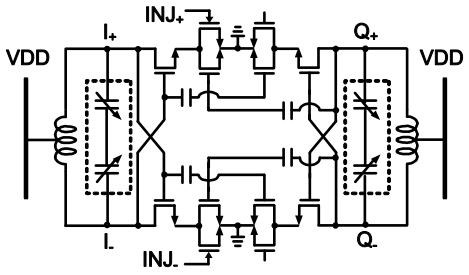
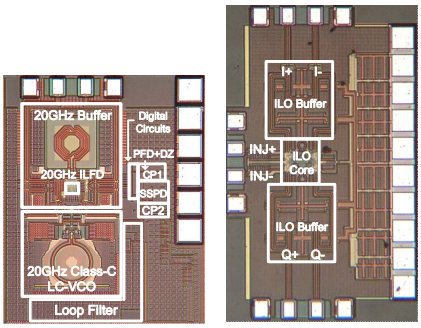


Fig.6. Schematic of a 60-GHz QILO.



(a) (b)

Fig.7. Chip micrographs (a) 20GHz SS-PLL(b) 60GHz QILO

IV. Experimental Results

The proposed 60GHz frequency synthesizer is implemented in a standard 65nm CMOS process. The microphotographs of both chips are shown in Fig.7 in which the 20GHz SS-PLL and QILO occupy an area of 700μm×800μm and 1000μm×600μm including PADs, respectively. The measurement is performed on two probe stations with cables and an external buffer to compensate for cable loss. The phase noise is evaluated using an Agilent E5052B signal source analyzer (SSA) and a 50-to-75 GHz external mixer. The 60GHz QILO consumes an average power of 14mW from 1.2V supply. It can generate free-running frequencies from 58.3-65.4GHz.

To validate the design of the proposed 20GHz SS-PLL, we utilize an output taken from MUX_1 with half reference clock so that the synthesizer can support all required frequency channels using 36MHz or 40MHz REF clocks. Fig.8. shows the measured phase noise characteristics of 20GHz SS-PLL at carrier frequency of 20.88GHz, 60GHz QILO locked to 20GHz PFD/CP PLL, and 60GHz QILO locked to 20GHz SS-PLL both at a carrier frequency of 62.64GHz. In the sub-sampling mode, the out-of-band phase noise of 60GHz QILO locked to 20GHz SS-PLL is maintained at -115dBc/Hz at 10MHz offset, where its in-band phase noise shows a 15dB reduction at 100 kHz offset comparing to the case where 60GHz QILO locked to conventional 20GHz PFD/CP PLL. The reference spur in the sub-sampling mode is measured to be -38dBc at 64.8GHz. The calibrated output power of 20GHz PLL is approximately -4 dBm. The power consumption of the 20GHz SS-PLL is 20.2mW from 10.6mW of the 20GHz VCO and its buffer, 4.8mW of the ILFD and 4.8mW of digital circuits from 1.2V supply. This is about 3 times power reduction compared to [1],[8].

Table I summarizes the comparison of the proposed work with the state-of-the-art 60GHz PLLs. Sub-harmonic injection method shows the lowest out-of-band phase noise at 10MHz offset comparing to [4]-[7]. However, due to the use of relatively lower REF clock, the work in [1],

TABLE I: PERFORMANCE COMPARISON WITH THE-STATE-OF-THE-ART 60GHZ PLLS

Ref.	Reference Freq. (MHz)	Frequency (GHz)	Integrated Jitter (ps)	Phase Noise @10kHz offset	Phase Noise @10MHz offset	Features	Power (mW)
[4]	234	58.0-60.4	3.2	-50 dBc/Hz	-100 dBc/Hz	Direct 60GHz Diff. PLL	80
[5]	135	57.9-68.3	0.24	-80 dBc/Hz	-108 dBc/Hz	Direct 60GHz QPLL	25
[6]	100	56.0-62.0	0.94	-71 dBc/Hz	-109 dBc/Hz	60GHz AD-PLL	48
[7]	40	53.8-63.3	0.23	-89 dBc/Hz	-107 dBc/Hz	60GHz SS-QPLL	42
[1]	36	58.1-65.0	9.0	-40 dBc/Hz	-117 dBc/Hz	Sub-harmonic Injection 20GHz PLL + 60GHz QILO	72
This (PFD/CP)	36	58.3-65.4	12.0	-40 dBc/Hz	-115 dBc/Hz	Sub-harmonic Injection 20GHz PLL + 60GHz QILO	32.8
This (SS)	**36**	58.3-65.4	**2.1**	**-69** dBc/Hz	**-115** dBc/Hz	Sub-harmonic Injection **20GHz SS-PLL** + 60GHz QILO	**34.2**

as well as, PFD/CP mode of the proposed work have higher in-band phase noise [4]-[6],[10]. The sub-sampling loop of the proposed work successfully reduces the division ratio and suppresses the in-band phase noise to -69dBc at 10kHz offset. Moreover, sub-sampling operation reduces integrated jitter from 12ps to 2.1ps as it is integrated from 10kHz to 40MHz.

V. CONCLUSION

The proposed 60GHz frequency synthesizer using 20GHz SS-PLL and 60GHz QILO is presented. It achieves a suppression of in-band phase noise in sub-sampling mode and also achieves low out-of-band phase noise. It can support various 60GHz standards.

ACKNOWLEDGEMENT

This work was partially supported by MIC, SCOPE, MEXT, STARC, Canon Foundation, and VDEC in collaboration with Cadence Design Systems, Inc., and Agilent Tech. Japan, Ltd.

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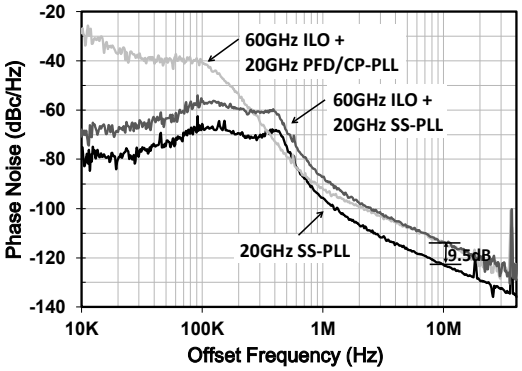

Fig.8. Measured phase noise plots at 62.64 GHz

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