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A 60 μW 60 nV/$\sqrt{}$Hz Readout Front-End for Portable Biopotential Acquisition Systems

Refet Firat Yazicioglu, Patrick Merken, Robert Puers, *Senior Member, IEEE*, and Chris Van Hoof

***Abstract*—There is a growing demand for low-power, small-size and ambulatory biopotential acquisition systems. A crucial and important block of this acquisition system is the analog readout front-end. We have implemented a low-power and low-noise readout front-end with configurable characteristics for Electroencephalogram (EEG), Electrocardiogram (ECG), and Electromyogram (EMG) signals. Key to its performance is the new AC-coupled chopped instrumentation amplifier (ACCIA), which uses a low power current feedback instrumentation amplifier (IA). Thus, while chopping filters the 1/f noise of CMOS transistors and increases the CMRR, AC coupling is capable of rejecting differential electrode offset (DEO) up to $\pm$50 mV from conventional Ag/AgCl electrodes. The ACCIA achieves 120 dB CMRR and 57 nV/$\sqrt{}$Hz input-referred voltage noise density, while consuming 11.1 μA from a 3 V supply. The chopping spike filter (CSF) stage filters the chopping spikes generated by the input chopper of ACCIA and the digitally controllable variable gain stage is used to set the gain and the bandwidth of the front-end. The front-end is implemented in a 0.5 μm CMOS process. Total current consumption is 20 μA from 3V.**

***Index Terms*—AC coupling, analog integrated circuits, biopotential amplifier, chopper modulation, electroencephalography, electrocardiography, electromyography, electrode offset, instrumentation amplifier.**

I. Introduction

ELECTROENCEPHALOGRAM (EEG), Electrocardiogram (ECG), and Electromyogram (EMG) waves are common biopotential signals that are recorded routinely in modern clinical practice. Commonly, patients are connected to a bulky and mains-powered instrument, which reduces their mobility and creates discomfort. This limits the acquisition time, prevents the continuous monitoring of patients, and affects the diagnosis of the illness. Therefore, there is a growing demand for low-power, small-size, and ambulatory biopotential acquisition systems [1]–[3]. The ultimate goal is to implement a biopotential acquisition system that is comfortable and invisible to eye with long-term power autonomy, high signal quality, and configurability for different biopotential signals. The aim is not only to increase the patients' quality of life but also to extend device applications to sports, entertainment, comfort monitoring, and so on.

A crucial and power consuming building block of the biopotential acquisition system is the readout front-end, which defines the quality of the extracted signals. However, long-term power autonomy dictates the need for low-power circuitry, putting strict design constraints on the readout front-end circuit. Fig. 1 shows the characteristics of the EEG, ECG, and EMG signals [4]. Due to the low frequency and μV level amplitude of these signals, in-band noise of the readout is dominated by 1/f noise. Moreover, common-mode interference from the mains correlate the biopotential signals [5], and there is the problem of electrode offset generated at the skin-electrode interface [4]. Therefore, in order to achieve signal extraction under these circumstances a front-end is needed with high CMRR, low-noise, and high-pass filter (HPF) characteristics. Moreover, amplitude and bandwidth characteristics of biopotential signals vary for EEG, ECG, and EMG signals and different applications of these signals. Therefore, front-end should have configurable gain and filter characteristics.

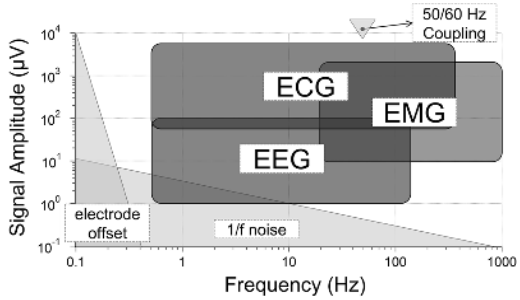

Fig. 1. Frequency and amplitude characteristics of biopotential signals, EEG, ECG, and EMG, and contaminating signals of the biopotential signals (not to scale).

This work [6] describes a low-noise and low-power readout front-end with configurable characteristics for different biopotential signals. Section II gives an overview of the building blocks of the front-end and presents the state of the art. Section III describes the AC-coupled chopping technique and presents the current feedback instrumentation amplifier (IA) that is used in the AC-coupled chopped instrumentation amplifier (ACCIA). Section IV describes the chopping spike filter stage that filters the chopping spikes generated due to the input chopper of the ACCIA. Section V presents the gain stage of the front-end. Section VI presents the test results of the ASIC and compares its performance with literature. Finally, Section VII states the conclusions of this work.

II. Readout Front-End Architecture Overview

Fig. 2 shows the architecture of the implemented readout front-end for the acquisition of EEG, ECG, and EMG signals. The readout channel of the system consists of the ACCIA, a chopping spike filter (CSF) stage, a digitally programmable gain

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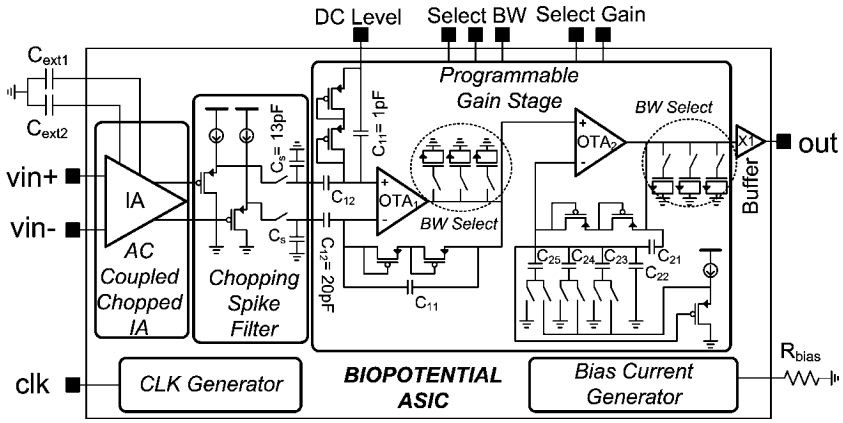

Fig. 2. Architecture of the biopotential readout front-end for the acquisition of EEG, ECG, and EMG signals.

stage and an output buffer. In addition, ASIC includes a bias current generator and a clock generator operating from a single external clock of 128 kHz, and generating the 4 kHz chopping clock for the ACCIA and 8 kHz track and hold (T&H) signal with selectable duty cycle for the CSF stage.

The most important and power consuming building block of the front-end is the IA. It defines the noise performance and the CMRR of the front-end, and filters the differential electrode offset (DEO). A standard IA architecture is the three-opamp IA [7]–[11]. However, the CMRR of the three-opamp IA depends on the matching of the resistors [12] and the need for low output impedance amplifiers results in excessive power dissipation. A second technique for implementing IAs is using switched-capacitor (SC) circuits [13], [14]. However, the main drawback of the SC amplifiers is the fold-over of noise above Nyquist frequency [15]. Thus, neither three-opamp IA nor SC IA is convenient for low-power and low-noise front-ends.

Another IA topology is called current feedback (current balancing) IA [16]–[21]. The gain of the IA is defined by the ratio of two resistors and the CMRR does not rely on the matching of the resistors. Additionally, there is no need for low output impedance amplifiers. However, the high number of parallel branches and the need for operational amplifiers increases the power dissipation of the IAs of [16]–[21]. Therefore, there is a need for a current feedback IA with minimized number of parallel branches.

Although implementation of such an IA can reduce the power dissipation, 1/f noise and process induced mismatches of the transistors will limit the power reduction and reduce the CMRR of the IA, respectively. A frequently used technique for filtering the 1/f noise and increasing the CMRR is chopping [15]. However, chopping amplifiers are inherently DC coupled systems. Two implementations of the AC coupling technique for chopping IAs use either external passive HPFs before the input of the IA [22], or use a differential difference amplifier (DDA) [23]. However, the low input impedance of the former design considerably degrades the signal-to-noise ratio, where as the latter consumes excessive power due to the resistive feedback amplifier topology. Therefore, a new AC coupling technique for chopping amplifiers is necessary.

In this work, an AC coupling technique for chopping amplifiers is proposed and applied to a new low-power current feedback IA. Thus, while AC coupling filters the DEO, chopping improves the CMRR and filters the 1/f noise of the current feedback IA. However, a common problem of the chopping amplifiers is the chopping spikes generated at the output due to the input chopper [15], where high frequency chopping spike components can fold-over into baseband and correlate the signal, if a sampling ADC is used after the front-end. Therefore, a CSF stage follows the ACCIA.

A digitally programmable gain stage with selectable gain and bandwidth is used to adjust the gain and bandwidth of the readout for different biopotential signals. Conventional gain stages use either SC or resistive feedback topologies, where former has the aliasing problem and latter consumes excessive power. The variable gain stage of this work operates in continuous-time mode and gain is defined by the ratio of two capacitors. Thus, while achieving low power dissipation, it can also perform the operation of an anti-aliasing filter.

III. AC Coupled Chopped Instrumentation Amplifier

A. AC Coupled Chopped Instrumentation Amplifier (ACCIA)

Fig. 3 shows the concept of the AC-coupled chopping technique. Operation of the ACCIA can be described as follows: DC input voltage, which is the DEO $(V_{\mathrm{offset,elec}})$ in our case, is modulated by the input chopper and copied to the terminals of R_1. This voltage creates a current through R_1, which is copied to R_2 and defines the output voltage after demodulation by the output chopper. A transconductance stage, GM, with transconductance gm and low-pass cut-off frequency, f_p, filters the DC component of the output and converts it into current. A chopper modulates the output current of the GM since DEO current through R_1 is modulated by the input chopper. At steady-state, the current supplied by GM equals $V_{\mathrm{offset,elec}}/\mathrm{R}_1$. Therefore, no current is supplied by the IA and the current passing through R_2 is zero so the output is zero. The transfer function of the topology can be

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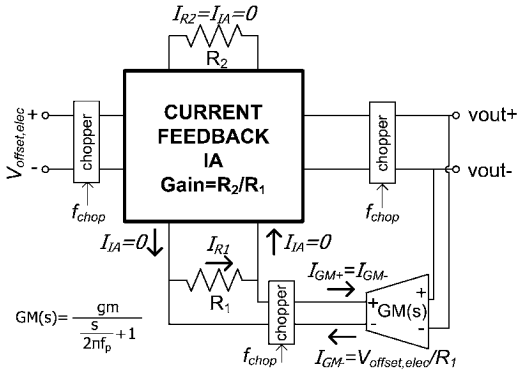

Fig. 3. Concept of the AC-coupled chopped instrumentation amplifier (ACCIA).

written as (1), assuming that low-pass cut-off frequency of the IA, $f_{LP,IA}$ is much larger than $f_{\rm chop}$, and $gm\mathrm{R}_2 \gg 1$.

$$\frac{V_{\rm out}}{V_{\rm in}}(s) = \frac{\mathrm{R}_2}{\mathrm{R}_1}\frac{s+2\pi f_p}{s+gm\mathrm{R}_2(2\pi f_p)} \tag{1}$$

On the other hand, the noise of the IA is only modulated by the output chopper. Therefore, the output noise power spectral density (PSD) of ACCIA, $\mathrm{S}_{\rm ACCIA}$, can be expressed in terms of the output noise PSD of the IA, $\mathrm{S}_{\rm IA}$, as

$$\begin{aligned} S_{\rm ACCIA}(f) &= \left(\frac{2}{\pi}\right)^2 \sum_{\substack{n=-\infty \\ n=\text{odd}}}^{+\infty} \frac{1}{n^2} S_{\rm IA}(f - nf_{\rm chop}) \\ &\cong S_{\rm IA,white}(f). \end{aligned} \tag{2}$$

If $f_{\rm LP,IA} \gg f_{\rm chop}$ and the 1/f noise corner frequency of the current feedback IA is smaller than $f_{\rm chop}/2$, $\mathrm{S}_{\rm ACCIA}$ equals the white noise component of $\mathrm{S}_{\rm IA}$, $\mathrm{S}_{\rm IA,white}$ [15]. As a result, while 1/f noise of the current feedback IA is eliminated by chopping, the electrode offset is filtered by the feedback loop implemented by GM.

Fig. 4 shows the implementation of the concept presented in Fig. 3. The GM is implemented by the $\mathrm{OTA}_2 - C_{\rm ext2}$ filter and the transconductance stage, gm_2. This results in an equivalent transconductance of $\mathrm{A_v}\ gm_2$, where $\mathrm{A_v}$ is the voltage gain of OTA_2. This ensures the condition $gm\mathrm{R}_2 \gg 1$ for the implementation of the characteristics presented in (1). Therefore, by replacing gm of (1) with $\mathrm{A_v}gm_2$ and f_p with $gm_{\rm OTA2}/(\mathrm{A_v C_{ext2}})$, high-pass cut-off frequency of the ACCIA, $f_{\rm HP,ACCIA}$, can be found from (1) as

$$f_{\rm HP,ACCIA} = (1/2\pi)\mathrm{R}_2 gm_2(gm_{\rm OTA_2}/\mathrm{C_{ext2}}). \tag{3}$$

OTA_2 is implemented as a current mirror OTA, Fig. 5(a), where $gm_{\rm OTA2}$ is reduced using a series-parallel division of current [24]. This results in $gm_{\rm OTA2}$ of 1 μS. The gm_2 stage is implemented as a basic differential stage, Fig. 5(b), which acts as a voltage-to-current converter. The output of gm_2 is mirrored to the terminals of R_1 through CM_1 and CM_2 in order to supply the current on R_1 generated by the DEO. In addition to the feedback loop that filters the DEO, another feedback loop is implemented by $\mathrm{OTA}_1 - \mathrm{C_{ext1}}$ and gm_1 in order to filter the IA offset. Input of $\mathrm{OTA}_1 - \mathrm{C_{ext1}}$ is connected to the output of the current feedback IA. Since at this node, DEO is modulated by the input chopper, $\mathrm{OTA}_1 - \mathrm{C_{ext1}}$ only filters the IA offset. At steady state, the current supplied by gm_1 equals $V_{\rm offset,IA}/\mathrm{R}_1$. Similar to gm_2, the output of gm_1 is mirrored to the terminals of R_1 in order to cancel the IA offset. Therefore, the combination of the two feedback loops cancels both the DEO and the IA offset.

B. Current Feedback Instrumentation Amplifier

Fig. 4 also shows the simplified schematic of the proposed current feedback IA. It has only four parallel branches and there is no need for opamps, thus power dissipation can be low. Current of I_1 is shared by the current sources I_2 and I_3. The voltage gain of the circuit can be calculated from the low-frequency small-signal analysis of the half-circuit [25], Fig. 6, and can be expressed as in (4). $\mathrm{R}_{\rm out,eq}$ equals to $\mathrm{R}_{\rm ds1}//\mathrm{R}_{\rm out2}$, and $gm_{\rm M1}$ and $gm_{\rm M2}$ are the transconductance of transistors M_1 and M_2, respectively. During the derivation of (4), it has been assumed that $\mathrm{R}_{\rm ds1}$ and $\mathrm{R}_{\rm ds2}$, are much larger than R_1 and R_2.

$$\frac{V_{\rm out,half}}{V_{\rm in,half}} = -\frac{\mathrm{R}_2}{\mathrm{R}_1}\frac{1}{1+(\alpha\mathrm{R}_2/\mathrm{R}_{\rm out,eq})} \tag{4}$$

$$\alpha = (1+1/gm_{M1}\mathrm{R}_1)(1+1/gm_{M2}\mathrm{R}_2) \tag{5}$$

If $\alpha\mathrm{R}_2 \ll \mathrm{R}_{\rm out,eq}$, then the differential voltage gain of the IA can be expressed as the ratio of two resistors, (6). The low-pass cut-off frequency of the IA, (7), can be found by replacing $\mathrm{R}_{\rm out,eq}$ with $\mathrm{R}_{\rm out,eq}//(1/\mathrm{sC_c})$, where $\mathrm{C_c}$ is shown in Fig. 4.

$$A_v = (V_{{\rm out},p} - V_{{\rm out},n})/(V_{{\rm in},p} - V_{{\rm in},n}) = \mathrm{R}_2/\mathrm{R}_1 \tag{6}$$

$$f_{\rm LP,IA} \cong (1/2\pi)(1/\alpha\mathrm{R}_2\mathrm{C}_c) \tag{7}$$

Therefore, both the gain and the low-pass cut-off frequency of the circuit can be set by selecting R_1, R_2, and designing the transconductance's of M_1 and M_2.

Since we are interested in minimizing the power dissipation of the circuit, the main limiting factor is the noise of the circuit. Analysis of the simplified schematic of the IA in Fig. 4 reveals that the input-referred noise power density of the current feedback IA can be given by

$$\begin{aligned} \overline{v_{\rm in,IA}^2} = 2\overline{v_{M_1}^2} + \overline{v_{R1}^2} + \frac{1}{A_v^2}\left(\overline{v_{R2}^2} + 2\overline{v_{M_2}^2}\right) + 2\frac{gm_{I1}^2}{g_1^2}\overline{v_{I_1}^2} \\ +2\frac{gm_{I2}^2}{(g_1//gm_1)^2}\overline{v_{I_2}^2} + 2\frac{gm_{I3}^2}{g_1^2}\overline{v_{I_3}^2} \end{aligned} \tag{8}$$

where gm_{I1}, gm_{I2}, and gm_{I3} are the transconductance of the current sources, and $g_1 = 1/\mathrm{R}_1$ and $g_2 = 1/\mathrm{R}_2$. Adding the noise contributions of gm stages, gm_1 and gm_2, and of transistors CM_1 and CM_2 of Fig. 4 to (8) gives the input-referred noise power density of ACCIA, (9). Only thermal noise of CMOS transistors is considered due to the chopping process. It has been also assumed that $\mathrm{A_v} \gg 1$ and transconductance of CM_1 and CM_2 are equal to gm_{I1}.

$$\begin{aligned} \overline{v_{\rm in,ACCIA}^2} = \frac{16kT}{3}\left[\frac{1}{gm_{M1}} + \frac{3}{4\,g_1}\right. \\ \left. + \frac{(2gm_{I_1} + gm_{I_3} + gm_1 + gm_2)}{g_1^2} + \frac{gm_{I2}}{(g_1//gm_{M1})^2}\right]. \end{aligned} \tag{9}$$

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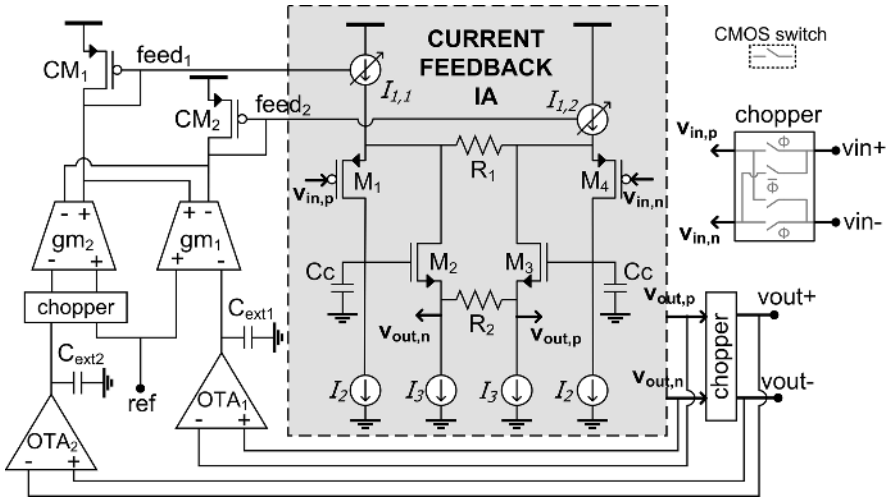
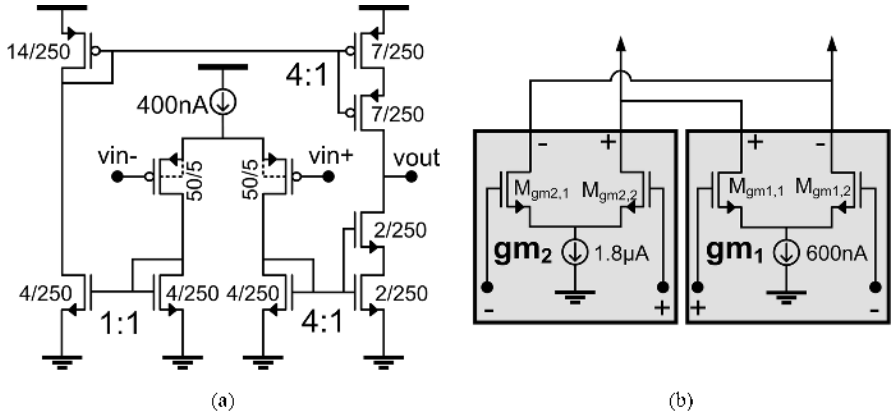


Fig. 4. ACCIA implementation that can eliminate the 1/f noise, while filtering the DEO and the IA offset. Simplified schematic of the current feedback IA is also shown. $\mathrm{C_{ext1}}$ and $\mathrm{C_{ext2}}$ are off-chip capacitors.



(a) (b)

Fig. 5. (a) Schematic of the OTA that is used to implement $\mathrm{OTA_1}$-$\mathrm{C_{ext1}}$ and $\mathrm{OTA_2}$ -$\mathrm{C_{ext2}}$ low-pass filters of Fig. 4. (b) Schematic of gm_1 and gm_2 of Fig. 4.

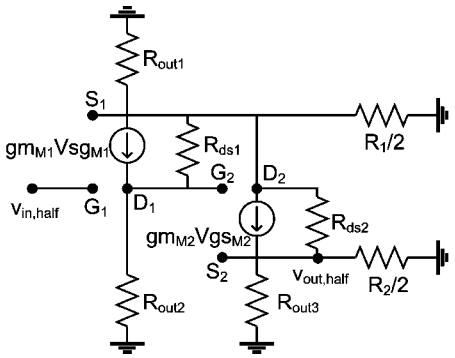


Fig. 6. Low-frequency small-signal model of the half-circuit of the simplified current feedback IA of Fig. 4.

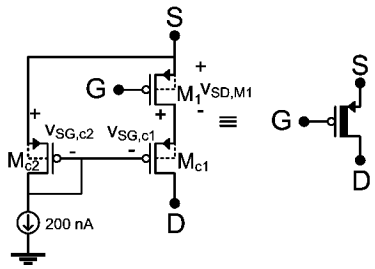


Fig. 7. Schematic of the input stage of the current feedback IA. $\mathrm{M_{c1}}$ and $\mathrm{M_{c2}}$ set the source-to-drain voltage of $\mathrm{M_1}$ independent of the input DC level.

Equation (9) states that in order to decrease the noise of the ACCIA, $\mathrm{R_1}$ must be minimized. Therefore, if an AC coupling technique similar to [26] is used, where AC coupling is achieved using capacitors and pseudo resistors before the input of the amplifier, then noise contributions of the current sources can be minimized by decreasing $\mathrm{R_1}$. However, this type of AC coupling technique results in low CMRR for high performance biopotential acquisition systems (e.g., 86 dB for [26]) due to the process related mismatches. Alternatively, we have selected g_1 close to gm_{M1} and operate the input pair transistors in weak inversion, and current source transistors in strong inversion, in order to minimize the noise of our circuit. Therefore, (9) can be reduced to (10), which gives the theoretical minimum noise assuming that g_1 and gm_{M1} is much larger than g_{I1}, g_{I2}, g_{I3}, gm_1, and gm_2. Similar analysis as in [26] gives a theoretical minimum NEF [19] of 4.7 for the presented ACCIA architecture (It has been assumed that the current through $\mathrm{M_1}$ is 1/6 of the supply current). However, in practice minimum noise level is limited by the input–output voltage swing constraints.

$$\overline{v_{\mathrm{in}}^2} = (1 + 3/4)16kT/3gm_{M1}. \tag{10}$$

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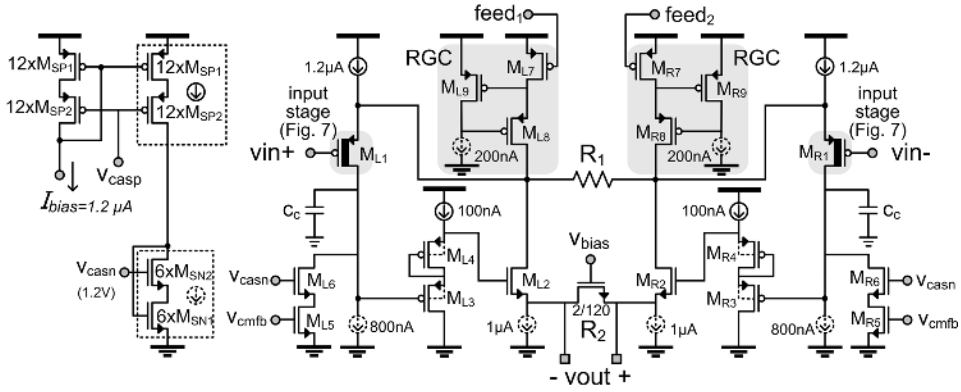

Fig. 8. Complete schematic of the current feedback IA that is used in the ACCIA implementation.

Another important point is the CMRR of the IA and effect of DEO on the CMRR [27]. Chopping cannot prevent the DEO induced CMRR reduction since the DEO is also modulated by the input chopper. Electrode offset dependent CMRR [27] of the IA can be written as

$$\frac{1}{\mathrm{CMRR_{TOTAL}}} = \frac{1}{\mathrm{CMRR_{SYS}}} + \frac{1}{\mathrm{CMRR_{\Delta gds,input}}} + \frac{1}{\mathrm{CMRR_{\Delta gds,source}}}. \quad (11)$$

where $\mathrm{CMRR_{SYS}}$, $\mathrm{CMRR_{\Delta gds,input}}$, and $\mathrm{CMRR_{\Delta gds,source}}$ are the systematic CMRR, CMRR with drain-to-source conductance (g_{ds}) mismatch of input pair transistors, and CMRR with g_{ds} mismatch of current sources $I_{1,1}$ and $I_{1,2}$.

Since current sources $I_{1,1}$ and $I_{1,2}$ are used to cancel the DEO current, their DC operating points are not matched leading to output transconductance mismatch. Therefore, regulated cascode current mirrors (RGC) [28] are used in order to minimize the output transconductance mismatch of $I_{1,1}$ and $I_{1,2}$, which increases $\mathrm{CMRR_{\Delta gds,source}}$.

On the other hand, an input stage is proposed in order to increase $\mathrm{CMRR_{\Delta gds,input}}$ and replaces the input transistors, $\mathrm{M_1}$ and $\mathrm{M_4}$, of Fig. 4. Fig. 7 shows the schematic of the input stage. Current through $\mathrm{M_1}$, $\mathrm{M_{c1}}$, and $\mathrm{M_{c2}}$ are fixed due to the structure of the circuit of Fig. 4, thus their gate-to-source voltages (V_{SG}) are constant. Hence, source voltage of $\mathrm{M_1}$ is copied to the drain of $\mathrm{M_1}$, where its DC level is shifted by the difference between the gate-to-source voltages of $\mathrm{M_{c2}}$ and $\mathrm{M_{c1}}$ ($V_{\mathrm{SG,C2}} - V_{\mathrm{SG,c1}}$). Therefore, source-to-drain voltage of $\mathrm{M_1}$, $V_{\mathrm{SD,M1}}$, is fixed and defined by

$$V_{\mathrm{SD,M1}} = V_{\mathrm{SG,c2}} - V_{\mathrm{SG,c1}} \quad (12)$$

As a result, $\mathrm{CMRR_{\Delta gds,input}}$ is increased due to the immunity of drain-to-source voltage to the input DC level. On the other hand, drain-to-source resistance of the final structure equals to a classical cascode stage, ensuring the condition, α $\mathrm{R_2} \ll \mathrm{R_{out,eq}}$, for (6).

Fig. 8 shows the complete schematic of the implemented current feedback IA. All the current sources are implemented by paralleling the unit cascode current source, $\mathrm{M_{SN1}}$, $\mathrm{M_{SN2}}$ for nMOS current sources and $\mathrm{M_{SP1}}$, $\mathrm{M_{SP2}}$ for pMOS current sources. Current sources $I_{1,1}$ and $I_{1,2}$ are implemented by combining a fixed current source and a RGC current mirror. Thus, current through $\mathrm{M_1}$ can be increased, while transconductance of the gm stages of Fig. 5(b) can be low to decrease its contribution to the noise of the IA. $\mathrm{R_2}$ is implemented with a nMOS transistor so that the gain of the IA can be continuously adjusted. The common-mode feedback circuit is implemented using two differential pairs as in [29], and the common-mode level is set via transistors $\mathrm{M_{R5}}$ and $\mathrm{M_{L5}}$. The source follower stages, which consist of transistors $\mathrm{M_{R3}}$, $\mathrm{M_{R4}}$ and $\mathrm{M_{L3}}$, $\mathrm{M_{L4}}$, act as level shifters in order to maximize the input–output voltage swing of the IA.

IV. Chopping Spike Filter (CSF)

A well-known problem of the chopping circuits is the chopping spikes at the output generated due charge injection from the input chopping switches. Different techniques have been proposed in order to filter these chopping spikes. Reference [30] uses a bandpass filter between the input and the output choppers. However, matching of the bandpass filter center frequency with the chopping frequency limits the efficiency of this technique. Another technique uses nested choppers in order to modulate the output chopping spikes [31]. However, biopotential signals have very high bandwidth for this technique (1 kHz for EMG signals).

Fig. 9 shows the implemented CSF stage. Before the appearance of the chopping spike, output is sampled to the capacitor and during the presence of a chopping spike, switch S is opened and output is held on the capacitor. An important consideration during the design of the CSF is the effect of T&H operation on the output noise of the IA. The noise transfer function of a T&H stage is given in [32]. Therefore, the output noise of the CSF stage can be written as

$$\overline{v_{\mathrm{out,SF}}^2(f)} = \overline{v_{\mathrm{out,ACCIA}}^2(f)} \times \left\{ \left[\frac{2BW_n m^2}{f_{\mathrm{clk}}} \mathrm{sinc}^2\left(\frac{\pi m f}{f_{\mathrm{clk}}}\right) \right] + \left[(1-m)^2 \left(1 + 2 \sum_{n=1}^{BW_n/f_{clk}} \mathrm{sinc}^2\left(\pi n (1-m)\right) \right) \right] \right\} \quad (13)$$

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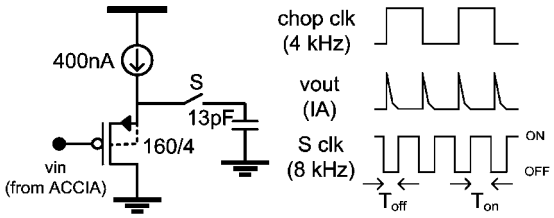

Fig. 9. Schematic of the chopping spike filter stage and the operation principle.

where $f_{\rm clk}$ is the operating frequency of CSF stage, $\rm BW_{\it n}$ is the noise bandwidth of the input, m is the duty cycle of the hold time $(T_{\rm off}/T_{\rm period})$. First and second terms represent the noise contributions of hold and track operations, respectively. If m is small, then the output PSD of CSF stage is very close to the input PSD. In this design, m is digitally selectable between 6.25% and 12.5%. Ratio of the input and the output noise PSD at $f = 0$ is $\sim$1.0 and $\sim$1.1 for m equal to 6.25% and 12.5%, respectively. Moreover, since the operating frequency of the T&H operation is twice the chopping frequency, there will be no aliasing of the 1/f noise into baseband, which is modulated to odd harmonics of the chopping frequency by the output chopper of the ACCIA.

V. Programmable Gain Stage

The programmable gain stage of the design includes a fixed gain stage, which is implemented as proposed in [26] with a gain of 20 and also acts as a differential-to-single end converter, and a continuous-time variable gain amplifier (VGA) stage with digitally controllable gain. Fig. 10 shows the schematic of the implemented continuous-time VGA. Pseudo-resistors of [26] are used in order to set the DC level at the inverting node of the OTA. A current-mirror OTA is used as shown in Fig. 5(a). The transfer function of the VGA can be written as

$$A_V(s) = \left\{1 + \frac{\rm C_{\it T}}{\rm C_1}\left[\left(s + \frac{1}{\rm C_{\it T}R_{par}}\right)\Big/\left(s + \frac{1}{\rm C_1R_{eq}}\right)\right]\right\} \cdot 1 \Big/ \left[s\left(\frac{\rm C_{\it T}}{\rm C_1}\frac{\rm C_{\it L}}{\it gm_{OTA}}\right) + 1\right] \quad (14)$$

where $\rm C_{\it T}$ is the total equivalent capacitance of the variable capacitor bank, $\rm R_{eq}$ is the equivalent resistance of the pseudo resistors, $\rm C_L$ is the total load capacitance, $gm_{\rm OTA}$ is the transconductance of the OTA, and $\rm R_{par}$ is the any parasitic resistance between node A and ground. The feedback loop implemented by the source follower prevents any parasitic resistance at node A. Therefore, DC gain of the stage can be set to unity and in-band gain can be defined by the ratio of $\rm C_{\it T}$ and $\rm C_1$. $\rm C_{\it T}$ can be set through the switches of the capacitor bank. If a capacitor is connected to ground, it increases $\rm C_{\it T}$, else its effective value is canceled by the source follower stage. Moreover, low-pass cut-off frequency of the gain stage can be set through the variable load capacitance. The gain of the VGA can be selected to be 2, 4, 8, or 13, setting the total gain of the gain stage to 40, 80, 160, or 260, respectively.

TABLE I
Operating Point of Transistors in Fig. 8 and Fig. 5(b)

Transistors	W/L (µm/µm)	$\rm I_D$ (µA)	gm/$\rm I_D$ (1/V)
M_{R1}, M_{L1}	1120/7	1.2	22.6
M_{RC1}, M_{LC1}	112/4	1.2	19.3
M_{RC2}, M_{RL2}	16/128	0.2	5.9
M_{R2}, M_{L2}	40/5	1.0	19.5
M_{R3}, M_{L3}, M_{R4}, M_{L4}	50/4	0.1	22.6
M_{R5}, M_{L5}	8/75	0.4	7.5
M_{R6}, M_{L6}	8/2	0.4	20.2
M_{R7}, M_{L7}, CM_1, CM_2	24/20	1.2	7.5
M_{R8}, M_{L8}	100/2	1.2	21
M_{R9}, M_{L9}	80/2	0.2	23.4
M_{SP1}	2/20	0.1	7.4
M_{SP2}	5/2	0.1	19.9
M_{SN1}	4/75	0.2	7.5
M_{SN2}	4/2	0.2	20.1
$M_{gm1,1}$, $M_{gm1,2}$	2.5/80	0.3	4.85
$M_{gm2,1}$, $M_{gm2,2}$	7.5/80	0.9	4.78

VI. Test Results and Discussions

We have fabricated the presented readout front-end in the AMIS 0.5 μm three-metal two-poly CMOS process. Fig. 11 shows the die micrograph. Core area measures less than 2 mm^2. Table I lists the operating point of each transistor in the current feedback IA of Fig. 8 and in the gm stages of Fig. 5(b). Current source transistors of the current feedback IA are operated barely in strong inversion in order to increase the input–output voltage swing. Transistor sizes are large in order to decrease the corner frequency of the 1/f noise below half the chopping frequency. Maximum allowed DEO is defined by the maximum differential current that can be supplied by gm_2 stage of Fig. 5(b) and $\rm R_1$. We have selected $\rm R_1$ as 50 kΩ, thus ACCIA can filter a maximum electrode offset of $\pm$50 mV. This limit has been set based on our DEO measurements from Ag/AgCl electrodes, Fig. 12, and considering the non-polarizable characteristics of Ag/AgCl electrodes [4] and low input DC current (presented in the next section) of the ACCIA. Maximum allowed DEO can be increased up to $\pm$200 mV without increasing the power consumption of the ACCIA by excluding the constant pMOS current sources of Fig. 8, and increasing the current mirroring ratio between $\rm CM_1$ and $\rm CM_2$ of Fig. 4, and $\rm M_{L7}$ and $\rm M_{R7}$ of Fig. 8 to 2, while replacing the $\rm R_1$ with a 100 kΩ resistor. However, theoretical NEF limit will be increased to 5.6, and transconductance of the current sources must be decreased in order to decrease their noise contributions. Further increase of the maximum allowed DEO is possible by increasing the power dissipation of the ACCIA.

$\rm R_2$ is implemented by a nMOS transistor of 2 μm/120 μm. If the output common-mode level is set to 1.15 V and the $V_{\rm bias}$ is tied to 3 V, equivalent resistance of this nMOS transistor is 500 kΩ, setting the gain of the IA to 10. The bandwidth of the current feedback IA is designed to be 40 kHz. Therefore, the chopping frequency is selected to be 4 kHz. The simulated 1/f noise corner frequency is lower than 400 Hz, thus 1/f noise aliasing due to chopping operation is prevented. CSF stage operates at 8 kHz and duty cycle is set to 6.25% during the tests.

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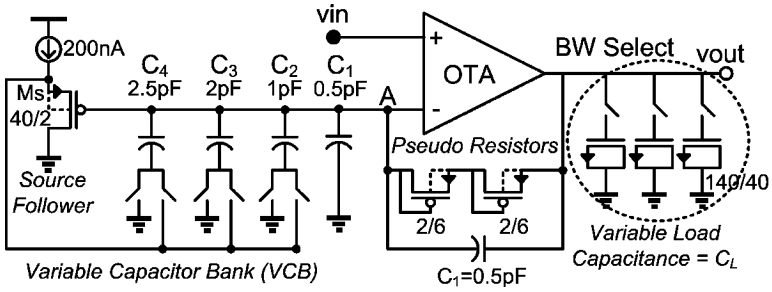

Fig. 10. Schematic of the VGA. Gain is set by the variable capacitor bank switches and low-pass cut-off frequency is set by the BW select switches.

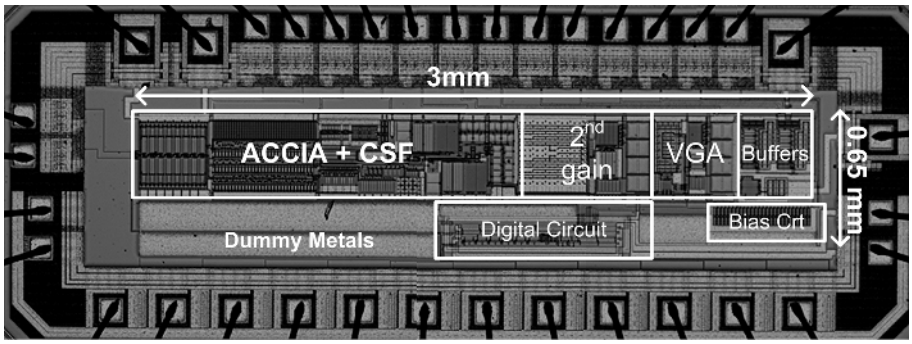

Fig. 11. Die micrograph of the biopotential readout front-end implemented in 0.5 μm CMOS process.

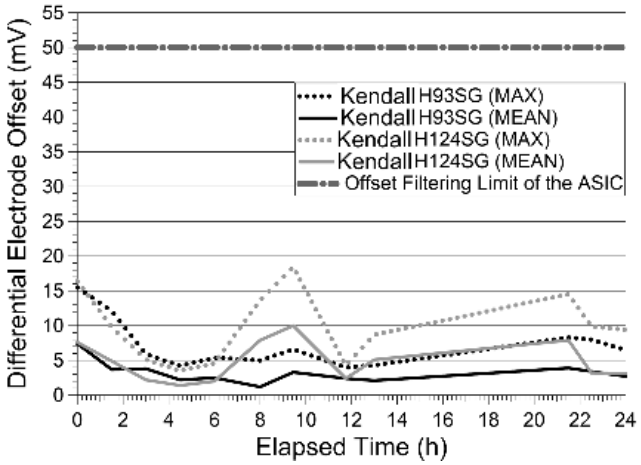

Fig. 12. DEO measurements for two different Ag/AgCl electrodes on two subjects from the same manufacturer during 24 hours. Five electrodes from each type are placed on the chest of the subject. Dotted lines show the maximum measured DEO from all possible combinations and straight lines show the average.

TABLE II
CURRENT CONSUMPTION OF THE BUILDING BLOCKS OF THE BIOPOTENTIAL READOUT FRONT-END

Building Blocks of Front-End	Current Consumption
AC Coupled Chopped IA (ACCIA)	11.1µA
Chopping Spike Filter (CSF)	800nA
Second Gain Stage	1.4µA
Third Gain Stage	750nA
Channel Buffer	2.4µA
Bias Buffer Opamps	2*600nA
Bias Circuit	2.4µA
Total Current Consumption	**20µA**
Total Power Dissipation	**60µW**

Table II gives the current consumption of the each block of the readout front-end.

A. Measurement of Performance

Fig. 13 shows the measured gain-bandwidth of the readout with changing VGA settings, when IA gain is 10. Gain of the channel can be set to 400, 800, 1550, and 2500. Moreover, high-pass cut-off frequency can be adjusted via external capacitor C_{ext2} of Fig. 4. Low-frequency roll-off occurs at 0.3 Hz for C_{ext2} of 1 μF, convenient for EEG and ECG applications, and can be set to 14 Hz for EMG applications by changing C_{ext2} to 22 nF. Additionally, low-pass cut-off frequency can be set by selecting the capacitive load of the gain stages through BW switches of Fig. 2.

Fig. 14 shows the CMRR measurement of the front-end and the change of CMRR with changing DEO. CMRR of the front-end is better than 120 dB up to 1 kHz and better than 110 dB, measured at 100 Hz, with 50 mV DEO. Fig. 15 demonstrates the operation of the chopping spike filter stage. Gain of the readout is 800, bandwidth is set to minimum, CSF duty cycle is 6.25%, and source resistance of input signal is 10 kΩ. Chopping spike components, measured at the output of the front-end, are completely filtered by the CSF stage.

Fig. 16 shows the measured input-referred voltage noise PSD of the biopotential readout front-end. Thermal noise level of the front-end is measured to be 57 nV/$\sqrt{}$Hz, which is consistent with the simulated value of 60 nV/$\sqrt{}$Hz. Chopping effectively eliminates the 1/f noise of the IA. Corner frequency of the 1/f noise is reduced from 350 Hz to 3 Hz, if the gain of the IA is 10. Residual 1/f noise is due to the gm_2 stage of Fig. 4 and stages

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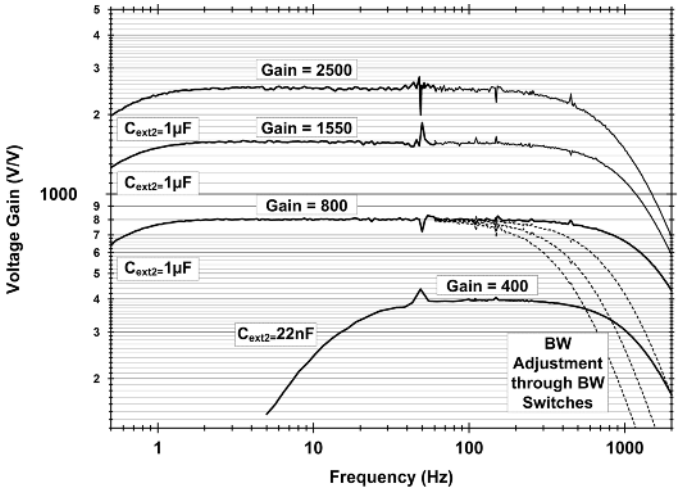

Fig. 13. Gain-bandwidth measurement of the biopotential readout front-end. Gain is adjusted through VGA. High-pass cut-off frequency is defined by the external capacitor, C_{ext2}. High cut-off frequency is set by digitally selecting the load capacitor of the gain stages.

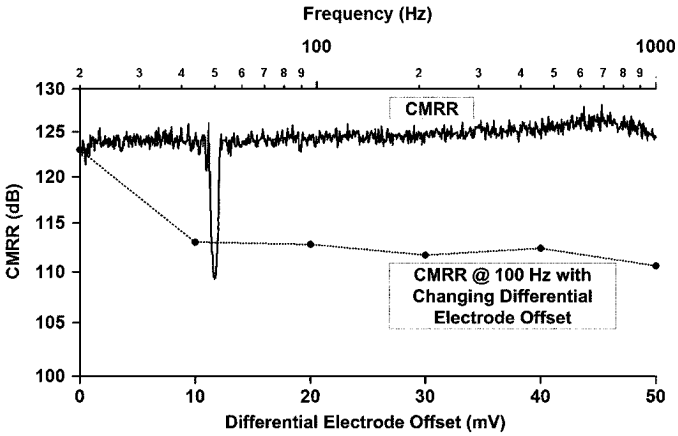

Fig. 14. CMRR measurement of the readout front-end and the change of CMRR with increasing DEO.

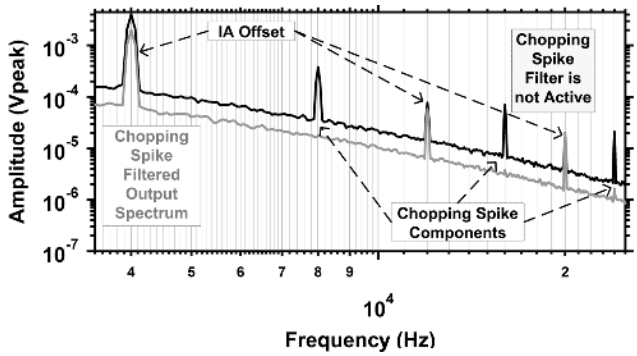

Fig. 15. Measured output spectrum of the front-end when gain is 800 and bandwidth is set to minimum. Chopping spike components appearing at the even harmonics of chopping frequency (4 kHz) is completely filtered by the chopping spike filter. (Chopping spike filtered spectrum is shifted to increase clarity).

following the ACCIA. As Fig. 16 shows, 1/f noise is decreased if the gain of the ACCIA is set to 20 via changing the gate bias of R_2 proving that the residual 1/f noise is due to the back-end

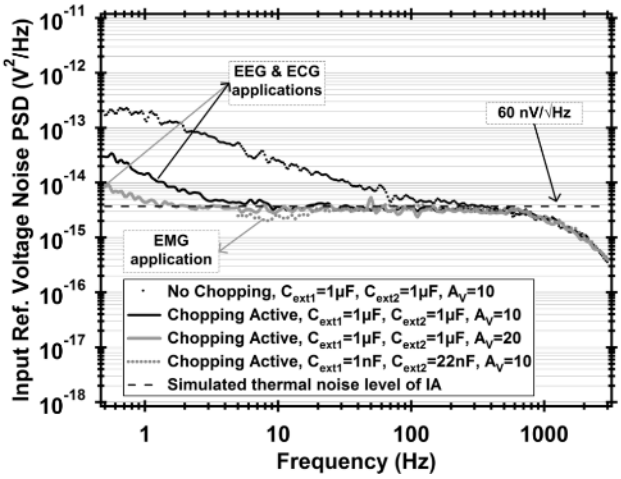

Fig. 16. Measured input-referred voltage noise PSD of the biopotential readout front-end demonstrating the reduction of 1/f noise. Chopping reduces the 1/f noise corner frequency from 350 Hz to 3 Hz, when the IA gain is 10. If the IA gain is set to 20, the 1/f noise is decreased, proving that the residual 1/f noise is due to the back-end stages.

TABLE III
IMPROVEMENT OF TOTAL NOISE WITH CHOPPING

Application	Integration BW (Hz)	Unchopped Noise (μV_{rms})	Chopped Noise (μV_{rms})
EEG	0.5-40	0.95	0.41
ECG	0.5-125	1.21	0.67
EMG	14-350	1.32	1.05

stages. Table III shows the improvement of the noise performance with chopping for different applications of the ASIC and Table IV summarizes the measured performance of the ASIC.

B. Biological Test Results

Fig. 17 shows the extracted biopotential signals from the readout front-end using disposable Ag/AgCl electrodes for ECG and EMG measurements and using Ag/AgCl cup electrodes with conductive paste for EEG measurements. It is important to note that no digital signal processing is performed on the extracted biopotential signals. EEG measurement has been performed on a subject with two electrodes connected to the backside of the skull (occipital cortex) and when his eyes are closed. Gain of the front-end is set to 2500 with minimum bandwidth configuration (140 Hz), and low cut-off frequency is set to 0.3 Hz by selecting C_{ext2} of 1 μF. Fig. 18 demonstrates that dominant rhythm at the output is in the alpha range (8–13 Hz) [5] and there is no sign of the 50 Hz. Similarly, ECG is extracted by connecting two electrodes to the chest of the subject and setting the gain of the front-end to 800 and bandwidth to 350 Hz, and keeping high-pass cut-off frequency at 0.3 Hz. All the characteristics of an ECG wave are clearly visible without any sign of 50 Hz. Finally, for the extraction of EMG waves, two electrodes are connected to the right arm muscle and gain is set to 400 with high cut-off frequency of 400 Hz, and C_{ext2} is changed by a 22 nF capacitor in order to set the low cut-off frequency to 14 Hz.

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TABLE IV
PERFORMANCE SUMMARY OF BIOPOTENTIAL READOUT FRONT-END (FOUR SAMPLES)

Voltage Supply	3V
Current Consumption	20μA
Input Common Mode Range	1.05V – 1.7V
Electronic Gain Selection (IA Gain = 10)	390, 800, 1550, 2500
Continuous Gain Adjustment	via R_2
Input Referred Voltage Noise Density	56.6 – 57.4 nV/√Hz
THD (@ 5 mVpp input and minimum gain)	0.45 – 0.52 %
CMRR (0 mV DEO)	> 120dB
CMRR (50 mV DEO)	> 110dB
PSRR + (@ 50Hz)	> 80dB
PSRR – (@ 50Hz)	> 78dB
Low Cut-Off Frequency (C_{ext2}=1μF, C_{ext2}=22nF)	0.30-0.34 Hz, 14.0 – 15.8Hz
High Cut-Off Frequency	Electronically Selectable
DC Input Current (@50 mV DEO)	< 0.5nA

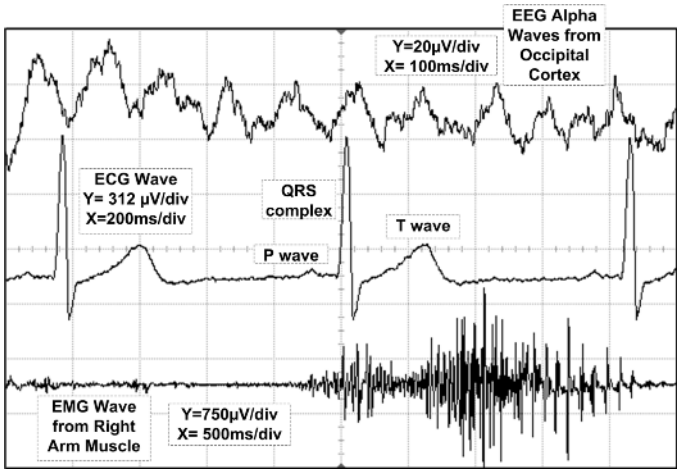

Fig. 17. Extracted biopotential signals from the readout front-end using Ag/AgCl electrodes without any digital signal processing. Amplitudes are referred to the front-end input.

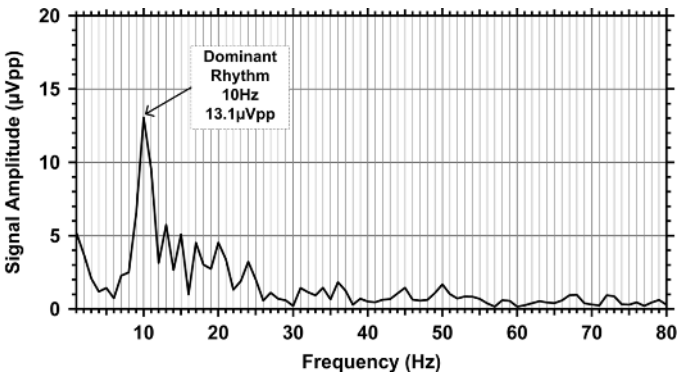

Fig. 18. Spectrum of the extracted EEG signal of Fig. 17 from occipital cortex. Patients' eyes are closed, thus dominant rhythm is in alpha range.

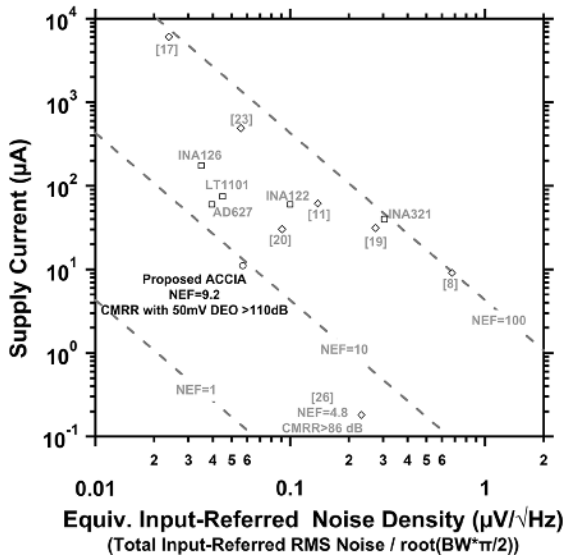

Fig. 19. Power-noise performance comparison of the ACCIA with the commercially available micropower IAs (□) and IAs from the literature (◇). Constant NEF contours are indicated by dashed lines. NEF of the commercial IAs are calculated for a −3 dB cut-off frequency of 100 Hz and including the 1/f noise of the IAs.

C. Comparison

In order to compare the power–noise performance of different amplifiers, noise efficiency factor (NEF) [19] is used as a figure of merit. A bipolar transistor having only thermal noise achieves a NEF of 1. Fig. 19 compares the power–noise performance of the ACCIA with the IAs in the literature and with the commercially available micro-power IAs. The presented IA achieves an NEF of 9.2, which is calculated from the 57 nV/$\sqrt{\text{Hz}}$ noise level and 11.1 μA current consumption. The discrepancy with the theoretical NEF value of 4.7 and measured value of 9.2 is due to the fact that current source transistors are operating barely in strong inversion. If the supply voltage is increased to 5 V, NEF of the ACCIA can be improved considerably. The IA of [22] is not included in the NEF curve, since low-input impedance of the AC-coupled amplifier of [22] will divide the input signal, resulting in a much lower signal-to-noise ratio than presented. Moreover, on the contrary to the proposal of [22], it is not possible to replace the external capacitor and resistor with on-chip capacitor and a transistor operating in subthreshold region, since this will prevent the operation of the chopping amplifier.

The only IA achieving a better NEF is proposed by [26]. However, it not only has very low CMRR (86 dB), which makes it unsuited for extracting clean biopotential signals, but also features a fixed high-pass cut-off frequency, which prevents its use for EMG (10–20 Hz) applications. It should be noted that noise level of the EEG amplifier of [26] is high for EEG applications. Therefore, if one would like to implement a biopotential readout

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circuit using the topology of [26], then current consumption of the circuit must be increased in order to reduce the total in-band noise. However, as the thermal noise level is reduced by increasing the current consumption of the circuit, 1/f noise will start to dominate the total noise under low frequencies. Therefore, NEF of the circuit will be degraded considerably. For instance, it can be calculated from the given values of [26] that the IA of [26], which has 16 μA current consumption, would have worse noise performance than our ACCIA, if the signal bandwidth is limited 40 Hz. Thus, NEF of the IA topology of [26] would be much worse than the ACCIA presented in this paper for low-noise and low-bandwidth applications. As a result, it can be concluded that the presented ACCIA has the best power–noise trade-off in the literature for EEG and EMG applications. On the other hand, it is important to note that IA [26] can be designed to have a better NEF than our ACCIA for ECG applications (however with much worse CMRR) since high noise levels (5 μV_{pp} [33]) can be tolerated for ECG systems.

VII. Conclusion

A readout front-end with configurable characteristics for EEG, ECG and EMG signals and capable of operating from conventional Ag/AgCl electrodes is presented. The proposed AC-coupled chopping technique eliminates 1/f noise, while filtering DEO and IA offset. The proposed current feedback IA that is used in the ACCIA achieves low-power dissipation due to the minimum number of parallel branches and elimination of the opamps. Combination of the AC-coupled chopping technique with the low-power current feedback IA achieves more than 120 dB CMRR and 57 nV/$\sqrt{}$Hz input-referred noise density, while consuming only 11.1 μA from 3 V. This results in the best power–noise trade-off among the IAs in literature for EEG and EMG applications. The proposed input stage of the current feedback IA prevents the reduction of the CMRR with increasing DEO and achieves more than 110 dB CMRR at ± 50 mV DEO.

The chopping spike filter stage completely filters the chopping spike components generated due to chopping. Moreover, digitally controllable VGA stage allows the adjustment of the gain and bandwidth of the channel. If the IA gain is set to 10, channel gain can be selected to be 400, 800, 1550, and 2500 via the continuous-time VGA. Meanwhile, the channel bandwidth can be decreased or increased in order to filter the out-of-band signals that will allow decreasing the sampling frequency of the back-end ADC, which will decrease its power dissipation.

The presented front-end consumes 20 μA from a single 3 V supply, thus it is capable of operating more than 3 years from 2 AA batteries. Combination of the presented front-end with a low-power ADC and radio will enable the implementation of portable/wearable fully autonomous biopotential acquisition systems.

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