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Ying Cao, Paul Leroux, Wouter De Cock, Michiel Steyaert

Institutions: Katholieke Universiteit Leuven

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10.8 A 63,000 Q-Factor Relaxation Oscillator with Switched-Capacitor Integrated Error Feedback

Ying Cao[1,2], Paul Leroux[1], Wouter De Cock[2], Michiel Steyaert[1]

[1]KU Leuven, Heverlee, Belgium,
[2]SCK-CEN, Mol, Belgium

There is a growing interest in implementing on-chip reference clock generators for low-cost low-power area-efficient SoCs, such as implantable biomedical devices and microcomputers. Relaxation oscillators are suitable candidates to generate such reference clocks due to their compact size, low power consumption and wide frequency tuning range. However, the poor phase noise performance and large long-term variation are two major problems that limit their application.

In [1], an anti-jitter (AJ) technique is proposed to filter the jitter noise. However, it requires a low-noise high-speed comparator to generate the output clock which can be power consuming and will practically limit the oscillator's overall phase-noise performance. The power averaging feedback (PAF) technique presented in [2, 3] provides another solution to reduce the oscillator's low-offset phase noise. In the PAF configuration, an active-RC LPF is used to convert the oscillation frequency into a voltage whose slow time-varying amplitude represents the close-in phase fluctuations. Large RC values are thus required to enable accurate extraction of the waveform's DC component, which consumes more area and moreover, its response time to high-frequency noise is rather long due to its limited bandwidth.

Those issues can be solved by employing a switched-capacitor (SC) integrated error feedback (IEF), as shown in Fig. 10.8.1. The core of the relaxation oscillator remains the same as in a conventional two-grounded-capacitor structure. The basic operating waveforms are illustrated in Fig. 10.8.2. The oscillator period can be written as $T_{osc}=2 \cdot RC \cdot ln(1-\alpha)^{-1}$, where α equals $vref/vdd$. The currents that charge the capacitors are directly derived from a resistor connected to the supply, which eliminates the aging effect and noise associated with an active current source [2]. Therefore, the comparator becomes the primary contributor to the oscillator's phase noise [4]. Another important modification to the conventional architecture is using only one comparator (*cmp1*) instead of two to detect the switching threshold. This gives an advantage to enable effective suppression of low-frequency noise (e.g., flicker noise) by using error feedback. Since in the two comparators case (one comparator for each left and right branch), the noise generated in each device is uncorrelated and does not cancel out. This makes the compensation of the clock period error inaccurate.

The working principle of the IEF is explained in Fig. 10.8.2. Assuming a low-frequency noise voltage appears at the reference node of *cmp1*, it causes a small delay variation t_e in addition to the fixed comparator delay t_d. Consequently, a time error, equal to t_e, is present in the oscillator clock period. The IEF compares the final voltage at the capacitor *vcap* with the reference voltage *vref* and integrates their difference *ve* by using the SC circuits. In a short time, the charging slope on the capacitor can be considered constant when its voltage level approaches *vref*, which is set close to *vdd*. Therefore, *ve* is linearly related to t_e. By subtracting *ve* from *vc*, which is the reference level at the comparator threshold node, the clock period error can be compensated. Not only is the IEF effective at suppressing the low-frequency noise, it also improves the oscillator's stability against voltage and temperature variation due to the closed-loop structure.

The integrating operation is performed in a predefined integrate-and-hold (IH) phase t_h. This is realized by using only few additional control units. The main purpose of the control logic is to guarantee one capacitor is reset to '0' before the other reaches *vref*. Then, the alternate charging process can be sustained. This is secured by using a second comparator *cmp2* which has been set to a lower threshold *ven* to monitor the voltages at the capacitors. Once it crosses *ven*, the comparator generates a signal to terminate the integrating phase and turns the SC integrator into hold. Since *cmp2* is only used to produce clock signals for the IH circuits, its noise specification has no influence on the oscillator's overall phase noise.

In order to effectively and accurately integrate the error information on the capacitor within 40ns scale ($<1/2\ T_{osc}$), the amplifier used in the SC has to have moderate-speed and high-gain. A normal class-A amplifier will consume a large amount of power to fulfill all requirements. In this design, a class-AB structure is adopted, which offers large driving ability while the static power consumption can be kept low. The amplifier has a differential-input and single-ended output structure, as shown in Fig. 10.8.3. Chopping has also been implemented in the amplifier to reduce its offset and flicker noise, which adds to the total phase noise of the oscillator clock. The amplifier has a DC gain of 80dB, and a static current draw of 20μA.

The relaxation oscillator has been implemented in a 65nm CMOS technology. For the selected R=46kΩ, C=0.85pF, $R1$=45kΩ, $R2$=30kΩ and $R3$=50kΩ, the oscillator frequency is f_{osc}=12.6MHz. The oscillator core, including the IEF, occupies an area of only 0.01mm², and consumes 82μA from a 1.2V supply. Figure 10.8.4 shows the measured phase-noise performance of the oscillator at 1.2V. It can be clearly seen that, the low-frequency noise has been greatly suppressed by the IEF. This enables the oscillator to achieve a phase noise of –62dBc/hz at 1kHz offset frequency, which turns out to a very high FOM [4] of 154.1dB@1kHz. At a large offset frequency of 1MHz, the phase noise is –120dBc/Hz. The –20dB/dec declining slope between 1kHz and 1MHz is clearly obtained from the measured phase-noise data.

The reduction of the flicker noise in the relaxation oscillator will lead to a high quality factor and small accumulated jitter. This is evident from the measurement results shown in Fig. 10.8.5. In the power spectrum of the oscillator output, the –3dB bandwidth is found to be 200Hz. This results in a quality factor of 63,000, which outperforms state-of-the-art relaxation oscilators (see Fig. 10.8.6). The measured accumulated jitter with IEF is proportional to the square root of the number of periods. This is the case only when the long-term jitter is dominated by uncorrelated noise, which confirms the removal of 1/f noise. The measured frequency change of the oscillator subjected to supply voltage variation is only ±0.07% over a range of 1.1 to 1.5V supply, which proves the effectiveness of the SC IEF loop. The temperature stability of the oscillator is mainly determined by the thermal characteristic of the charging resistor R. From 0 to 80°C, the total frequency variation is within ±0.82%. This could be further calibrated by applying an appropriate temperature gradient to *vref* according to the temperature coefficient of the charging resistor.

Figure 10.8.6 presents the performance summary and comparison with other state-of-the-art designs which have similar specifications and also with some recent MEMS oscillators. The proposed oscillator achieves the best reported quality factor in the category of relaxation oscillators with minimum area occupation. MEMS oscillators indeed have better frequency stability and lower close-in phase noise. However, this comes at the cost of a higher power consumption, larger area, and the requirement of special process steps. The relaxation oscillator with SC IEF proves a solution for high-Q low-cost on-chip clock generation.

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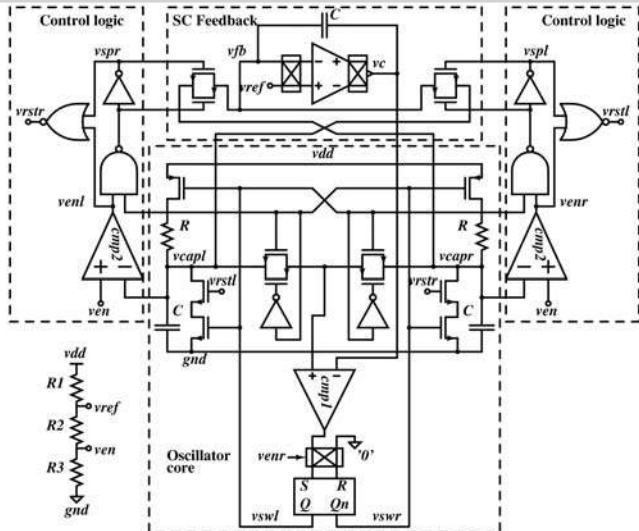
Figure 10.8.1: Schematic of the proposed relaxation oscillator with SC integrated error feedback.
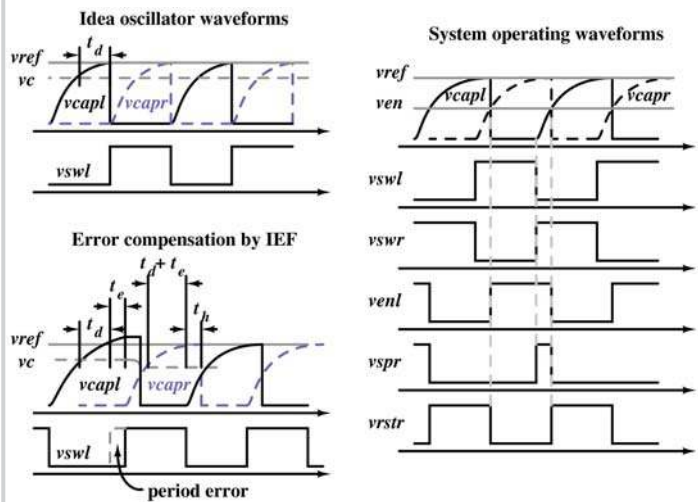

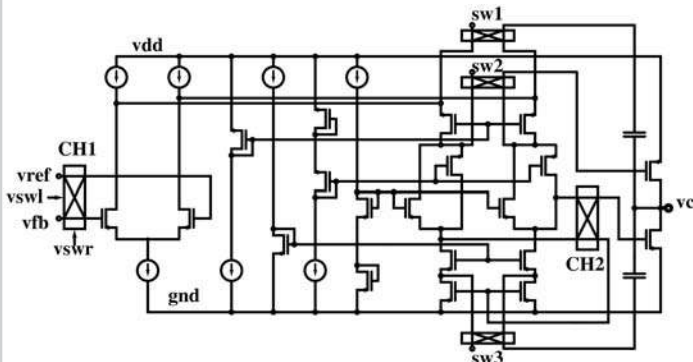Figure 10.8.2: Oscillator operating waveforms and error compensation mechanism.

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Figure 10.8.3: Schematic of the differential-input single-ended output chopped class-AB amplifier implemented in the SC integrator.

−62dBc/Hz@1kHz
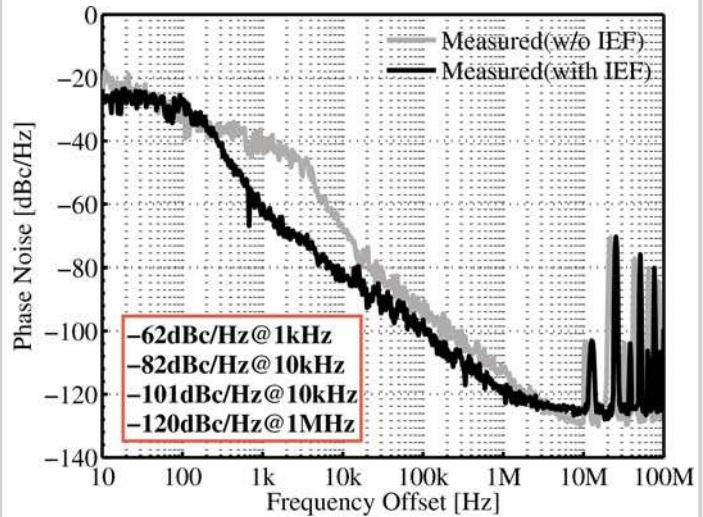−82dBc/Hz@10kHz
−101dBc/Hz@10kHz
−120dBc/Hz@1MHz

Figure 10.8.4: Measured phsae noise @1.2V (Agilent PXA Signal Analyzer).
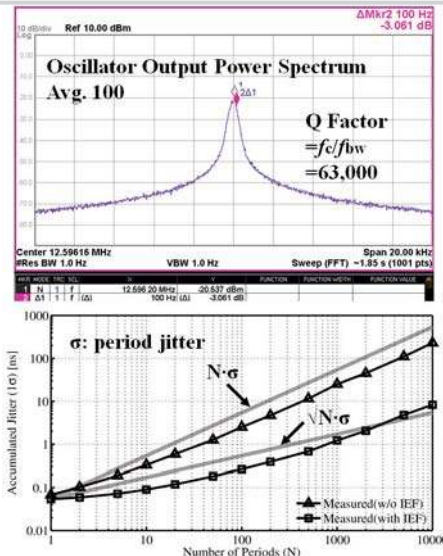
Figure 10.8.5: Measured quality factor and accumulated jitter performance.

| Feature	[1]	[2]	[3]	[5]	[6]	This Work
	Relaxation	Relaxation	Relaxation	MEMS	MEMS	Relaxation
Technology	65nm CMOS	0.18μm CMOS	65nm CMOS	0.35μm CMOS	MEMS: HARPSS-on-SOI IC: 0.5μm CMOS	65nm CMOS
Area [mm²]	0.03	0.04	0.02	0.026	2.25	0.01
Frequency [MHz]	12	14	6	60	5.5	12.6
Vdd [V]	1.3	1.8	1.25	MEMS: 12 IC: ±1.65	MEMS: 3-15 IC: 5	1.2
Power Cons. [μW]	91	43.2	100	950	1800	98.4
Q-Factor	N/A	11,666	23,885	48,000	Resonator: 103,000 Oscillator: 54,000	63,000
FOM [dB]	162 @100kHz	146@100kHz	117.6@1kHz	N/A	N/A	154.1@1kHz, 152.6@100kHz
Variation [%] with Vdd	N/A	±0.16 @1.7 to 1.9V	±0.26 @1.15 to 1.35V	N/A	N/A	±0.07 @1.1 to 1.5V
Variation [%] with Temp.	N/A	±0.75 @-40 to 125°C	±0.2 @-40 to 125°C	35ppm @0 to 70°C	332ppm @25 to 125°C	±0.82 @0 to 80°C

Figure 10.8.6: Performance comparison.
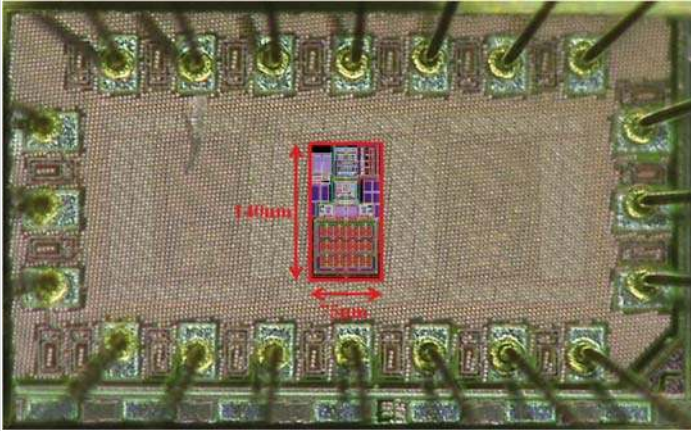
Figure 10.8.7: Die photo. The core area is 0.075×0.14mm².