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A 64-MHz 2.15-µW/MHz On-Chip Relaxation Oscillator with 130-ppm/°C Temperature Coefficient

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Abstract: This paper presents a 2.15 µW/MHz at the frequency of 64 MHz relaxation oscillator with a dynamic range of frequency from 47.5 MHz to 80 MHz. To reduce the power consumption and improve energy efficiency, this work employs only one comparator and one capacitor to generate the output clock in comparison with conventional relaxation oscillator structures. A total of 50% ± 5% of the duty cycle is obtained for the output clock by implementing an auxiliary comparator. The proposed relaxation oscillator uses the output voltages of an external low-dropout (LDO) voltage and bandgap reference (BGR) for the required supply and reference voltages, respectively. Two current sources are implemented to provide the required currents for trimming the output frequency and driving the comparators. Measurement results indicate that the relaxation oscillator achieves a temperature coefficient (TC) of 130 ppm/°C over a wide temperature range from −25 °C to 135 °C at the frequency of 64 MHz. The relaxation oscillator consumes 115 µA of current at the frequency of 64 MHz under a low-dropout (LDO) voltage of 1.2 V. The proposed relaxation oscillator is analyzed and fabricated in standard 90 nm complementary metal-oxide semiconductor (CMOS) process, and the die area is 130 µm × 90 µm.

Keywords: relaxation oscillator; hysteresis comparator; low-power oscillator; crystal replacement; duty cycle compensation

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1. Introduction

Clock generators are widely used in integrated circuit (IC) design to offer a reference clock from several hertz to tens of gigahertz frequency range. In a radio frequency (RF) transmitter (TX) chain, an up-mixer circuit shifts generated low-frequency (LF) data from a digital-to-analog converter (DAC) to RF and delivers it to a power amplifier (PA) for transmission [1]. On the other hand, at the first stage of a receiver (RX) chain, a low-noise amplifier (LNA) is located to amplify the received signal from the antenna. The signal is shifted from RF to LF through a down-mixer circuit and delivered to a base-band amplifier (BBA) and an analog-to-digital converter (ADC) [2,3]. Phase-locked loops (PLLs) are the most common architectures for generating an RF reference clock [1,4].

To generate LF and high frequency (HF) clocks, the relaxation oscillators are suitable candidates to realize the growing demand for on-chip, low-power, and low-cost clock generators for applications such as the Internet of Things (IoT), wearable devices, wireless network sensors, etc. Crystal oscillators offer ultralow phase noise performances. However, due to the high values of employed inductors and capacitors, the crystal oscillator has to be used as an external component, and it would be a costly product [5]. As a result, crystal oscillators can be replaced by low-cost, low area, and low-power relaxation oscillators for on-chip applications [6]. In Bluetooth low energy (BLE) applications, the potential inaccuracy of the oscillator causes the receiver to be activated for a guard time before the actual beacon. Thus, to ensure reliable reception when operating slave sensor nodes

in connection modes, the high temperature accuracy of the clock generator is required, especially for low-duty cycle signals [7]. Nano-watt power consumption clock generators are proposed in [7–9]. Nevertheless, the target frequencies do not exceed tens of kilohertz. Although the reported works [10–12] provide high stable output frequency of tens of megahertz clock generators, the circuits consume huge amounts of power.

In [12], a relaxation oscillator with using frequency-error feedback loop in a 5 nm fin field-effect transistor (FinFET) process is proposed. However, the design consumes a large power consumption of 840 µW at the target frequency of 77 MHz. In [13], to minimize power consumption and sensitivity to temperature variation, simplified logic control circuits are used by employing an improved delay compensation technique. However, the structure and performance level of the design should be improved to accommodate higher frequencies. The reported oscillator in [14] uses matching between capacitors and transistors to suppress process and temperature variations. However, a high energy efficiency of 408 µW/MHz is achieved.

Supply voltage variations have effects on voltage swings and comparator bandwidth. On the other hand, current sources use reference voltages to provide a constant current for wide temperature variations. Therefore, the generated current could be changed by reference voltage variations, where these variations affect the behavior of comparators and the charge time of capacitors. A low dropout (LDO) can minimize supply voltage variations and the required reference voltages over a wide temperature variations could be offered by a bandgap reference (BGR) [15]. In this work, an external LDO and BGR are employed to provide the required voltages 1.2 V, 900 mV, respectively.

The proposed relaxation oscillator in this paper offers 2.15 µW/MHz of energy efficiency at 64 MHz by using a single comparator structure to generate the output clock in comparison with conventional structures [7–9,13,16]. The organization of this paper is as follows: Section 2 discusses the proposed relaxation oscillator; Section 3 presents the hysteresis comparator operation in circuit level; and Section 4 discusses the programmable current source. The experimental results are shown in Section 5.

2. Overall Structure of the Proposed Relaxation Oscillator

The proposed relaxation oscillator includes two hysteresis comparators (Comp.1 and Comp.2) and two current sources (Cur.Gen.1 and Cur.Gen.2), as indicated in Figure 1.

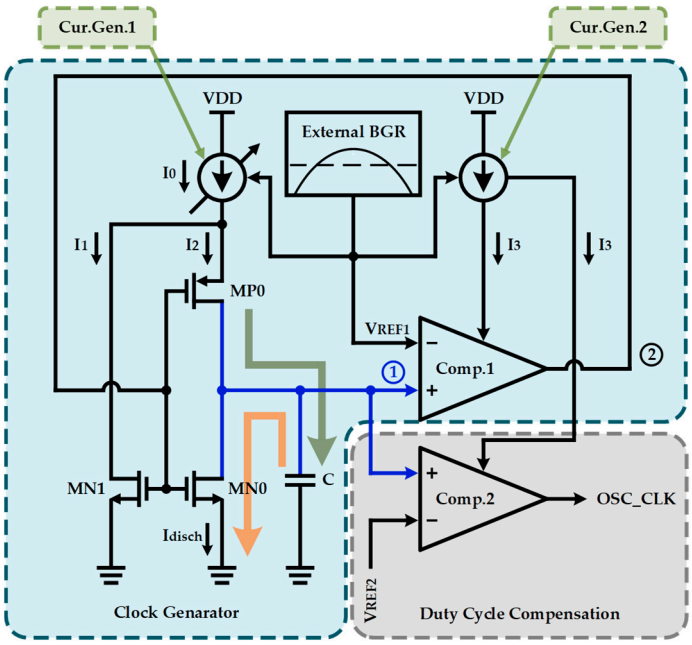


Figure 1. Architecture of the proposed relaxation oscillator.

Comp.1 and Comp.2 are implemented to generate the output frequency and compensate for the duty cycle, respectively. Cur.Gen.1 provides a programmable DC current to charge the capacitor (C). Cur.Gen.2 is employed to offer the required current to drive Comp.1 and Comp.2.

In the design of relaxation oscillators, employing two or more comparators to generate the output clock could increase the power consumption. Moreover, the mismatch between comparators and capacitors could be increased at the layout level when the number of them is more than one. Therefore, to improve the energy efficiency and minimize the mismatch in this work, only one comparator (Comp.1) and one capacitor (C) are employed to generate clock frequency in comparison to conventional structures [7–9,13,16].

Figure 2 illustrates the timing diagram of the positive input and output of Comp.1, Node.1 and Node.2, respectively, when the negative input of Comp.1 is connected to the reference voltage of V_{REF1}.

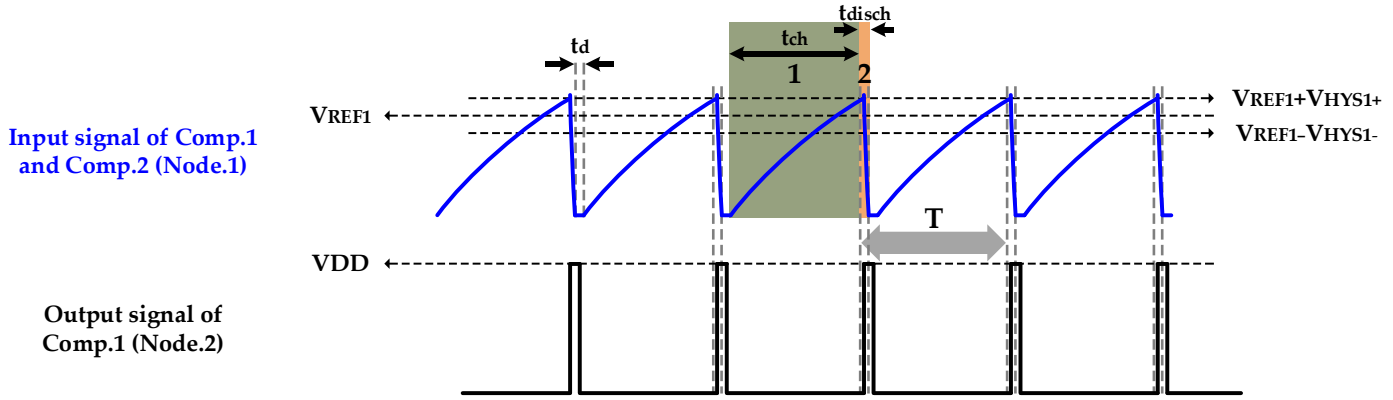


Figure 2. Timing diagram of the positive input (Node.1) and output of Comp.1.

As emphasized in Figure 2, the output voltage of Comp.1 would be described in two scenarios. (1) Whereas the voltage level of the positive input of a non-inverting comparator is 0 V, the output of the comparator follows its positive input; hence, the voltage of Node.2 is GND. In this scenario, when the output voltage of Comp.1 is GND, the transistors MN0 and MN1 operate as open circuit switches; therefore, the capacitor (C) is charged by $I_2 = I_0$ through MP0 till its voltage meets the sum of V_{REF1} and the up threshold voltage of Comp.1 (V_{HYS1+}), as shown in Figure 1. The capacitor (C) would be charged with a linear slope by an ideal current source. However, due to the output impedance of Cur.Gen.1, the slope of V_c is not linear, as shown in Figure 2. The charge time of the capacitor (C) is written by following expressions:

$$I = C\frac{dV}{dt} \tag{1}$$

$$t_{ch} = \frac{C}{I}(V_c) \tag{2}$$

where

$$V_c = V_{REF1} + V_{HYS1+} \tag{3}$$

(2) In the second scenario, when the voltage level of the capacitor (C) (Node.1) is equal or greater than $V_{REF1} + V_{HYS1+}$, the output voltage of Comp.1 is switched to VDD. On this transition, the transistor MP0 operates as an open circuit switch and the transistors MN0 and MN1 are in triode region. The transistor MN0 discharges the stored charge on the capacitor (C). The current of the transistor MN0 can be expressed by the following equation:

$$I_{disch} = -\frac{V_C}{R_{ON,MN0}}e^{-\frac{t}{\tau}} \tag{4}$$

where $R_{ON,MN0}$ and τ are given by the following expressions, respectively:

$$R_{ON,MN0} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_{MN0}(V_{GS,MN0} - V_{TH,n})} \tag{5}$$

$$\tau = R_{ON,MN0} \times C \tag{6}$$

thus, the discharge time could be given by:

$$t_{disch} = 5 \times \tau \tag{7}$$

To satisfy Kirchhoff's current low (KCL), during the discharge time, the transistor MN1 operates in the triode region and I_0 is connected the ground via the transistor MN1 ($I_1 = I_0$). The capacitor (C) is discharging and the output voltage of Comp.1 switches to GND when the voltage level at the Node.1 is equal or less than V_{REF1} minus the down threshold voltage of Comp.1 (V_{HYS1-}). Furthermore, as shown in Figure 2, the switching delay of Comp.1 and the transistors MN0 and MP0 generate a non-negligible delay (t_d) that must be taken into account. Because both transistors MN0 and MP0 are in the off region during the delay (t_d), the capacitor (C) does not charge immediately. The capacitor (C) resumes charging when the transistors MN0 and MP0 operate in cut-off and triode regions, respectively. Thereby, the period (T) of the oscillator can be defined by the following expression:

$$T = \frac{C}{I}(V_{REF1} + V_{HYS1+}) + 5(R_{ON,MN0} \times C) + t_d \tag{8}$$

then:

$$f = \frac{1}{T} \tag{9}$$

In Equation (8), C, V_{REF1}, $R_{ON,MN0}$, and t_d have constant values. Hence, the operating frequency of the oscillator could be reconfigurable by employing a programmable current source to generate I.

As indicated in Figure 2, the frequency of the oscillator is defined by Comp.1, nonetheless, the duty cycle of the generated clock could not reach 50%, due to the fast discharge of the capacitor (C). Therefore, an auxiliary comparator (Comp.2) is employed to compensate for the required duty cycle of the output clock. It is noteworthy that Comp.2 has no contribution to the charge and discharge of the capacitor (C). Thus, the auxiliary comparator (Comp.2) does not change the period (T).

Figure 3 shows the timing diagram of the positive input and output of Comp.2, Node.1, and OSC_CKL, respectively. The operation of Comp.2 is the same as that of Comp.1, where the reference voltage of Comp.2 (V_{REF2}) is lower than the reference of Comp.1 (V_{REF1}) for duty cycle compensation, as stated in Figure 3. Because the signal at Node.1 is independent of the output of Comp.2, by selecting a lower reference voltage (V_{REF2}) for Comp.2, the duty cycle could be compensated. The operation of Comp.2 follows two conditions: (1) When the voltage level of the positive is equal to or greater than $V_{REF2} + V_{HYS2+}$, the output of Comp.2 is VDD, and (2) while it is equal to or lower than $V_{REF2} - V_{HYS2-}$, the output voltage is 0 V. As shown in Figure 3, the duty cycle of the output clock could be reconfigurable by selecting different values of the reference voltage (V_{REF2}), V_{HYS2+}, and V_{HYS2-}.

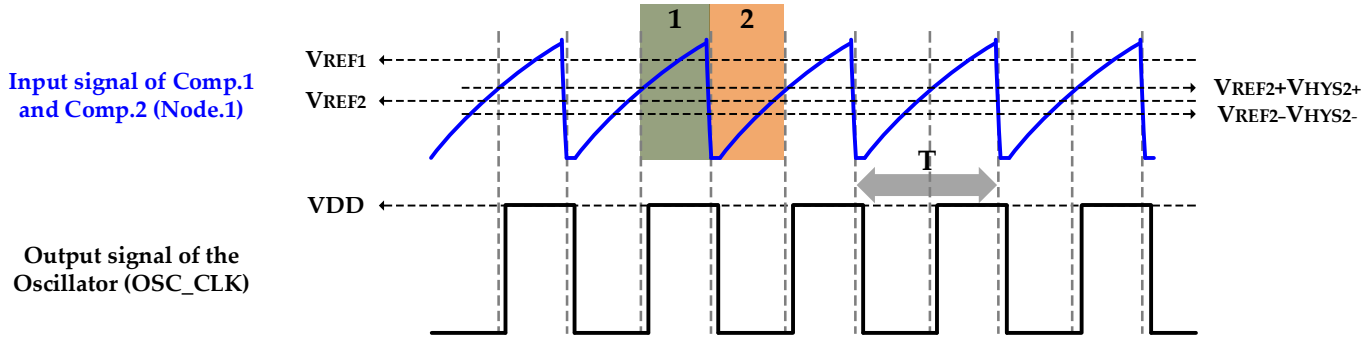


Figure 3. Timing diagram of the positive input (Node.1) and output of Comp.2.

3. Hysteresis Comparator

A hysteresis comparator is one of the most common circuits for generating clocks in the LF and HF ranges. A comparator-based oscillators provide better temperature coefficient (TC) in comparison with an inverter-based oscillators due to the better temperature dependent behavior of comparators [17]. Different up (V_{HYS+}) and down (V_{HYS-}) threshold voltages can be provided by a hysteresis comparator. The loop characteristics of the output voltage of a non-inverting comparator is indicated in Figure 2. A non-inverting comparator operates as follows: when the voltage level of the positive input (V_{IN}) is lower than voltage of the negative input minus the different down threshold voltage ($V_{INB} - V_{HYS-}$), the output voltage is GND, and it is VDD when the voltage of the positive input is greater than the sum of the negative input and down threshold voltage ($V_{INB} + V_{HYS+}$) [18,19], as illustrated in Figure 4. Therefore, when the negative input is connected to a reference voltage (V_{REF}), the output voltage of the non-inverting hysteresis comparator would be reported as follows:

$$\begin{cases} V_{IN} < V_{REF} - V_{HYS-};\ V_{OUT} = GND \\ V_{IN} > V_{REF} + V_{HYS+};\ V_{OUT} = VDD \end{cases} \quad (10)$$

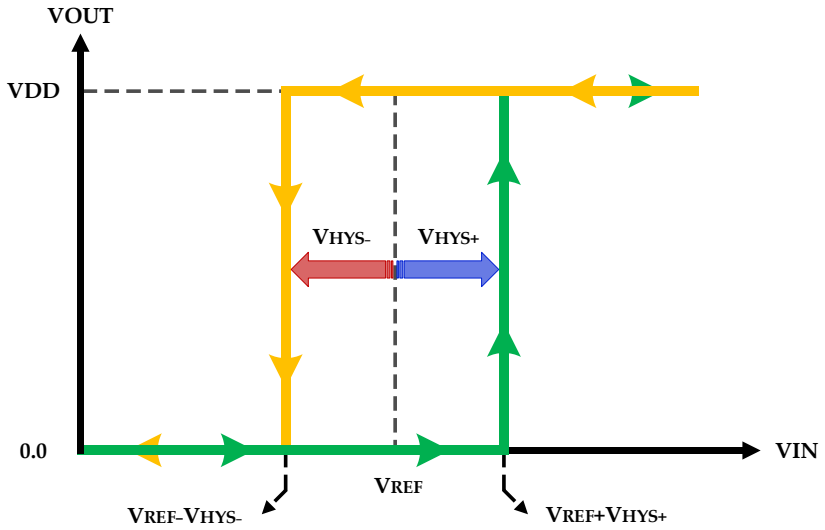


Figure 4. Loop characteristics of a non-inverting comparator.

Figure 5 indicates the schematic of the employed hysteresis comparator in this work. a is defined by the size ratios of transistors MP2 and MP3, where it is greater than 1 and generates the V_{HYS+}. On the other hand, b is greater than 1 as well; it is described by the

size ratio of transistors MP4 and MP5 to create V_{HYS-}. Thereby, the values of V_{HYS+} and V_{HYS-} can be calculated [18,19]:

$$V_{HYS+} = \sqrt{\frac{2I_{bias}}{\mu C_{ox}\left(\frac{W}{L}\right)_{MN4,5}}} \times \frac{\sqrt{a}-1}{\sqrt{a}+1} \tag{11}$$

$$V_{HYS-} = \sqrt{\frac{2I_{bias}}{\mu C_{ox}\left(\frac{W}{L}\right)_{MN4,5}}} \times \frac{\sqrt{b}-1}{\sqrt{b}+1} \tag{12}$$

where $(W/L)_{MN4,5}$ is the size of transistors MN_4 and MN_5. When the input voltage remains within the up (V_{HYS+}) and down (V_{HYS-}) threshold voltages, the output retains memory of its state, as stated in Figure 4. It is worth noting that the voltage level at the input has to exceed the up (V_{HYS+}) threshold voltage to switch the output voltage from GND to VDD. In the other case, the voltage level of the input has to be driven below the down (V_{HYS-}) threshold voltage to switch the output voltage from VDD to GND.

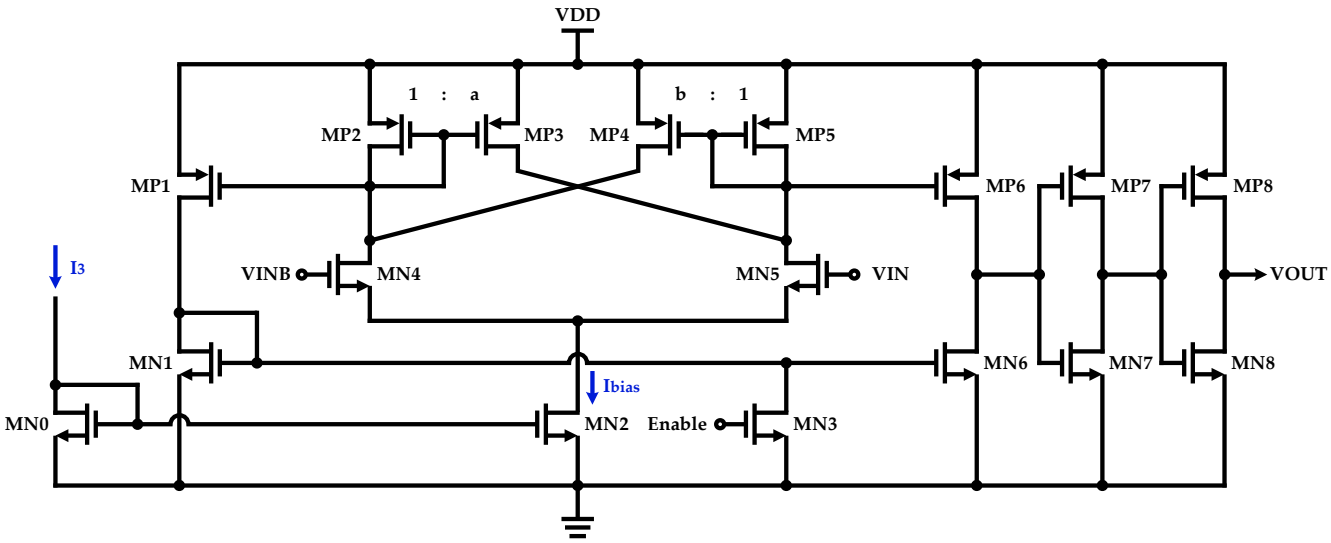


Figure 5. Structure of the implemented non-inverting hysteresis comparator.

4. Programmable Current Source

As discussed in the overall architecture section, the value of the capacitor (C) has a direct effect on the period (T) and frequency of the oscillator. Moreover, in the SoC design, parasitic capacitors due to metals and transistors are inevitable, although the parasitic capacitors can be minimized in layout. Nevertheless, the minimized parasitic capacitors should be extracted and added to the capacitor (C). Figure 6 indicates the structure of the programmable current source which is implemented to eliminate variable parasitic capacitors due to the operation of transistors in ON or OFF regions. The current of I_0 is controllable by 5-bit TRIM<4:0>. The current source provides a reconfigurable of DC current from 9.6 µA to 18.4 µA for the lowest and highest operation by 32 steps with 275 nA resolution to control the frequency. Therefore, the current of I_0 can is given by the following expression:

$$I_0 = 2 \times I_{REF} + N \times I_0{}' \tag{13}$$

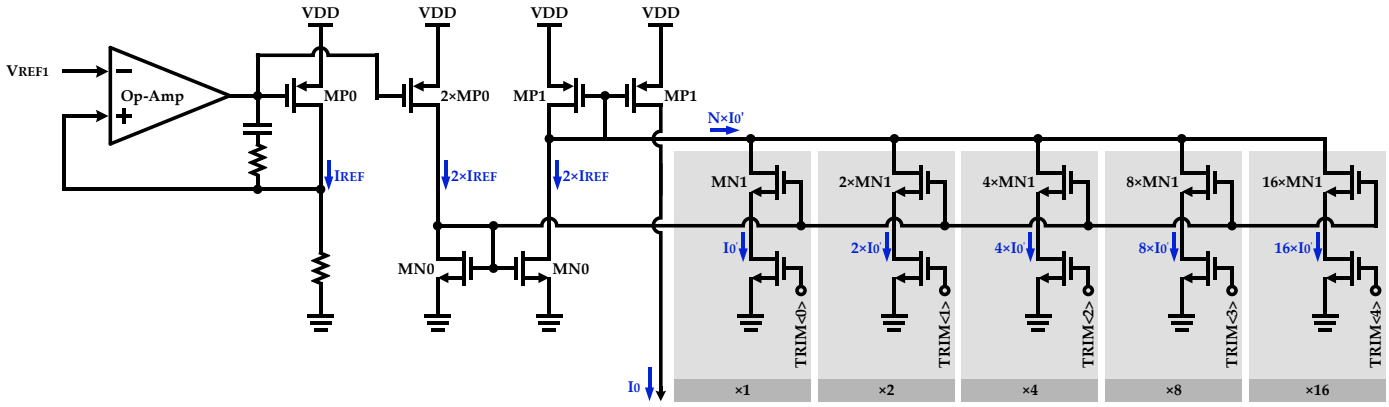
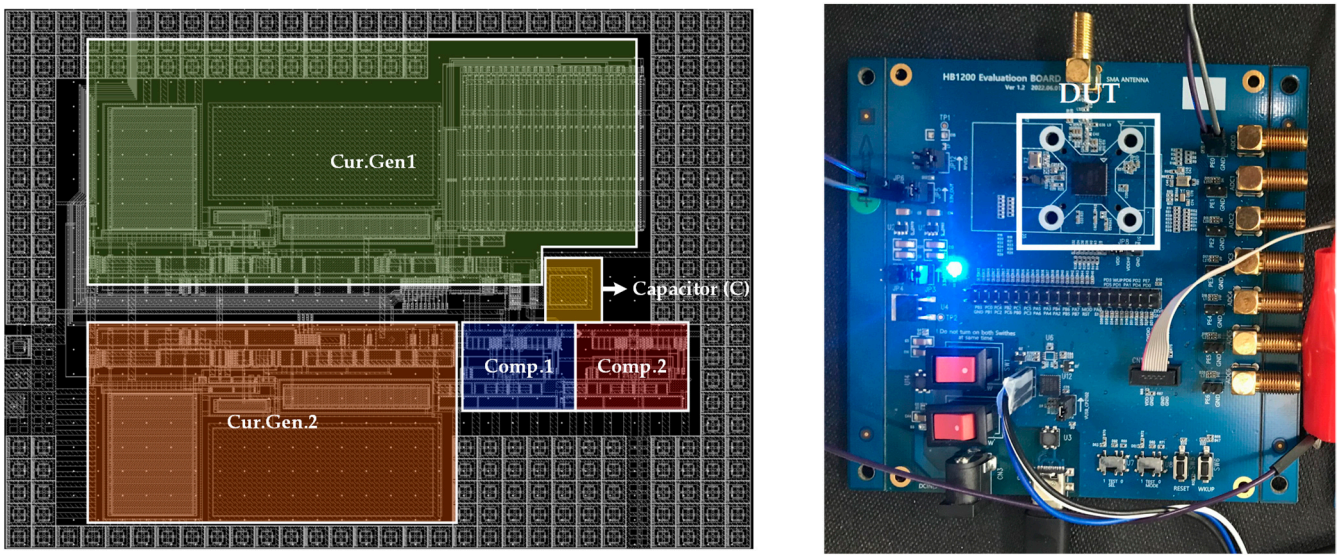


Figure 6. Schematic of the implemented programmable current source (Cur.Gen.1).

5. Experimental Results

The proposed fully integrated relaxation oscillator is analyzed and implemented in a 90 nm complementary metal-oxide semiconductor (CMOS) process with an active area of 0.0117 mm^2. Figure 7a illustrates the location of Cur.Gen.1, Cur.Gen.2, Comp.1, Comp.2, and the capacitor (C) in the top layout of the implemented relaxation oscillator. Figure 7b shows the device under test (DUT) for measurement. The required supply and reference voltages are offered by external LDO and BGR, respectively, to measure the output clock of the oscillator. The relaxation oscillator consumes 115 µA of current at the frequency of 64 MHz. The post-layout simulation results of the internal (Node.1 and Node.2) and output clock signals of the oscillator are depicted in Figure 8. The duty cycle of 47% is achieved in the presented paper by employing the auxiliary comparator. Monte-Carlo simulation presents an estimation of the behavior of the circuit for process corner variations. Figure 9 illustrates the simulated Monte-Carlo results of the proposed relaxation oscillator for global and local mismatch process errors, where the standard derivation of 2.56 MHz is obtained for 100 samples. Figure 10a indicates measurement results of the oscillator where an overall dynamic range of 32.5 MHz from 47.5 MHz to 80 MHz with a resolution of 1 MHz is achieved. Measurement results illustrates a TC of 130 ppm/°C is obtained over a wide temperature range from −25 °C to 135 °C at the frequency of 64 MHz, as depicted in Figure 10b.



(**a**) (**b**)

Figure 7. (**a**) Top layout of the proposed relaxation oscillator, and (**b**) DUT.

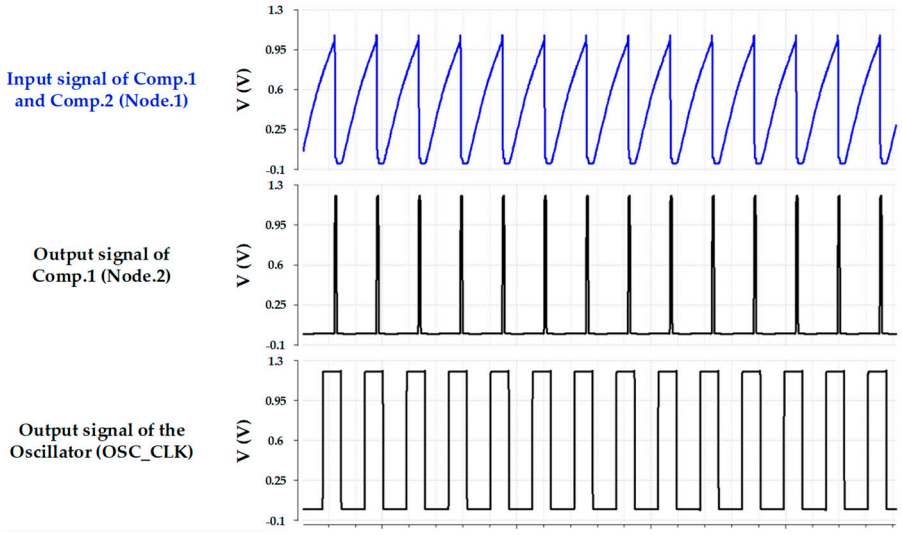


Figure 8. Simulated timing diagram of proposed relaxation oscillator.

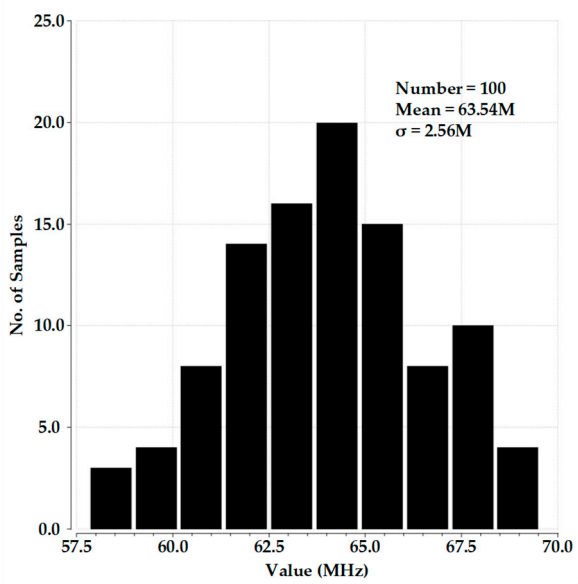
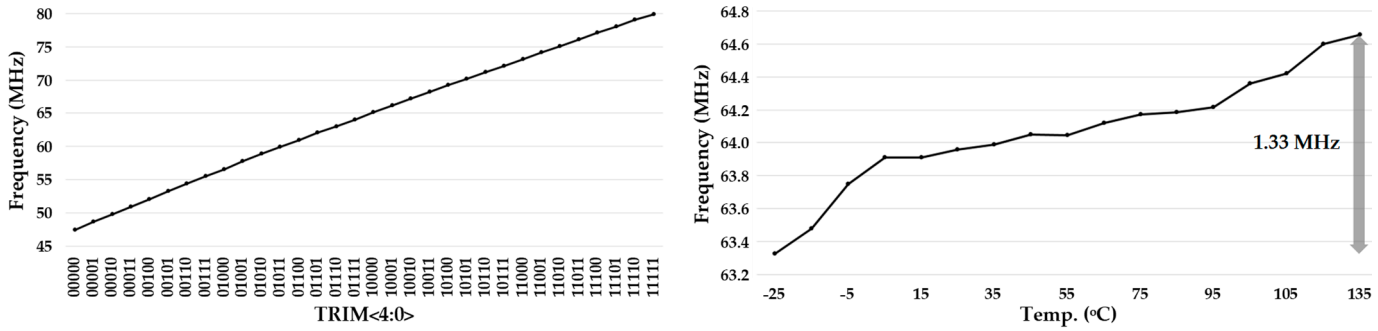


Figure 9. Post-layout Monte-Carlo simulation of the proposed relaxation oscillator.



(**a**) (**b**)

Figure 10. Measurement results for the output frequency clock of the proposed relaxation oscillator (**a**) over a wide frequency range from 47.5 MHz to 80 MHz, and (**b**) over a wide temperature range from −25 °C to 135 °C.

Although there are a variety of figures of merit (FoMs) to compare the performances of oscillators, the suggested FoM in [20] generally includes all important parameters of an oscillator, such as frequency-to-power ratio, temperature range (ΔT), feature size of technology ($L_{\min}$), TC, and occupied area. Therefore, the FoM could be written using the following equations [20]:

$$\text{FoM} = 10\log\left(\frac{f_{\text{osc}}(\text{Hz}) \times \Delta T \times L_{\min}^2(\text{nm})}{P(W) \times TC \times A(\text{mm}^2)}\right) \tag{14}$$

Table 1 reports the performance summary of the proposed relaxation oscillator and compares it with other state-of-the-art designs. As indicated in Table 1, the oscillator presented in this work has a superior energy efficiency of 2.15 µW/MHz and a FoM of 175.96 dB in comparison with other similar works. The relaxation oscillator in [12] reports a higher operating frequency clock with a lower TC in a smaller occupied area. Nonetheless, the huge power consumption degrades the energy efficiency and FoM performances significantly in comparison to other oscillators. The oscillator reported in [13] consumes less power and offers a better TC; however, due to the lower operating frequency, the energy efficiency performance and FoM are degraded.

Table 1. State-of-the-art performance summary and comparison.

Parameter	This Work †	[12] †	[13] †	[16] †	[17] †	[20] †	[21] ‡
Tech. (nm)	90	5	180	180	180	130	180
Approach	Relaxation oscillator	Relaxation oscillator	Relaxation oscillator	Switched capacitor	Inverter-based RC	Relaxation oscillator	CDS-like
Supply (V)	1.2	1.2	1.1–2	1.2	1.8	2.5	1.8
Freq. (MHz)	64	77	1.02	13.4	18.13	1	10
Power (µW)	138	840	5.72	157.8	245.7	428	91.44
Energy Efficiency (µW/MHz)	2.15	10.9	5.6	11.77	13.55	428	9.14
Temp. Range (°C)	−25–135	−40–125	−40–125	−20–100	N.A.	25–200	N.A.
Temp. Coeff. (ppm/°C)	130	36.36	59	193.15	N.A.	108	20.8
Area (mm^2)	0.0117	0.0077	0.0513 *	0.039 *	0.056	0.007	N.A.
FoM (dB)	175.96	151.3	175	166.4	N.A.	160	N.A.

† Measurement results, ‡ Post-layout simulation results, * Estimated area occupation from die photo.

The relaxation oscillator in [20] provides an output clock frequency for high-temperature applications up to 200 °C with the smallest occupied area in comparison with other oscillators in Table 1. However, the oscillator dissipates a huge amount of power and offers the worst energy efficiency performance in comparison with other works. The CDS-like oscillator in [21] presents a superior TC of 20.8 ppm/°C in comparison with other works. Nevertheless, the post-layout simulation results show a greater amount of energy efficiency in comparison with the proposed oscillator in this paper and [12,13].

The operation frequency and power consumption define the energy efficiency performance of an oscillator. Moreover, both power consumption and operating frequency have the largest contributions to FoM performance. Consequently, a structure with a high operation frequency and low power consumption could provide better energy efficiency and FoM performances. Energy efficiency and FoM performances are significantly improved by using a single comparator to generate the output clock.

6. Conclusions

In this article, the fully integrated relaxation oscillator is analyzed and implemented in 90 nm CMOS process with a die area of 130 µm × 90 µm. The energy efficiency of 2.15 µW/MHz is obtained to generate the output clock of 64 MHz, whereas the TC of 130 ppm/°C is achieved for a wide temperature range from −25 °C to 135 °C. The superior energy efficiency and FoM performances are achieved by using a single comparator

structure to generate the output clock. According to the measurement results, the oscillator offers a dynamic frequency range of 47.5 MHz to 80 MHz with a resolution of 1 MHz by 32 steps. Moreover, the duty cycle of the output clock is compensated for 50% ± 5% by employing an auxiliary comparator.

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References

1. Razavi, B. *RF Microelectronics*; Prentice Hall: Upper Saddel River, NJ, USA, 2011.
2. Asl, S.A.H.; Rad, R.E.; Rikan, B.S.; Pu, Y.; Hwang, K.C.; Yang, Y.; Lee, K.-Y. A 1.8–2.7 GHz Triple-Band Low Noise Amplifier with 31.5 dB Dynamic Range of Power Gain and Adaptive Power Consumption for LTE Application. *Sensors* **2022**, *22*, 4039. [CrossRef] [PubMed]
3. Rikan, B.S.; Kim, D.; Choi, K.-D.; Asl, S.A.H.; Yoo, J.-M.; Pu, Y.; Kim, S.; Huh, H.; Jung, Y.; Lee, K.-Y. A Low-Band Multi-Gain LNA Design for Diversity Receive Module with 1.2 dB NF. *Sensors* **2021**, *21*, 8340. [CrossRef] [PubMed]
4. Hejazi, A.; Rikan, B.S.; Asl, S.A.H.; Lee, K.-Y. A Sub-1-mW Fractional-N Phase-Locked Loop For Mixer-Based Wake-up Receiver. In Proceedings of the Wireless Sensors. International SoC Design Conference (ISOCC), Yeosu, Republic of Korea, 21–24 October 2020; pp. 220–221. [CrossRef]
5. Everard, J.; Burtichelov, T.; Ng, K. Ultralow Phase Noise 10-MHz Crystal Oscillators. *IEEE Trans. Ultrason. Ferroelectr. Freq. Control.* **2018**, *66*, 181–191. [CrossRef] [PubMed]
6. Abbasizadeh, H.; Rikan, B.S.; Lee, K.-Y. A fully on-chip 25MHz PVT-compensation CMOS Relaxation Oscillator. In Proceedings of the IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC), Daejeon, Republic of Korea, 5–7 October 2015; pp. 241–245. [CrossRef]
7. Paidimarri, A.; Griffith, D.; Wang, A.; Burra, G.; Chandrakasan, A.P. An RC Oscillator With Comparator Offset Cancellation. *IEEE J. Solid-State Circuits* **2016**, *51*, 1866–1877. [CrossRef]
8. Liao, Y.; Chan, P.K. A 1.1 V 25 ppm/°C Relaxation Oscillator with 0.045%/V Line Sensitivity for Low Power Applications. *J. Low Power Electron. Appl.* **2023**, *13*, 15. [CrossRef]
9. Tsubaki, K.; Hirose, T.; Kuroki, N.; Numa, M. A 32.55-kHz, 472-nW, 120 ppm/°C, fully on-chip, variation tolerant CMOS relaxation oscillator for a real-time clock application. In *Proceedings of the 2013 Proceedings of the ESSCIRC (ESSCIRC), Bucharest, Romania, 16–20 September 2013*; pp. 315–318. [CrossRef]
10. McCorquodale, M.S.; Pernia, S.M.; O'Day, J.D.; Carchner, G.; Marsman, E.; Nguyen, N.; Kubba, S.; Nguyen, S.; Kuhn, J.; Brown, R.B. A 0.5-to-480 MHz Self-Referenced CMOS Clock Generator with 90ppm Total Frequency Error and Spread-Spectrum Capability. In Proceedings of the IEEE International Solid-State Circuits Conference-Digest of Technical Papers, San Francisco, CA, USA, 3–7 February 2008; pp. 350–619. [CrossRef]
11. Sundaresan, K.; Allen, P.E.; Ayazi, F. Process and temperature compensation in a 7-MHz CMOS clock oscillator. *IEEE J. Solid-State Circuits* **2006**, *41*, 433–442. [CrossRef]
12. Mehta, N.; Tell, S.; Turner, W.; Tatro, L.; Goh, G.; Gray, C.T. A 77 MHz Relaxation Oscillator in 5 nm FinFET with 3 ns TIE over 10 K cycles and ±0.3% Thermal Stability using Frequency-Error Feedback Loop. In Proceedings of the 2021 IEEE Asian Solid-State Circuits Conference (A-SSCC), Busan, Republic of Korea, 7–10 November 2021; pp. 1–3. [CrossRef]
13. Chen, C.; Zhan, C.; Zhang, Z.; Zhang, N.; Wang, L. A 5.72-μW, 1.02-MHz, −40~125 °C, 1 μs-Startup Time Relaxation Oscillation with Fully-on-Chip Voltage Reference and LDO Regulator. In Proceedings of the 2021 IEEE International Conference on Integrated Circuits, Technologies and Applications (ICTA), Zhuhai, China, 24–26 November 2021; pp. 237–238. [CrossRef]
14. Sebastiano, F.; Breems, L.; Makinwa, K.; Drago, S.; Leenaerts, D.; Nauta, B. A low-voltage mobility-based frequency reference for crystal-less ULP radios. In Proceedings of the ESSCIRC 2008-34th European Solid-State Circuits Conference, Scotland, UK, 15–19 September 2008; pp. 306–309. [CrossRef]

15. Asl, S.A.H.; Lee, K.-Y. A 18.05 ppm/°C, 38.5 uW Bandgap Reference Based on Weak Inversion Region Operation Design. In Proceedings of the 2022 29th IEEE International Conference on Electronics, Circuits and Systems (ICECS), Glasgow, UK, 24–26 October 2022; pp. 1–4. [CrossRef]
16. Chang, Y.-A.; Liu, S.-I. A 13.4-MHz Relaxation Oscillator With Temperature Compensation. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2019**, *27*, 1725–1729. [CrossRef]
17. Ko, J.; Lee, M. A 1.8 V 18.13 MHz Inverter-Based On-Chip RC Oscillator with Flicker Noise Suppression Using Logic Transition Voltage Feedback. *Electronics* **2019**, *8*, 1353. [CrossRef]
18. Asl, S.A.H.; Rikan, B.S.; Hejazi, A.; Pu, Y.; Huh, H.; Jung, Y.; Hwang, K.C.; Yang, Y.; Lee, K.-Y. A Design of Analog Front-End with DBPSK Demodulator for Magnetic Field Wireless Network Sensors. *Sensors* **2022**, *22*, 7217. [CrossRef] [PubMed]
19. Qian, X.; Teo, T.H. A low-power comparator with programmable hysteresis level for blood pressure peak detection. In Proceedings of the TENCON 2009—2009 IEEE Region 10 Conference, Singapore, 23–26 January 2009; pp. 1–4. [CrossRef]
20. Sadeghi, N.; Sharif-Bakhtiar, A.; Mirabbasi, S. A 0.007-mm^2 108-ppm/°C 1-MHz Relaxation Oscillator for High-Temperature Applications up to 180 °C in 0.13-µm CMOS. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2013**, *60*, 1692–1701. [CrossRef]
21. Gagliardi, F.; Manfredini, G.; Ria, A.; Piotto, M.; Bruschi, P. Low-Phase-Noise CMOS Relaxation Oscillators for On-Chip Timing of IoT Sensing Platforms. *Electronics* **2022**, *11*, 1794. [CrossRef]