# A 65-nm-CMOS 100-MHz 87%-efficient DC-DC down converter based on dual-die system-in-package integration

# A 65-nm-CMOS 100-MHz 87%-efficient DC-DC down converter based on dual-die System-in-Package integration

Henk Jan Bergveld, Katarzyna Nowak, Ravi Karadi
NXP Semiconductors, Research, High Tech Campus 32, 5656AE, Eindhoven, the Netherlands
HenkJan.Bergveld@nxp.com

Sebastien Iochem, Jorge Ferreira, Sophie Ledain, Eric Pieraerts, Mickael Pommier
NXP Semiconductors, 2 Rue de la Girafe, Caen Cedex, 14096, France

***Abstract* -- The increasing number of efficient voltage conversions realized in small volumes in many applications has introduced a trend towards small-form-factor DC-DC converters with integrated passives. Preferably, the DC-DC converter is integrated with the load, often in nm-CMOS, allowing for local supply optimization yielding increased power efficiency. However, energy-storage densities in nm-CMOS are low and silicon area is expensive. Therefore, to limit cost of monolithically integrated systems, passive components have low values, leading to very high switching frequencies, which compromises efficiency. This paper follows an alternative approach, where the active converter part is realized in 65-nm CMOS and the passive part in a low-cost high-density passive-integration process. With the active die flip-chipped on the passive die a small System-in-Package (SiP) is obtained with a peak efficiency of 87.5% at 100 MHz switching frequency and 85 mW output power. This performance is mainly caused by the high quality of the integrated passives.**

***Index Terms*—DC-DC power conversion, Microassembly, Packaging, Pulse width modulated power converters, Passive circuits, CMOS integrated circuits**

## I. INTRODUCTION

In many applications there is an increasing demand for efficient voltage converters that can be accommodated in a small volume. Examples are portable devices, which become smaller while hosting an increasing number of features and associated voltage conversions, and automotive applications, where particularly in the dashboard the number of electronic functions including local supplies increases in a limited space. This has led to a trend towards small-form-factor DC-DC converters with integrated passive components. In many cases, these small converters are inductive DC-DC converters as their output voltage can be more easily controlled over line and load variations than in case of capacitive DC-DC converters, and only one inductor and two capacitors are needed. Integration of the passive components into the package always implies relatively small component values of the passives compared to DC-DC converters with external passive components, regardless of the technology used. Therefore, the converter switching frequency needs to increase leading to a lower peak efficiency due to increased switching losses.

The integration of a DC-DC converter is especially useful when local supply generation is needed, for example in voltage-scaling techniques for digital ICs [1]. The IC is then divided into independent voltage islands, each of which is powered by an individual power supply with an output voltage that minimizes power consumption of the supplied voltage island. In practice, in such applications DC-DC down converters are used with output powers in the range of 100-400 mW. Since digital ICs are mostly realized in nm-CMOS processes with ever decreasing feature sizes, the integrated DC-DC converter also needs to be realized in the same nm-CMOS IC process.

Several approaches can be distinguished to integrate the DC-DC converter with the load. In the first approach, the DC-DC converter is monolithically integrated with the load in standard nm-CMOS. Since silicon area is expensive in state-of-the-art nm-CMOS processes and energy-storage densities are limited, particularly the on-chip inductor will have a low inductance value and switching frequencies will be high. Examples can be found in [2], where a switching frequency of 660 MHz in 180-nm CMOS leads to a peak efficiency of only 30%, and in [3], where a switching frequency of 170 MHz in 130-nm CMOS achieves a peak efficiency of 78% based on a 2-phase interleaved concept.

In the second approach, non-standard CMOS is used for monolithic integration. For example, 180-nm SiGe with additional top copper metallization is used leading to 64% peak efficiency at 65-MHz switching frequency [4], or standard CMOS with a MEMS post-processed Plastic Deformation Magnetic Assembly (PDMA) inductor is used leading to a peak efficiency below 60% at 10 MHz [5],[6]. The needed input and output capacitors, although claimed to be realizable with similar technology as for the coils, are in the tens of nF range and still take up considerable relatively expensive CMOS silicon area. In a series of papers, DC-DC down converters with post-processed thin-film inductors based on amorphous CoZrTa alloy are predicted to allow efficiencies between 80 and 88% with switching frequencies around 100 MHz. However, again the area-consuming input and output capacitors with values up to 100 nF are assumed to be realized in expensive nm-CMOS processes [7]-[9]. Using a thin-film post-processed inductor with CoHfTaPd magnetic layers achieves 83% efficiency at 3-MHz switching frequency [10]. In this case, high-value (1 μF) external SMD input and output capacitors are used.

In the third approach, the passives are realized in a (mixture of) different technology(ies) leading to optimum implementation. For example, off-chip SMD air-core inductors and on-chip capacitors are used in [11],

implementing an 8-phase interleaved DC-DC converter in 90-nm CMOS running at 233 MHz with a peak efficiency of 83%. Using ferrite as a substrate for a solenoid inductor on which the power IC is mounted to form a Chip-Size Module (CSM) achieves 93% efficiency at roughly 1-MHz switching frequency [12]. As in [10], external SMD input and output capacitors are used.

This paper follows an alternative approach, where all passives are realized in a low-cost high-density passive-integration IC process [13]-[15], and the active die is flip-chipped on top of the passive die [16]-[18]. The high capacitance density yields a relatively small area for high-value input and output capacitors. The relatively large area of the planar air coil on the same die is not a problem, since the silicon-area cost in the passive IC process is low. In contrast to the first demonstrator described in [16], the active die has been realized in 65-nm CMOS, in line with the state-of-the-art load circuits, and efficiency has been dramatically improved.

Specifications for the integrated DC-DC converter are derived in section II. Moreover, details on the active-die design are given. Section III briefly describes the used passive-integration process, as well as the design of the passive die and the DC-DC converter assembly process. Measurement results are given in section IV. Finally, conclusions are drawn in section V.

## II. DC-DC CONVERTER SPECIFICATIONS AND ACTIVE-DIE DESIGN

### A. Integrated Power Management

The supply voltage in 65-nm CMOS is limited to 1.2 V. It is assumed that the source voltage of the energy supply, e.g. a Li-ion battery, is first down-converted to 1.2 V centrally in the system using an appropriate IC technology. This is schematically depicted in Fig. 1. The central DC-DC converter is assumed to power a digital IC, sub-divided into several voltage islands and realized in 65-nm CMOS. Local voltage down conversion on the digital IC from $V_{in}$=1.2 V to the supply voltage needed by the voltage island is realized either by an integrated DC-DC down converter or by a Low-DropOut linear voltage regulator (LDO). The use of either an integrated DC-DC converter or an LDO depends on the power required by the digital core on the voltage island and its silicon area. For low-silicon-area voltage islands with associated low power levels using an LDO may lead to the optimum efficiency-cost trade-off. The output voltage of the integrated DC-DC converter is assumed to be controllable in small steps between 0.7 V (minimum voltage to retain flip-flop states) and 1.2 V. A control block controls the DC-DC converter or LDO in each voltage island to obtain the desired performance of the digital core. The highlighted DC-DC converter powering voltage island 1 in Fig. 1 is the design target in this paper.

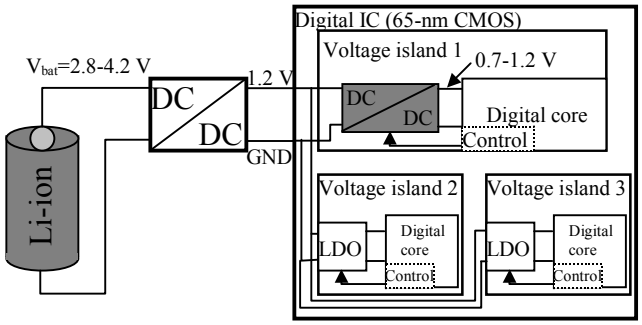


Fig. 1. Block diagram of a battery-powered system with integrated power management. The highlighted DC-DC converter is the design target

### B. Design Choices

A simple buck topology has been chosen to realize the targeted integrated DC-DC converter and optimized for $V_{out}$=0.85 V and an output current $I_{out}$ of 100 mA. This $V_{out}$ value is halfway between 0.7 V and 1 V. Above 1 V a bypass switch is used to improve efficiency. The current consumption of 100 mA is assumed typical for a voltage island containing a digital core. A maximum switching frequency $f_s$ of 100 MHz has been chosen as a practical limit, as higher frequencies make dealing with parasitics more difficult. Consequently, continuous conduction mode was selected for simplicity. Closed-loop control has not been implemented in the converter itself. Instead, a 5-bit digital duty-cycle input code is used to control the converter duty cycle. This would allow for the use of the DC-DC converter in a voltage-scaling control loop. An example is given in Fig. 1, where the output of the control block situated in the digital core can be a duty cycle value leading to a corresponding supply voltage that ensures the desired digital-core performance. The schematic of the integrated DC-DC converter is shown in Fig. 2.

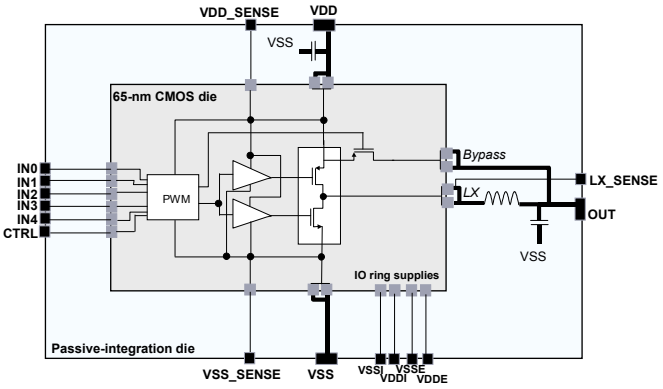


Fig. 2. Block diagram of the realized two-die integrated DC-DC converter

The duty-cycle control input signals IN0-IN4 control the duty cycle between 50% and 100%. Duty cycles below 50%

are not needed due to the minimum output voltage of the DC-DC converter of 0.7 V. The CTRL input can be used to externally control $f_s$ for analysis and test purposes. The PWM block generates a square-wave signal with frequency $f_s$ and the programmed duty cycle $D$. The power connections VDD, VSS, LX and OUT have been implemented using double bump pads both on the active and the passive die to lower the series impedance. Sense lines have been implemented to monitor the internal supply lines and the LX node to investigate the switching waveforms. The bypass switch is used to bypass the converter at high duty-cycle values.

### C. High-Level Optimization and Design Implementation

The active-die design has been optimized for the above-mentioned specifications by performing design-space exploration using a high-level first-order Matlab model of the converter working in continuous conduction mode. The high-level model calculates the converter efficiency as a function of the specifications ($V_{in}$, $V_{out}$, $I_{out}$), technology parameters (capacitance and resistance for a 1-µm width and minimum-length unit-area power NMOST and PMOST in 65-nm CMOS and $L/R$ ratio estimate for the used planar air-core inductor as a function of frequency), design parameters (inductance $L$ and $f_s$), and applied switch driving method (Hard Switching, HS, or Zero-Voltage Switching, ZVS). The choice for either HS or ZVS impacts the equivalent switching capacitance of the power MOSTs. In the case of ZVS, part of the switching capacitance is charged/discharged via the inductor current, leading to an effectively lower equivalent switching capacitance and associated lower switching losses [16].

For each set of design parameters ($L$, $f_s$) and for a chosen switch driving method (HS or ZVS) the optimum power-switch sizes are calculated by minimizing the total power-switch losses. Since switch conduction losses ($I^2R$) decrease with increasing switch area and switching losses ($fCV^2$) increase with increasing switch area, the optimum switch size is found when the switch conduction and switching losses are equal. The used equations for optimum width of the NMOST and PMOST are identical to those in [7],[8]. Taking the inductor conduction losses into account, the total losses, and therefore the converter efficiency, can now be calculated. Note that the model is only a first-order model. For example, overlap losses (simultaneous non-zero current through and voltage across power switches when switching on or off) and body-diode conduction losses have not been included. Moreover, the impact of voltage drop across the power switches and inductor on the actual duty-cycle value as taken into account in [19] has also been neglected. However, as will be shown in section IV, the eventual measurement results, where all effects not taken into account occur, are rather close to the results predicted by the design-space exploration.

The result of the performed design-space exploration for the HS DC-DC down converter with $V_{in}$=1.2 V, $V_{out}$=0.85 V and $I_{out}$=100 mA is shown in Fig. 3. With the practical limit of the switching frequency set at 100 MHz as mentioned above, the optimum efficiency of 88.9% was achieved at an inductance of 10.1 nH. The corresponding power switch widths were found to be 2998 µm for the NMOST and 7786 µm for the PMOST. Note that a larger switching frequency improves efficiency. This is mainly caused by the lower inductance that can be used and its associated lower series resistance. This effect more than compensates for the increase in switching losses due to the increased value of $f_s$.

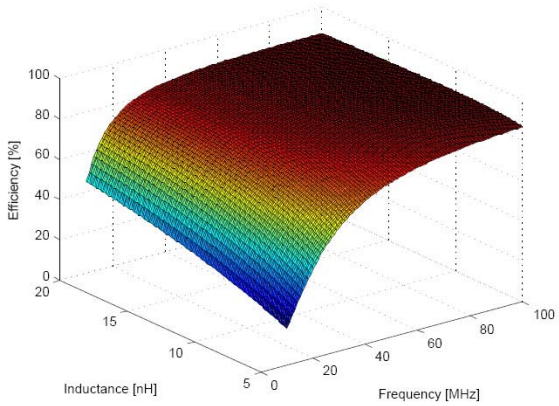


Fig. 3. Result of design-space exploration for a HS DC-DC converter

In a similar plot for the ZVS case, a peak efficiency of 90.5% was found at $f_s$=100 MHz and $L$=9.4 nH. Hence, the peak efficiency is only 1.6% higher compared to HS. The main reason is the rather low supply voltage of 1.2 V, leading to a relatively small effect on reduction in switching losses ($fCV^2$). Moreover, in the case of ZVS, the reduction in the equivalent switching capacitance assuming ideal ZVS implementation was taken into account, where the power MOSTs switch on exactly at the moment when the drain-source voltage has become zero. This is very hard to achieve in practice. Therefore, a practical ZVS implementation will lead to an even lower efficiency improvement. Therefore, we chose to implement a HS power stage, where cross conduction was prevented using a hand-shaking Break-Before-Make (BBM) scheme illustrated in Fig. 4a. Each driver section comprises three stages. Based on simulations it was found that the most power-efficient implementation of the hand-shaking procedure resulted from placing the associated logic in the second driver stage.

The area of the bond-pad limited active die is 754 µm x 754 µm in 65-nm CMOS. Significant effort was spent on reducing the resistance of the connections of the power MOSTs to the bump pads compared to the design described in [16]. The active-die layout is shown in Fig. 4b.

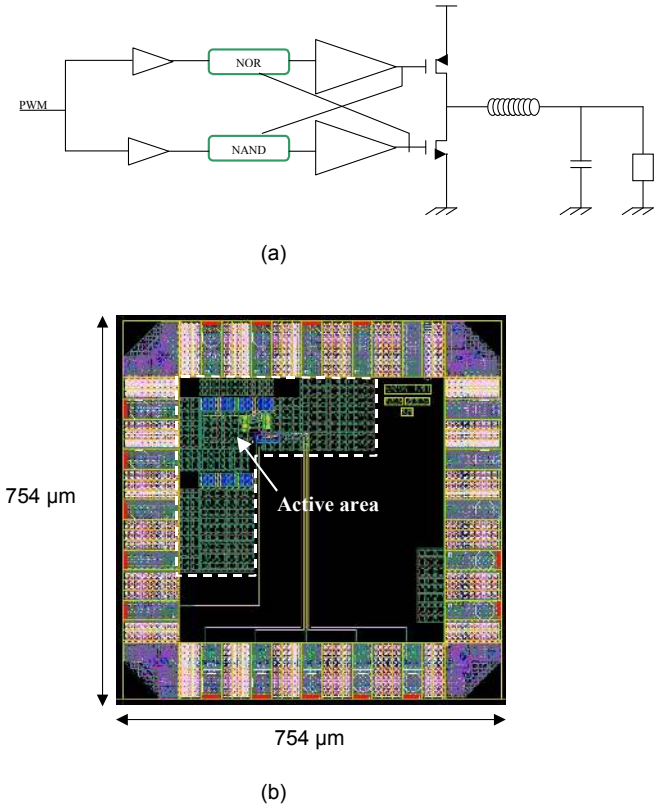


Fig. 4. (a) Schematic implementation of the hand-shaking BBM scheme, (b) Active-die layout

## III. PASSIVE-DIE DESIGN AND SIP ASSEMBLY

### A. *Passive-Integration Technology*

The passive die was designed in the Passive-Integration Connective Substrate (PICS) process [13]-[18]. The PICS process was developed in NXP Semiconductors to integrate passive components such as high-Q inductors, resistors, accurate MIM capacitors, and, in particular, high-density (~30 nF/mm$^2$) MOS 'trench' capacitors for decoupling and filtering. These were fabricated in silicon by dry-etching arrays of high-aspect-ratio macro pores with diameter and spacing of the order of approximately 1 µm, and up to roughly 30 µm in depth. Capacitors were made by filling the pore arrays with an approximately 30-nm thick silicon oxide/nitride/oxide ('ONO') dielectric layer stack followed by a roughly 0.7-µm thick in-situ phosphorus-doped poly-Si top electrode. The next generation of trench or 'pillar' capacitors has been qualified for ~80 nF/mm$^2$ by using thinner (~16 nm) oxy-nitride dielectrics with a breakdown voltage of 15.5 V [15]. These capacitors have been used for the integrated DC-DC converter described here. A schematic overview of the process is given in the form of a cross section in Fig. 5 [15]. The basic substrate topology is a 3D trench array (actually a pillar array) with aspect ratio of around 20, as shown in Fig. 6a. This structure is then filled up by the oxy-nitride layer and the doped poly-Si layer, most of the layers being deposited by Low-Pressure Chemical Vapor Deposition (LPCVD). This structure (see Fig. 6b for a top view) is then capped with a Physical Vapor Deposition (PVD) metal electrode layer. After oxide deposition a second metal layer is formed from which inductors can be patterned. An 8-µm thick copper layer was used for this purpose in this study to allow the design of a planar air-core inductor with acceptable series resistance.

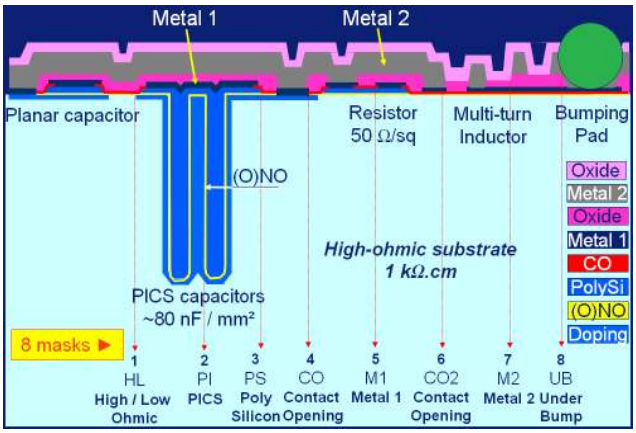


Fig. 5. Schematic cross section of a PICS wafer including multi-turn inductor, planar MIM and high-density 'trench' MOS capacitors, poly-Si resistors, two metal layers and bumping pad. The eight mask steps are shown on the right-hand side [15]

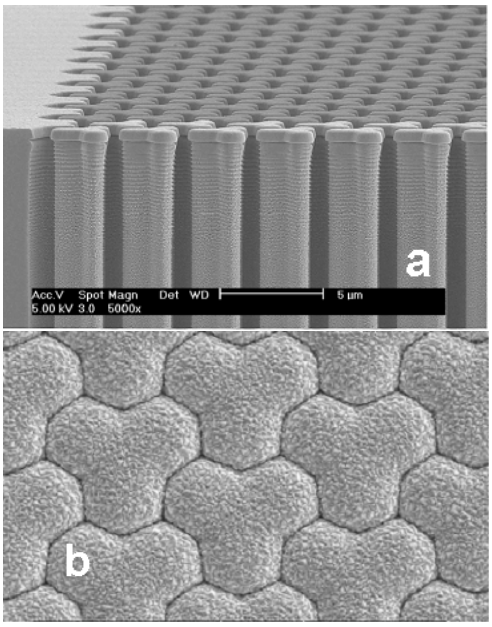


Fig. 6. Capacitor images: (a) side view of a 3D trench-array after Reactive Ion Etching (RIE) and (b) top view after filling with a MOS capacitor stack [18]

### B. *Passive-Die Design*

The input decoupling capacitor was designed to be 21 nF,

the largest part being placed underneath the active die with the remaining part directly beside it. The value was obtained after performing simulations including extracted parasitics on the active and passive dies as well as an equivalent electrical model of the used package. The output capacitor was designed to be 30 nF, yielding a calculated output ripple of 12.5 $mV_{pp}$ with the 10.1-nH inductor. Applying the main lesson learned from [16], the output capacitor was placed outside of the inductor. The octagon-shaped inductor has three turns with a width of 50 µm and a minimum spacing of 8 µm. The inductor area is 1 $mm^2$ and a stand-alone version along with other characterization structures was placed elsewhere on the passive wafer for characterization purposes. A photograph of the manufactured passive die before dicing is shown in Fig. 7a.

### C. SiP Assembly of the Integrated DC-DC Converter

The passive die measures 4.8 x 4.8 $mm^2$ to fit the smallest HVQFN40 package that was readily available in the used pilot line. The active die was bumped and flip-chipped upside-down on the passive die, see Fig. 7b. Then, as a next step double flip-chip was applied to reduce the series impedance even further, see Fig. 7c. In this step bumps were placed on the passive die and the sandwich was connected upside-down on the package lead frame. The finished HVQFN40 package is shown in Fig. 7d. A future passive-die size reduction is certainly possible, as many of the 40 pads on the passive die needed to accommodate the lead frame of the used HVQFN40 package are dummy pads and also relatively large empty spaces are still present on the passive die, see Fig. 7a.

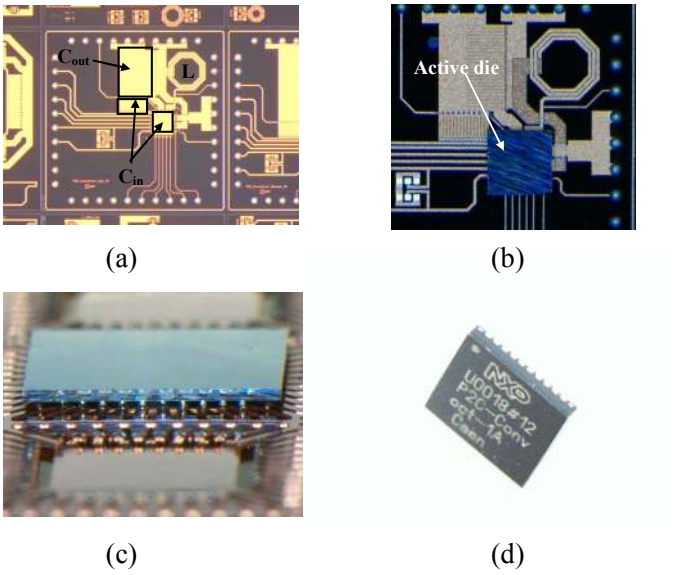


Fig. 7. (a) Passive die before dicing, (b) Active die flip-chipped on passive die, (c) Sandwich double-flip-chipped on HVQFN40 lead frame, (d) HVQFN40 package including two-die sandwich

## IV. Measurement Results and Analysis

### A. Wafer-Level Probing Results for Planar Air Coil

The measured inductance $L$ and resistance $R$ of the stand-alone inductor as a function of frequency measured by means of wafer probing are shown in Fig. 8. Compared to the results for the planar air-core inductor in [16], the series resistance $R$ of the inductor at 100 MHz has been considerably reduced by moving the output capacitor to the outside of the inductor, see also Fig. 7a. The measured inductance $L$ has been corrected for the roughly 1-nH inductance in the ground lead of the characterization structure. At 100 MHz, an $L$ value of 11 nH and an $R$ value of 0.56 Ω have been measured. The measured $L$ is slightly higher than simulated with Momentum in the design phase (10.3 nH) since the characterization structure has been measured on the standard-thickness wafer for practical reasons, whereas in Momentum the thinner thickness of 200 µm applicable in the SiP has been used. A thinner wafer brings the planar coil closer to the ground plane hence slightly reducing its inductance at higher frequencies. The measured $R$ value at 100 MHz is in line with the simulated value obtained with Momentum at 100 MHz (0.52 Ω). The resonance frequency is clearly above 1 GHz.

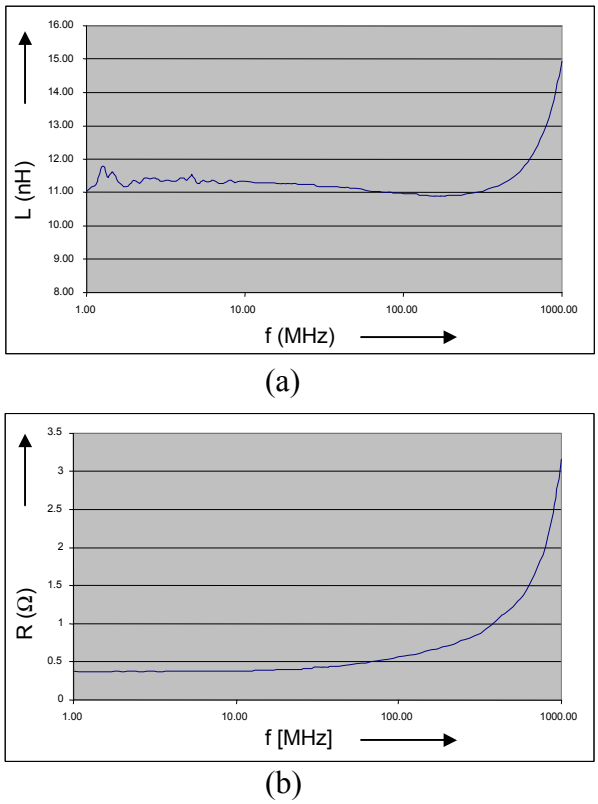


Fig. 8. (a) Measured inductance $L$ (nH), and (b) measured resistance $R$ (Ω) as a function of frequency $f$ (MHz) for the stand-alone inductor characterization structure obtained by wafer probing

## B. *Measurement Set-Up*

A photograph of the used PCB is shown in Fig. 9. In addition to the HVQFN40 package containing the dual-die integrated DC-DC converter shown in the middle, the other components on the PCB are merely needed for testing. On the left-hand side, a fixed resistor or variable resistor can be used as a load. On the right-hand side, 5 pull-up resistors and switches are used to program the 5-bit duty-cycle input code. On the bottom-right hand side, a variable resistor to ground is used to vary the switching frequency $f_s$. The input voltage $V_{in}$ of 1.2 V needs to be connected at the bottom. Finally, a separate ring supply can be connected at the top for analysis purposes and the resistance of the bumps used in the double flip-chip process can be measured.

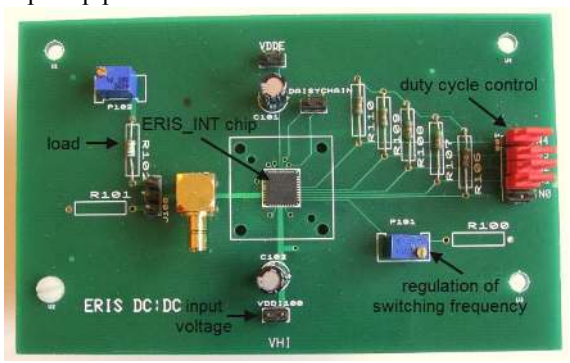


Fig. 9. PCB used for measurements with integrated DC-DC converter

## C. *Measurement Results of Integrated DC-DC Converter*

The measured efficiency versus output current $I_{out}$ is shown in Fig. 10 for various (a) $V_{out}$ and (b) $f_s$ values, where $V_{out}$ was kept constant over the entire $I_{out}$ range by manually adjusting the duty cycle via the 5-bit duty-cycle code. At $V_{out}$=0.85 V, the peak efficiency is 85.6% at $I_{out}$=80.6 mA. Both the peak efficiency and optimum $I_{out}$ value are somewhat lower than predicted by the high-level modeling step, since the total series impedance including package has been slightly underestimated in the high-level modelling process. However, even though the used high-level model is only first order, its predicted results are still close to the measured results and it has been useful to guide the design process. The peak efficiency of 87.5% is achieved at $V_{out}$=0.95 V, $I_{out}$=90 mA and $f_s$=100 MHz.

Further inspection of Fig. 10 shows that at the same DC output current $I_{out}$, the efficiency is higher for higher $V_{out}$ values. A probable reason is that the output power increases for higher $V_{out}$ values, while ripple-current losses decrease due to a lower peak-to-peak current ripple (at $D$>50% the peak-to-peak ripple current decreases as function of increasing $V_{out}$). At low output current values, the efficiency increases for higher $f_s$ values. Apparently, current-ripple losses are dominant here and these losses decrease significantly at higher $f_s$ values while switching losses increase to a lower extent, leading to a net increase in efficiency.

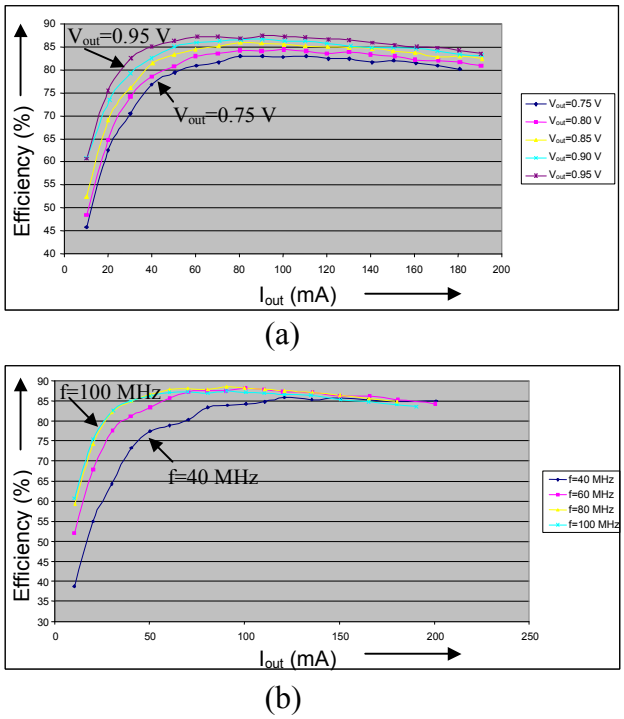


Fig. 10. Measured efficiency (%) as a function of $I_{out}$ (mA): (a) for various $V_{out}$ values at $f_s$=100 MHz, (b) for various $f_s$ values at $V_{out}$=0.95 V, peak efficiency of 87.5% is achieved at $f_s$=100 MHz and $I_{out}$=90 mA

The measured efficiency of the DC-DC converter at $I_{out}$=100 mA and that calculated as $V_{out}/V_{in}$ for a linear regulator (LDO) are shown in Fig. 11. Clearly, the efficiency for the realized integrated DC-DC converter at $I_{out}$=100 mA is higher than that obtained with a linear regulator over most of the output voltage range. This makes the use of an integrated DC-DC converter as developed in this paper instead of a linear regulator to supply a voltage island in a digital IC an attractive solution to achieve power savings.

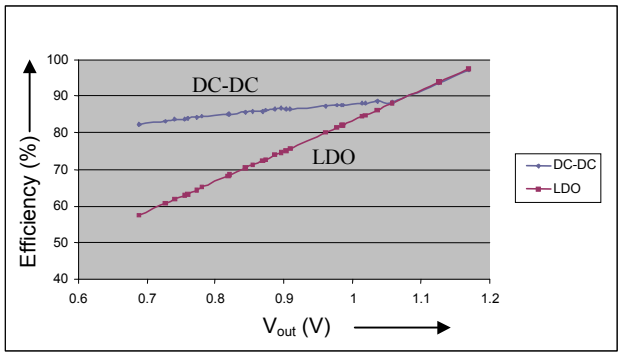


Fig. 11. Measured efficiency (%) of integrated DC-DC converter at $I_{out}$=100 mA and $f_s$=100 MHz, and calculated linear-regulator efficiency ($V_{out}/V_{in}$) as a function of $V_{out}$ (V)

The switching waveform at the LX node is shown in Fig.

12 for $f_s$=100 MHz and $I_{out}$=100 mA. The peak-to-peak amplitude is slightly lower than 1.2 V around the DC value (output voltage) of 0.7 V due to a parasitic inductive voltage division between the internal LX node and the external measurement input of the used oscilloscope. Only measurement noise and no parasitic LC oscillation can be distinguished, indicating the effectiveness of the power-supply decoupling on the passive die.

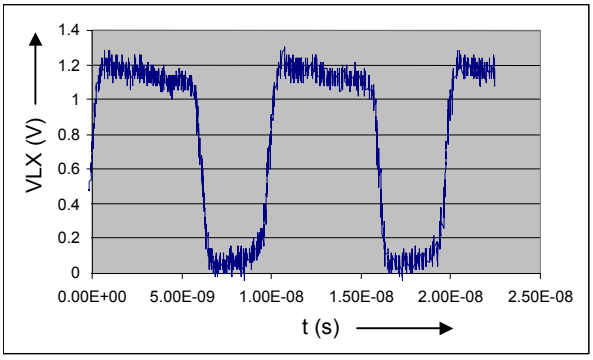


Fig. 12. Measured LX-node voltage $V_{LX}$ (V) versus time $t$ (s) at $f_s$=100 MHz and $I_{out}$=100 mA

### D. Outlook

The integrated DC-DC converter presented in this paper operates from $V_{in}$=1.2 V. A future version that runs directly of a Li-ion battery would be attractive, since a central DC-DC converter in the system is prevented, see Fig. 1. In [19], a high-level optimization procedure is presented that compares the maximum attainable efficiency for such an integrated DC-DC converter when using an air-core inductor or a thin-film magnetic-core inductor based on NiFe magnetic material as presented in [20]. Using such a thin-film magnetic-core inductor results in higher efficiency at the cost of higher passive silicon area [19]. The efficiency of this type of inductor is close to that obtained with commercial low-value chip inductors [20], so in case the footprint can be decreased sufficiently, this would be an attractive option for future integrated DC-DC converters. Obviously, it would impact the passive IC design process. A circuit implementation of the High-Voltage (HV) power stage directly connected to the Li-ion battery may be based on cascoding as in [9],[21], or on HV MOSTs realized in baseline nm CMOS without any additional process masks [22].

## V. Conclusions

An integrated DC-DC down converter has been realized that converts an input voltage of 1.2 V to an output voltage between 0.7 V and 1.2 V at an output current of around 100 mA. The integration is based on a two-die approach, where the 65-nm CMOS active die including power stage, drivers and duty-cycle control has been flip-chipped on a passive-integration die with the input decoupling and output LC filter. The main advantage of using a separate dedicated passive-integration die is a significantly higher capacitance density compared to monolithic integration. Therefore, the total passive silicon area is significantly lower, enabling a small footprint of the DC-DC converter, while still enabling high-value input and output capacitors for proper decoupling at high switching frequencies. The resulting sandwich has been double-flip-chipped in a small HVQFN40 package yielding an integrated DC-DC converter with a peak efficiency of 87.5% at an output voltage of 0.95 V, an output current of 90 mA, and a switching frequency of 100 MHz. This good performance results mainly from the high quality of the passives, including 8-µm thick copper metallization to obtain good planar air coils. Compared to a linear regulator, the integrated DC-DC converter is attractive in terms of power savings when used to supply power to a digital core in a voltage island in a digital IC realized in nm-CMOS, since its efficiency is significantly higher over a large output voltage range. Although the focus in this paper has been on integrated power management, alternatively, the presented two-die approach can also be applied to realize small-form-factor stand-alone DC-DC converters without any external components.

## Acknowledgment

The authors would like to thank Harish Kundur, Stefan Menten and Gerard van der Weide of NXP Semiconductors, and Bruno Allard and Nicolas Degrenne of INSA, Lyon, France, for their help in designing the active die. Ralf Pijper and Luuk Tiemeijer of NXP Semiconductors are acknowledged for their help in characterizing the passive components. Wim Besling, Catherine Bunel, and Reinout Woltjer of NXP Semiconductors are acknowledged for their efforts to enable a fast development of the demonstrator described in this paper. Finally, Patrick Smeets and Gerard Villar Piqué of NXP Semiconductors are acknowledged for useful comments on the original manuscript.

## References

[1] M. Meijer, J. Pineda de Gyvez, and R. Otten, "On-chip digital power supply control for system-on-chip applications", in *Proc. IEEE Int. Symp. Low-Power Electronics and Design*, ISPLED'05, Monterey, Ca., USA, August 8-10, 2005, pp. 311-314.

[2] M. Alimadadi, S. Sheikhaei, G. Lemieux, P. Palmer, S. Mirabbasi, and W. Dunford, "A 660MHz ZVS DC-DC converter using gate-driver charge-recycling in 0.18µm CMOS with an integrated output filter", in *Proc. IEEE Power Electronics Specialists Conference*, PESC'08, Rhodes, Greece, June 15-19, 2008, pp. 140-146.

[3] J. Wibben, and R. Harjani, "A high-efficiency DC-DC converter using 2nH integrated inductors", *IEEE J. Solid-State Circ.*, vol. 43, no. 4, pp. 844-854, April 2008.

[4] S. Abedinpour, B. Bakkaloglu, and S. Kiaei, "A 65MHz switching rate, two-stage interleaved synchronous buck converter with fully integrated output filter", in *Proc. IEEE Int. Symp. Circuits and Systems*, ISCAS'06, Kos, Greece, May 21-24, 2006, pp. 5315-5318.

[5] S. Musunuri, P.L. Chapman, J. Zou, and C. Liu, "Design Issues for Monolithic DC-DC Converters", *IEEE Tran. Power Electr.*, vol. 20, no. 3, pp. 639-649, May 2005.

[6] S. Musunuri, and P. Chapman, "Design of low power monolithic DC-DC buck converter with integrated inductor", in *Proc. IEEE Power*

*Electronics Specialists Conference*, PESC'05, Recife, Brazil, June 12-16, 2005, pp. 1773-1779.
[7] V. Kursun, S.G. Narendra, V.K. De, and E.G. Friedman, "Analysis of Buck Converters for On-Chip Integration With a Dual Supply Voltage Microprocessor", *IEEE Tran. VLSI Syst.*, vol. 11, no. 3, pp. 514-522, June 2003.
[8] V. Kursun, S.G. Narendra, V.K. De, and E.G. Friedman, "Low-Voltage-Swing Monolithic dc-dc Conversion", *IEEE Tran. CAS II*, vol. 51, no. 5, pp.241-248, May 2004.
[9] G. Schrom, P. Hazucha, J.H. Hahn, V. Kursun, D. Gardner, S. Narendra, T. Karnik, and V. De, "Feasibility of Monolithic and 3D-Stacked DC-DC Converters for Microprocessors in 90nm Technology Generation", in *Proc. IEEE Int. Symp. Low-Power Electronics And Design*, ISPLED'04, Newport Beach, Ca., USA, August 9-11, 2004, pp. 263-268.
[10] Y. Katayama, S. Sugahara, H. Nakazawa, and M. Edo, "High-Power-Density MHz-Switching Monolithic DC-DC Converter With Thin-Film Inductor", in *Proc. IEEE Power Electronics Specialists Conference*, PESC'00, Galway, Ireland, June 18-23, 2000, pp. 1485-1490.
[11] G. Schrom, P. Hazucha, F. Paillet, D. Rennie, S. Moon, D. Gardner, T. Karnik, P. Sun, T. Nguyen, M. Hill, K. Radhakrishnan, and T. Memioglu, "A 100MHz eight-phase buck converter delivering 12A in 25mm$^2$ using air-core inductors", in *Proc. IEEE Applied Power Electronics Conference*, APEC'07, Anaheim, Ca., USA, February 25-March 1, 2007, pp. 727-730.
[12] Z. Hayashi, Y. Katayama, M. Edo, and H. Nishio, "High-Efficiency DC-DC Converter Chip Size Module With Integrated Soft Ferrite", *IEEE Tran. Magn.*, vol. 39, no. 5, pp. 3068-3072, September 2003.
[13] F. Roozeboom, A. Kemmeren, J. Verhoeven, F. van den Heuvel, J. Klootwijk, H. Kretschman, T. Frič, E. van Grunsven, S. Bardy, C. Bunel, D. Chevrie, F. le Cornec, S. Ledain, F. Murray, and P. Philippe, "More than 'Moore': towards Passive and System-in-Package integration", in *Proc. of Electrochem. Soc. Symp.*, vol. 2005-8, pp. 16-31, 2005.
[14] F. Roozeboom, A. Kemmeren, J. Verhoeven, F. van den Heuvel, J. Klootwijk, H. Kretschman, T. Frič, E. van Grunsven, S. Bardy, C. Bunel, D. Chevrie, F. le Cornec, S. Ledain, F. Murray, and P. Philippe, "Passive and heterogeneous integration towards a silicon-based System-in-Package concept", *Thin Solid Films*, vol. 504, pp. 391-396, 2006.
[15] F. Roozeboom, J. Klootwijk, J. Verhoeven, F. van den Heuvel, W. Dekkers, S. Heil, J. van Hemmen, M. van de Sanden, W. Kessels, F. le Cornec, L. Guiraud, D. Chevrie, C. Bunel, F. Murray, H. Kim, and D. Blin, "ALD options for Si-integrated ultrahigh-density decoupling capacitors in pore and trench designs", *Electrochem. Soc. Trans.*, vol. 3, no. 15, pp. 173-181, 2007.
[16] H.J. Bergveld, R. Karadi, and K. Nowak, "An inductive down converter System-in-Package for integrated power management in battery-powered applications", in *Proc. IEEE Power Electronics Specialists Conference*, PESC'08, Rhodes, Greece, June 15-19, 2008, pp. 3335-3341.
[17] H.J. Bergveld, K. Nowak, and R. Karadi, "Integrated Inductive DC-DC Down Conversion for Integrated Power Management Using a Two-Die Approach", presented at *1st Int. Workshop on Power Supply on Chip*, PwrSoc'08, Cork, Ireland, Sept. 22-24, 2008.
[18] F. Roozeboom, H.J. Bergveld, K. Nowak, F. Le Cornec, L. Guiraud, C. Bunel, S. Iochem, J. Ferreira, S. Ledain, E. Pieraerts, and M. Pommier, "Ultrahigh-density trench capacitors in silicon and their application to integrated DC-DC conversion", accepted for publication at *Eurosensors XXIII*, Lausanne, Switzerland, Sept. 6-9, 2009.
[19] F. Haizoune, H.J. Bergveld, J. Popovic-Gerber, and J.A. Ferreira, "Topology Comparison and Design Optimisation of the Buck Converter and the Single-Inductor Dual-Output Converter for System-in-Package in 65nm CMOS", in *Proc. IEEE Int. Power Electronics and Motion Control Conf.*, IPEMC'09, Wuhan, China, May 17-20, 2009, pp. 295-301.
[20] R. Meere, T. O'Donnell, H.J. Bergveld, N. Wang, and S.C. O'Mathuna, "Analysis of Micro-Inductor Performance in a 20-100 MHz DC/DC Converter", in press, *IEEE Tran. Power Electr.*, Sept./Oct.2009.
[21] V. Kursun, S.G. Narendra, V.K. De, and E.G. Friedman, "High Input Voltage Step-Down DC-DC Converters for Integration in a Low Voltage CMOS Process", in *Proc. IEEE Int. Symp. Quality Electr. Design*, ISQED'04, San Jose, Ca., USA, March 24-26, 2004, pp. 517-521.
[22] A. Heringa and J. Sonsky, "Novel power transistor design for a process independent high voltage option in standard CMOS", in *Proc. IEEE Symp. Power Semiconductor Devices and IC's*, ISPSD'06, Naples, Italy, pp. 1-4, June 4-8, 2006.