A 660MHz ZVS DC-DC Converter Using Gate-Driver Charge-Recycling in 0.18µm CMOS with an Integrated Output Filter

Mehdi Alimadadi, Samad Sheikhaei, Guy Lemieux, Patrick Palmer, Shahriar Mirabbasi, William Dunford

Department of Electrical and Computer Engineering
University of British Columbia (UBC), Vancouver, Canada

***Abstract*—The design and manufacture of a prototype chip level power supply is described, with both simulated and experimental results. Of particular interest is the inclusion of a fully integrated on-chip *LC* filter. A high switching frequency of 660MHz and the design of a device drive circuit reduce losses by supply stacking, low-swing signaling and charge recycling. The paper demonstrates that a chip level converter operating at high frequency can be built and shows how this can be achieved, using zero voltage switching techniques similar to those commonly used in larger converters.**

Both simulations and experimental data from a fabricated circuit in 0.18µm CMOS are included. The circuit converts 2.2V to 0.75~1.0V at ~55mA.

I. Introduction

Current high-performance processor designs contain multi-core CPUs on a single chip. Not all of these CPU cores are fully utilized at once; therefore, some may be scaled back in clock frequency and voltage to save power according to (1). This technique is called Dynamic Voltage and Frequency Scaling (DVFS).

$$P = CV^2F \quad (1)$$

Scaling a common supply voltage is appropriate for many applications, but temporarily degrades the system performance [1]. In multi-core CPUs, multiple supply voltages are needed to operate the performance-critical cores at the highest voltage while all other cores are throttled back with DVFS. However, it is challenging to bring in and distribute several voltages on a single chip.

In this paper, a fully integrated on-chip DC-DC buck converter for localized power regulation is introduced. The challenge of the design of a fully-integrated buck converter comes from the necessity of being limited to CMOS power transistors and on-chip passive filter components so that no off-chip components are needed. A multi-MHz switching frequency results in a reduction in the filter inductor and capacitor area which allows full integration of these power supplies. To compensate for the switching power loss under high-frequency operation, low swing drivers and supply stacking techniques are used together with charge recycling of the PMOS drive chain to improve conversion efficiency. The main contribution of this work is the use of charge recycling, where excess charge from operating the PMOS gate drivers is delivered as energy to the load.

Design choices are described along with simulation results. Experimental results are presented for a converter on a chip using a 0.18µm process and operating at 660MHz. Conclusions will be drawn concerning the design and performance.

II. Circuit Design

A. Synchronous Buck Converters

A low voltage buck converter can be constructed with a CMOS inverter (Figure 1). Although body diodes exist, they are not shown as the converter is not expected to make use of them, reverse currents being taken by the MOS channels.

In advanced switch mode power converters, zero voltage switching (ZVS) operation is used to reduce dynamic power loss in switching power transistors [2]. In Figure 1, C_x includes all the parasitic capacitances at node V_{inv} including M_p and M_n drain to ground capacitances. When both M_p and M_n are off, a positive inductor current will remove charge from C_x, reducing V_{inv}, while a negative inductor current will charge C_x, increasing V_{inv}. When $V_{inv} = 0$, the M_n transistor is turned on, while when $V_{inv} = V_{DD}$, the M_p transistor is turned on. In this way, ZVS operation is achieved for both M_n and M_p transistors by independently driving their gates and allowing the inductor current to reverse.

In Figure 2, the two time periods, intervals 2 and 4, when both transistors are off are characterized as T_{delay1} and T_{delay2}, and correspond to the delay-time needed to implement ZVS operation. There are four intervals of operation:

- Interval 1 when M_p is on. During this time, the inductor current increases linearly since the voltage across it is constant. At the end of this interval, M_p is turned off in accordance with the required converter output voltage (the duty cycle).
- Interval 2 when both M_p and M_n are off. The charge that is stored in the parasitic capacitance C_x is removed by the inductor current. This results in a rapid drop of

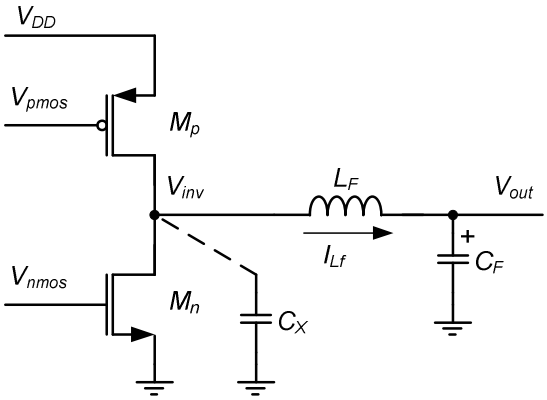

Figure 1. Block diagram of a CMOS synchronous buck converter

V_{inv}. In this short period of time, the inductor current can be assumed to be constant, as shown.

- Interval 3 starts when the voltage across M_n is close to zero. At this time the M_n is turned on under ZVS to provide a low-resistance path for the inductor current. The voltage across the inductor is constant, so the inductor current decreases linearly and by design reverses. At this point of time, M_n is turned off.
- Interval 4 when both M_p and M_n are off. Parasitic capacitance C_x is charged by the inductor current. This results in a rapid increase of V_{inv}. At the end of this interval, V_{inv} is close to V_{DD} and M_p is ready to be turned on under ZVS.

B. *Stacked Driver Design*

A significant power loss in high frequency switching is associated with the gate charge in the switching power transistors. Here, two separate inverter chains are used to drive each of the power transistors of the buck converter circuit as shown in Figure 3. The inverter chains are tapered in size using a fan-out factor of 4×, eventually achieving the required gate drive current. They are also stacked in series across the V_{DD} supply. This gives each inverter chain a lower supply voltage, reducing their power losses and resulting in low-swing operation of NMOS and PMOS to save gate power [3].

The size of the PMOS transistor M_p in Figure 3 is set to be three times the size of the NMOS transistor M_n for symmetrical operation. Consequently, the chain to drive M_p is similarly three times larger than the bottom chain, which is optimized to drive M_n. Since the PMOS chain is larger, a significant amount of charge accumulates in the middle capacitor C_m which should operate near $V_{DD}/2$.

C. *Gate-driver Charge-recycling*

In [3], the excess charge in C_m is dissipated to V_{SS} through an additional regulator forcing node V_m to $V_{DD}/2$. Here, charge-recycling is achieved by two series diode-connected NMOS transistors, D_1 and D_2. These transistors conduct when $V_{inv} < (V_m - 2V_t)$ without a need for additional gating signals. Charge recycling occurs during intervals 2 and 4 when both M_p and M_n are off and

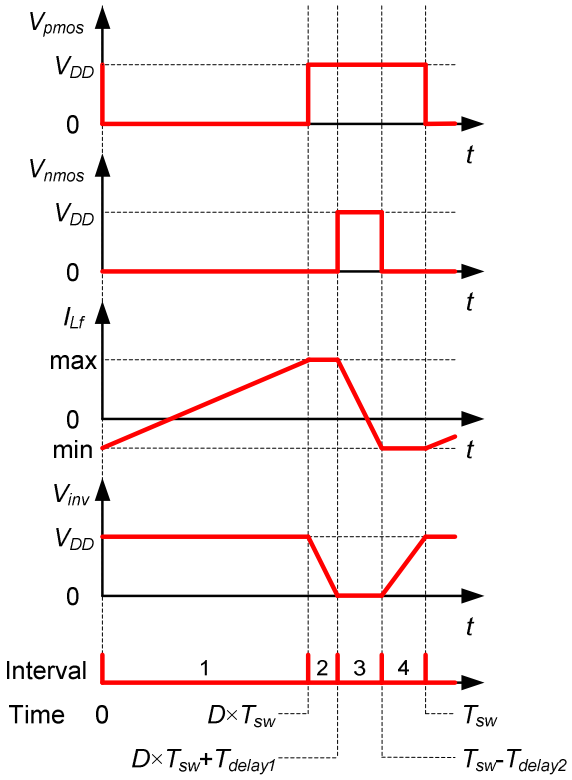

Figure 2. Idealized timing diagram of the internal signals

V_{inv} is in transition. In particular, when V_{inv} is rising there is significant charge stored on the gate of M_p that is discharged through the upper driver to the C_m node at the same time that current is drawn from this node into C_x. When V_{inv} is falling, any additional surplus charge from the PMOS drivers can also be delivered to C_x. The two diode-connected transistors in series also act as a voltage regulator for V_m when M_n is on and V_{inv} is low.

In addition negative feedback exists that ensures V_m stays around $V_{DD}/2$. If V_m is increased, the bottom chain receives a higher supply voltage, which results in increasing its power intake and causing V_m to drop. At the same time, M_n turns on with a higher V_{gs} and V_{inv} is further pulled down. Diodes D_1 and D_2 receive higher V_{gs}, facilitating removing the charge from C_m. Similarly, if V_m is decreased, the top chain receives a higher supply voltage, which results in increasing its power intake and causing V_m to increase. D_1 and D_2 receive lower V_{gs}, facilitating accumulation of charge in C_m.

Capacitance C_m was chosen to be 20 times larger than the NMOS C_{gate} to limit ripple at V_m. L_F and C_F values were chosen to be 4.38nH and 1.1nF, respectively, to operate at a switching frequency of 660MHz with a voltage ripple of less than 5% at 50mA load.

III. Implementation

A. *Integrated Passive Components*

Traditionally, magnetic materials are used in construction of inductors to confine the magnetic field

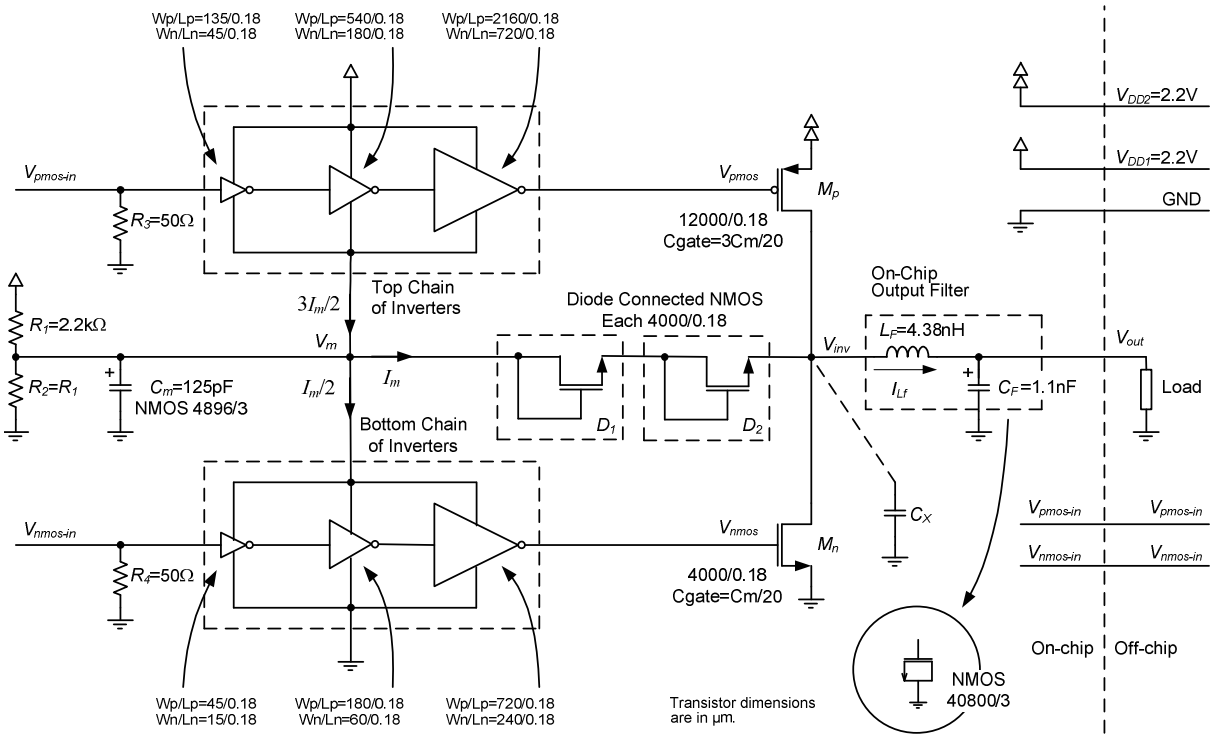

Figure 3. Circuit diagram of the implemented DC-DC converter prototype with charge-recycling diodes

close to the coil, thereby increasing the inductance. Although magnetics on silicon have been introduced before [4], this is not done here to keep the inductor design compatible with conventional CMOS process and a coreless inductor is being used.

In CMOS processes, the silicon substrate has a relatively low resistivity and eddy currents in the silicon can be considerable. As the eddy current tries to create a magnetic field that opposes the applied magnetic field, the effect of eddy currents is seen as a reduced net flux and thus a reduced inductance. Since different substrate structures have different resistivity, they will have different effects on the inductance.

Any coupled currents in the substrate will increase the substrate noise because they change the substrate voltage. Consequently, a metal Patterned Ground Shield (PGS) is placed in between the inductor coil and the substrate [5]. By using strings of ground-substrate contacts any induced current in the substrate will be shorted at regular intervals to the system ground as well. The inductor characteristics will become independent of the substrate structure and eddy currents in the substrate may also reduce. Among the different patterns that are introduced and studied in the literature, the wide bar pattern shown in Figure 4 avoids eddy current path and is used in this work [6].

Use of only higher metal layers for the inductor and the lowest metal layer for PGS will keep the inductor high up above the PGS. Excluding use of the lower metal layers for the inductor, will also reduce its stray capacitance. On the other hand, block out masks can be applied in fabrication process to keep the doping level under the spiral coil at a minimum [7].

Here the inductor L_F design is two turns of simple concentric coils implemented in the top four metal layers of the chip. The tracks include shorts along their length. The ground shield is implemented using the lowest of the six available metal layers. The current density is 0.122mA/µm^2. The value of inductance was extracted using ASITIC [8]. ASITIC is CAD tool for RF circuit design, particularly for modeling spiral inductors, transformers, capacitors in IC design and accounts for substrate coupling. The substrate plays an integral part in determining the quality factor and self-resonance frequency of such an inductor. ASITIC calculations include the electrically induced losses and coupling as well as the magnetically induced eddy current losses. Skin effect and proximity effects, or eddy currents in the metallization, are also included. The inductance extracted following optimization was found to be 4.38nH, at 660MHz, with lumped pi model capacitances of 6.5pF and a quality factor of 10 at a resonant frequency around 1GHz. This implies low eddy current losses. A DC series resistance of 0.7Ω was also extracted.

In CMOS technology there are a few different types of capacitors available, including Metal-Insulator-Metal (MIM), Fractal and MOSFET gate capacitances. MIM capacitors are manufactured using special metal layers and as such they can be accurately characterized but they have low capacitance density. Fractal capacitors are made of geometrically shaped regular metal layers. They have

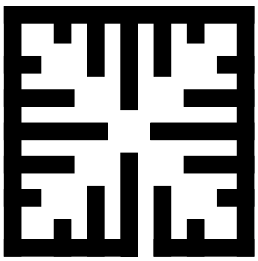

Figure 4. A wide bar PGS [6]

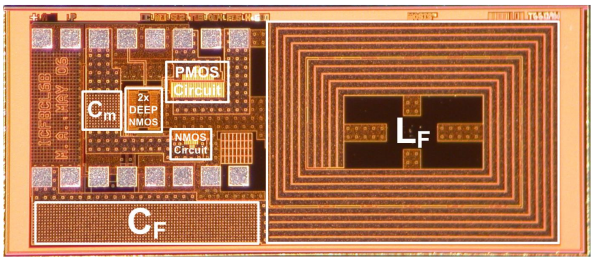

Figure 5. Chip micrograph

higher capacitance density but their capacitance can vary depending on the variations of the fabrication process [9]. MOSFET gate capacitors have the highest capacitance density, but they are non-linear [10].

The Equivalent Series Resistance (ESR), of such a capacitor consists mainly of two MOS related parts: gate resistance and channel resistance. Therefore, the ESR exhibits a minimum for a certain device aspect ratio [10]. A reduced ESR not only decreases power dissipation in the capacitor, but also lowers the voltage ripple across it.

In switch mode power converters, capacitors are used as bulk energy storage devices. As such, they are usually large. In this work, an array of hundreds of NMOS devices in parallel is used to provide the high capacitance needed as C_F. The nonlinear behavior of gate capacitance is not significant here because the capacitance can be predicted according to the smoothed design working voltage.

B. Chip Design

In the prototype, a resistive voltage divider, R_1 and R_2 is used to keep V_m around $V_{DD}/2$ at startup and does not significantly contribute to operational power. Node V_m is also made available off-chip to be externally probed or adjusted if necessary. Input resistors R_3 and R_4 in Figure 3 are 50Ω terminators so $V_{pmos\text{-}in}$ and $V_{nmos\text{-}in}$ could be driven by external signal generators at the high frequency of 660MHz.

To keep things simple due to fabrication deadlines, this design does not automatically delay signals to achieve ZVS. Instead, the implementation relies upon the test equipment to generate input signals $V_{pmos\text{-}in}$ and $V_{nmos\text{-}in}$ with the appropriate timing.

The NMOS transistors in the top inverter chain for M_p need to have zero body voltage with respect to their source, so they are isolated from the p-substrate using n-well and deep n-well implantation as described in [11]. The same procedure is used for D_1 and D_2, where the body should be connected to the drain to reverse bias the intrinsic body diode.

The chip micrograph is shown in Figure 5. The chip is laid out for on-chip probing. The 4mm^2 total die area uses 2.5mm^2 for the converter. Even at 660MHz, the inductor dominates the area. The capacitor C_F occupies a much smaller area. Designed for an output current of 50mA at 1V, the power converter achieves a power-to-area ratio of 50m/2.5 = 20mW/mm^2.

IV. Simulation And Measurement Results

A. Simulations

To investigate the effectiveness of the charge-recycling scheme, three variants of the circuit were designed and simulated. The first variant (i) is a baseline converter with full-swing drivers; therefore no recycling diodes or C_m is present. The other two circuit variants have low-swing/stacked drivers: (ii) with no diodes, (iii) with diodes and C_m. Simulation results for output voltage and efficiency versus duty cycle are shown in Figures 6 and 7, respectively. For the low-swing no-diode circuit (ii) a supply voltage of $V_{DD}/2$ is connected to V_m to keep it stable. For circuit (iii), V_m is not connected to the $V_{DD}/2$ supply, but it was checked to make sure that it was stable around $V_{DD}/2$.

As expected, the circuit with all the options has the highest efficiency. Indeed, the efficiencies show improvement with each additional change. For example, at a 40% duty cycle, the efficiency of the circuits are (i) baseline 22%, (ii) low-swing 30%, and (iii) energy recycling diodes 35%. Thus the efficiency improves from 22% to 35%. Figures 6 and 7 also show that while circuits (ii) and (iii) are more efficient than (i), they have lower V_{out} at the same duty cycle.

B. Chip Measurements

Testing of this chip was done at 2.2V like the simulations. A total of ten chips were tested to study the variation in fabrication process and to determine that the test results are statistically significant. Test measurements with standard error (S_E) bars are presented in Figure 8. The physical measurements required the use of an external supply of 1.1V connected to V_m because it was higher than the expected voltage of $V_{DD}/2$. However, measurements show that this supply voltage was not delivering any power to the circuit as it was always sinking current to reduce V_m. The output is adjustable between 0.75V to 1V by varying duty cycle D from 45 to 64% with a fixed load. Conversion efficiency, P_{out}/P_{in}, ranges 25 to 31%.

V. Discussion

In creating a controllable fully integrated switch-mode converter operating at nearly 1GHz, a number of technical difficulties have been overcome. The circuit topology is a DC-DC buck converter allowing adjustment of the output voltage in the usual step down converter

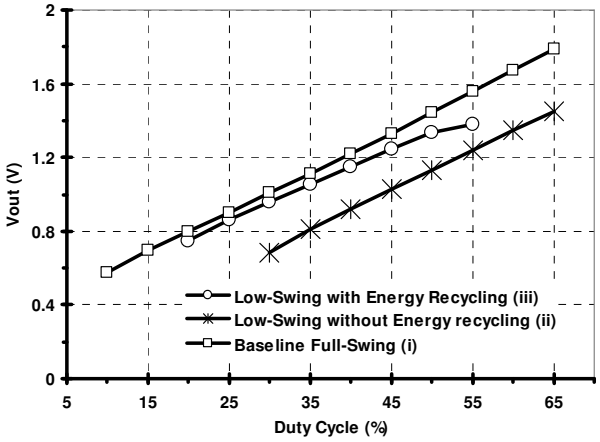

Figure 6. Simulated output voltage variation with duty cycle

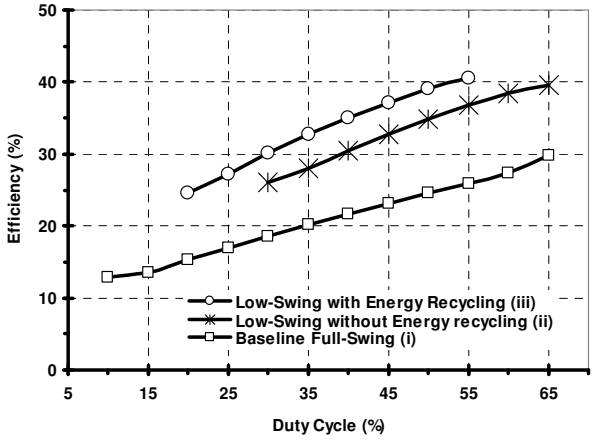

Figure 7. Simulated efficiency variation with duty cycle

manner. The inductor design followed that of integrated RF inductors and was found to be suitable for use in switch-mode, as the stray capacitances were relatively small. The parameter extraction used was also very effective. Reaching an efficiency of around 30% in such circumstances is very good and at a first attempt rivals that of switched capacitor converters sometimes proposed. Clearly the limitation associated with such high driver powers at these high frequencies is a challenge that must be addressed in all such designs.

There are a few limitations with the implemented prototype. First, M_p and M_n and the drive chains should all be implemented with low-V_t transistors. Using them would help the drivers fully turn on with the low-voltage supply, thereby reducing power consumption in the drive chains and improving power delivery to the output load. However, these were not available in the CMOS process that was used. Instead, regular transistors were used, resulting in degraded efficiency in both simulation results and the manufactured prototype. Using an ad hoc method of simulating low-V_t transistors, conversion efficiency at a 40% duty cycle is improved to 46% (up from 35%).

Second, power is lost due to the voltage drop across diodes D_1 and D_2. The diodes were used to keep it simple for proof-of-concept, but a more complex circuit could be devised. Nonetheless, it is clear from the simulations that the concept is working and a significant improvement in efficiency is gained by the use of the driver energy recycling. Although there is a drop in V_{out} after switching to low-swing drivers, Figure 6 clearly shows that the addition of the energy recycling diodes is able to improve energy conversion to the point where the V_{out} is nearly restored to the same level obtained with the original full-swing drivers. This restoration in the voltage conversion ratio (Figure 6) also implies that the rising edge of V_{inv} is sped up. Speeding it up by means of an increased reverse inductor current would be detrimental to the conversion efficiency because of discharging C_F and it would increase the losses with a higher ripple current.

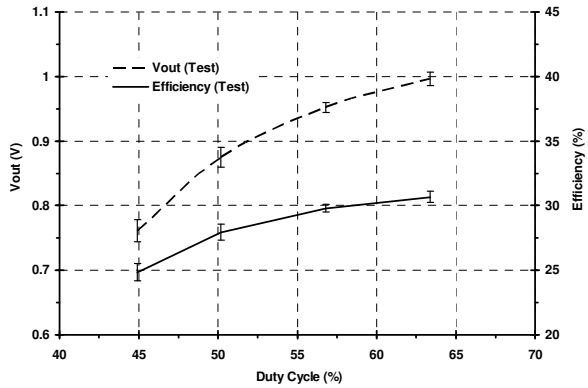

Figure 8. Measured chip results with standard error (S_E) bar

Another simple solution might be to use two PMOS and NMOS series transistors as shown in Figure 9. Only during charge recycling, when V_{inv} is in transition, both transistors need to be on, providing for the current path from node V_m to node V_{inv}.

Third, the ZVS timing delays were controlled by the signal generator, but a proper circuit needs to be added to control these delays itself. This was not implemented to keep the design simple.

To employ the ZVS technique, turn on time for M_p and M_n need to be delayed. Turn off times are still dictated by the duty ratio of the gating signals.

Figure 9 shows a possible solution. Transistor M_p can be turned on and off by pull-down transistor M_{nu} and pull-up transistor M_{pu}, respectively. Similarly, transistor M_n can be turned on and off by pull-up transistor M_{pd} and pull-down transistor M_{nd}, respectively. As ZVS affects only the turn on time, delayed gating signals are only needed for M_{nu} and M_{pd}.

When a signal propagates through a CMOS chain of inverters, it gets delayed due to charging and discharging of gate capacitances through MOSFET on resistances. This means that V_{inv} is a delayed and inverted version of V_{pmos} and so on. In Figure 9, V_{inv} is used as the delayed gating signal for M_{nu} and M_{pd}. A similar method that provides ZVS for M_n has been previously proposed by

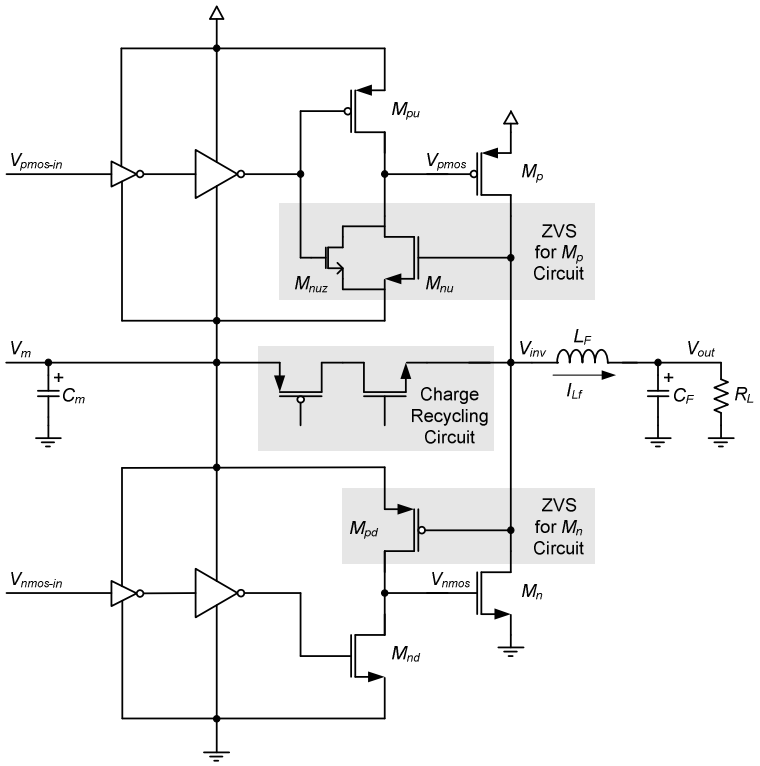

Figure 9. Circuit diagram of the proposed ZVS and charge recycling circuits for the DC-DC converter

the authors [12] [13]. Here, the ZVS circuits for M_p and M_n are similar except for the addition of a small transistor M_{nuz}. This transistor assists M_{nu} in turning on the M_p transistor at start-up. That is because when V_{inv} is low, M_{nu} can not pull-down V_{pmos} as its gate voltage is low. For the proper operation of ZVS for M_p circuitry, a negative inductor current is needed, thus the value of the inductor L_F is important.

A start-up transistor is not needed to assist M_{pd} when V_{inv} is high. Current builds up in the inductor as V_{inv} goes high. It is this already build-up inductor current that brings down V_{inv}, effectively assisting M_{pd} in start-up.

VI. Conclusions

The chip demonstrates the operation of a 660MHz converter implemented entirely in 180µm process, including on-chip passives. The measured efficiency obtained is excellent for such a prototype and for such a high switching frequency.

The use of the external source voltage sink indicates that the simulation of the gate driver inverters is not as accurate as required when using standard transistors in the supply-stacked manner.

The efficiency of the prototype could be improved in a few ways. Using low-V_t transistors would help the drivers fully turn on with the low-swing voltage supply, thereby reducing power consumption in the drive chains. Power is also lost due to the voltage drop across diodes D_1 and D_2. The diodes keep it simple, but a more complex circuit could be devised. For example [14] mimics the behavior of a diode using a transistor, where the gate is driven by a voltage comparator sensing V_{DS}. However, gating circuitry used here must operate much more quickly, on the order of tens of picoseconds.

It is anticipated that the difficulties brought about by the limitations imposed on this design will be removed in later implementations. However, it is clear that the simulation tools may need further development before such merged technology designs can be produced in a confident manner. Together with clock energy recycling introduced in [12] and [13], this is another step in the development of practical DVFS solutions.

Acknowledgment

The authors would like to thank Canadian Microelectronics Corporation (CMC Microsystems) for providing CAD tools and facilitating the chip fabrication. This work is supported in part by funding from the Natural Sciences and Engineering Research Council of Canada (NSERC).

References

[1] N. Dragone, A. Aggarwal, and L. R. Carley, "An adaptive on-chip voltage regulation technique for low-power applications," in *Proc. IEEE Int. Symposium on Low Power Electronics and Design (ISLPED)*, 2000, pp. 20-24.

[2] A. J. Stratakos, S. R. Sanders, and R. W. Brodersen, "A low-voltage CMOS DC-DC converter for a portable battery-operated system," in *Proc. IEEE Power Electronics Specialists Conference (PESC)*, 1994, pp. 619-626.

[3] J. Xiao, A. Peterchev, J. Zhang and S. Sanders, "A 4μA-Quicent-Current Dual-Mode Buck Converter IC for Cellular Phone Applications," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2004, pp. 280-283.

[4] S. C. O. Mathuna, T. O'Donnell, W. Ningning, and K. Rinne, "Magnetics on silicon: an enabling technology for power supply on chip," *IEEE Trans. Power Electronics*, vol. 20, no. 3, pp. 585-592, May 2005.

[5] C. Yue, C. Yue and S. Wong, "On-chip spiral inductors with patterned ground shields for Si-based RF ICs," *IEEE J. Solid-State Circuits*, vol. 33, no. 5, pp. 743-752, 1998.

[6] J. N. Burghartz, "Progress in RF inductors on silicon-understanding substrate losses," in *IEEE Int. Electron Devices Meeting (IEDM) Dig. Tech. Papers*, 1998, pp. 523-526.

[7] J. N. Burghartz, D. C. Edelstein, M. Soyuer, H. A. Ainspan, and K. A. Jenkins, "RF circuit design aspects of spiral inductors on silicon," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 2028-2034, Dec. 1998.

[8] A. M. Niknejad, and R. G. Meyer, "Analysis, Design, and Optimization of Spiral Inductors and Transformers for Si RF IC's," *IEEE J. Solid-State Circuits*, vol. 33, no. 10, pp. 1470-1481, Oct. 1998.

[9] H. Samavati, A. Hajimiri, A. R. Shahani, G. N. Nasserbakht, and T. H. Lee, "Fractal capacitors," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 2035-2041, Dec. 1998.

[10] G. Villar, E. Alarcon, F. Guinjoan, and A. Poveda, "Optimized design of MOS capacitors in standard CMOS technology and evaluation of their Equivalent Series Resistance for power applications," in *Proc. IEEE Int. Symposium Circuits and Systems (ISCAS)*, 2003, pp. 451-454.

[11] J. Lin, "Challenges for SoC Design in Very Deep Submicron Technologies," National Semiconductor Corp. [Online]. Available: http://www.ece.uci.edu/codes+isss/Invited/JamesLin.pdf

[12] M. Alimadadi, S. Sheikhaei, G. Lemieux, S. Mirabbasi and P. Palmer, "A 3GHz Switching DC-DC Converter Using Clock-Tree Charge-Recycling in 90nm CMOS with Integrated Output Filter," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2007, pp. 532-533.

[13] M. Alimadadi, S. Sheikhaei, G. Lemieux, S. Mirabbasi, P. Palmer and W. Dunford, "Energy Recovery from High-frequency Clocks using DC-DC Converters," in *Proc. IEEE Int. Symposium on Very Large Scale Integration (ISVLSI)*, 2008, pp. 162-167.

[14] T. Y. Man, P. K. T. Mok and M. Chan, "A CMOS-Control Rectifier for Discontinuous-Conduction Mode Switching DC-DC Converters," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2006, pp. 358-359.