A 680nA ECG acquisition IC for leadless pacemaker applications

A 680 nA ECG Acquisition IC for Leadless Pacemaker Applications

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***Abstract*—A sub-μW ECG acquisition IC is presented for a single-chamber leadless pacemaker applications. It integrates a low-power, wide dynamic-range ECG readout front end together with an analog QRS-complex extractor. To save ASIC power, a current-multiplexed channel buffer is introduced to drive a 7 b-to-10 b self-synchronized SAR ADC which utilizes 4 fF/unit capacitors. The ASIC consumes only 680nA and achieves CMRR >90 dB, PSRR >80 dB, an input-referred noise of 4.9 μVrms in a 130 Hz bandwidth, and has rail-to-rail DC offset rejection. Low-power heartbeat detections are evaluated with the help of the ASIC acquiring nearly 20,000 beats across 10 different records from the MIT-BIH arrhythmia database. In the presence of muscle noise, both the average Sensitivity (Se) and Positive Predictivity (PP) show more than 90% when the input SNR >6 dB.**

***Index Terms*—Analog feature extraction, electrocardiogram (ECG), heartbeat detection, leadless pacemaker, low-power.**

I. Introduction

RECENTLY, a tiny leadless pacemaker [1], [2] residing completely inside the right ventricle of a patient's heart receives great attention as it requires no leads, no chest incision, and no scar, but provides the same functionality and life time as the traditional pacemaker does. Without doubt, development of such a miniature-sized pacemaker must be centered around ultra-low power consumption together with high quality signal acquisition and heartbeat classification. Although electrical pacing spends a significant part of the power budget of a pacemaker system, saving power in the sensing electronics is still crucial as cardiac rhythm disorders must be continuously monitored and classified for several years [3], [4]. As a result, high performance feature extraction methods, such as continuous wavelet transform (CWT), are avoided to classify the heartbeat due to its excessive computation power of the digital signal processing (DSP) [5]. A power-efficient alternative to this is shifting the functionality of QRS feature extraction to the analog domain. This will greatly reduce the system power consumption by reducing the computation complexity of the DSP as shown in Fig. 1 [6], [7]. The ECG acquisition IC ensures to readout both the ECG signal and to extract the meaningful ECG feature in the analog domain prior to digitization. An ADC then digitizes both the time-domain ECG signal (ECGout) and its feature signal (FEout) and provides it to a DSP. The FEout channel is simply emphasizing ECG signal activity in a specific frequency band. In the DSP, a low-power beat detection algorithm can be implemented by using the power of FEout as an input to detect signal peaks and then using the time-domain ECG signal to classify the heartbeat.

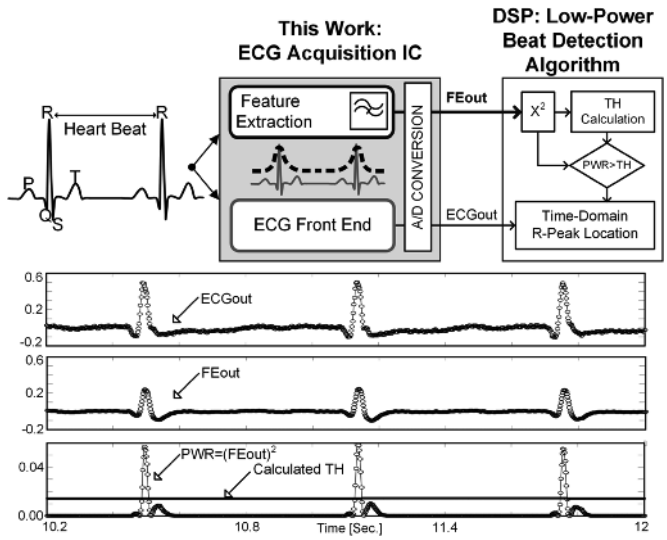

Fig. 1. Low-power ECG acquisition IC utilizing analog feature extraction to assist implementing low-power heartbeat detection algorithm [6].

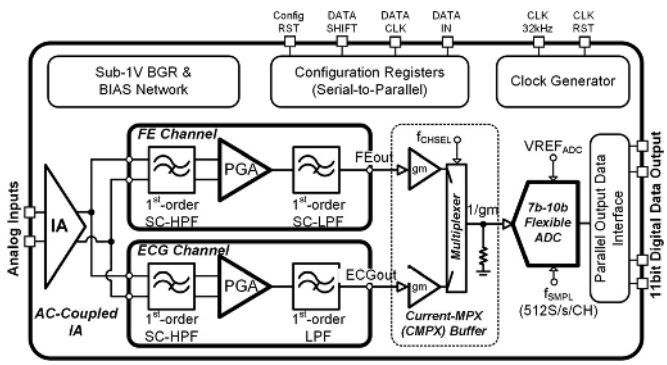

Fig. 2. The architecture of a single-channel ECG acquisition IC which embeds an feature extraction (FE) channel.

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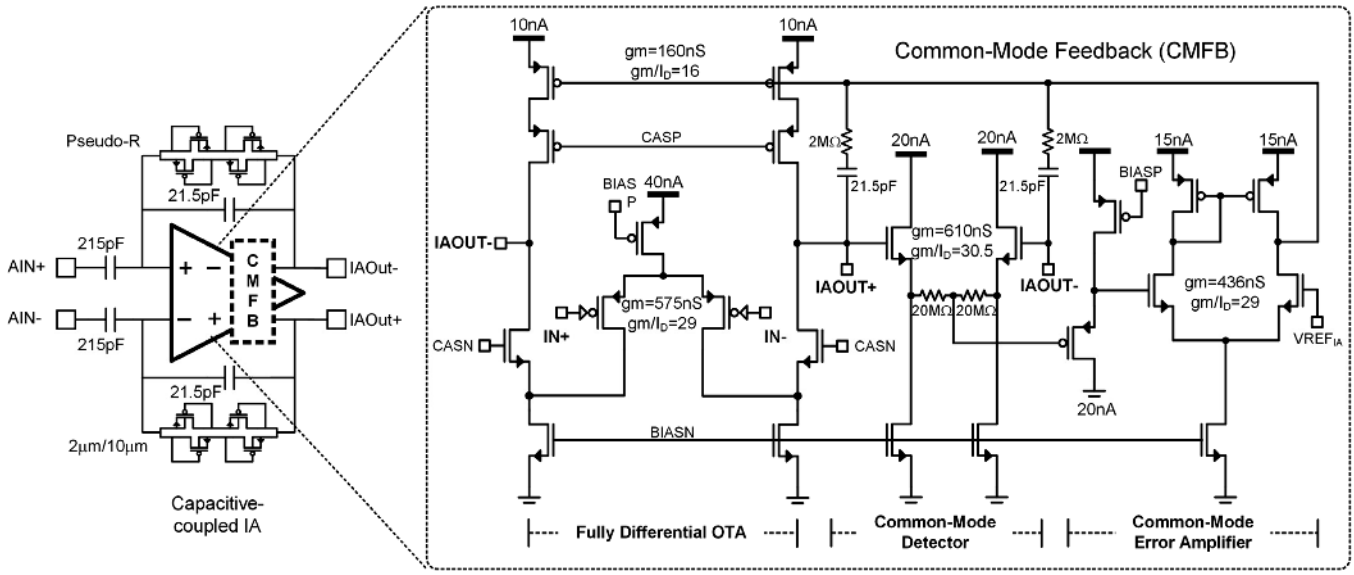

Fig. 3. Detailed implementation of the fully-differential capacitive-coupled IA.

In this paper, a sub-μW ECG acquisition IC [8] is presented for low-power heartbeat detection. The presented IC not only embeds a power efficient analog feature extractor but also it further integrates a current-multiplexed ADC driver and a self-synchronized ADC to improve the power efficiency of the analog back end. This advances the state-of-the-art by reducing power consumption of the IC below 1 μW without compromising other specs, such as input SNR $>$70 dB, CMRR $>$90 dB, PSRR $>$80 dB. Furthermore, it assists the DSP platform in implementing a low-power heartbeat detection algorithm by reducing digital computation complexities.

This paper is organized as follows: Section II describes the ASIC architecture and implementations. It includes: 1) the detail implementation of readout channel including an instrumentation amplifier (IA), switched-capacitor filters, and a programmable gain amplifier (PGA), and 2) the power-efficient data conversion technique based on a current-multiplexed (CMPX) buffer and a self-synchronized ADC. Section III summarizes ASIC measurement results. In Section IV, the heartbeat detection system is evaluated. Finally, Section V concludes the paper.

II. ASIC Implementation

Fig. 2 shows the architecture of a single-channel ECG acquisition ASIC which embeds a flexible, low-power QRS feature extraction channel. The ASIC integrates a fully differential AC-coupled IA as first stage which can handle rail-to-rail input DC offset without any external passive components. One branch of the IA goes to the analog feature extractor (FE), which consists of a programmable gain amplifier (PGA) and accurate narrow-bandwidth filters, and is used to precisely monitor the signal activity in a selected frequency band of the ECG signal. The ECG channel is similar, but provides wider signal bandwidth. In both ECG and FE channels, the signals are converted into single-ended at the PGA stage to reduce the power consumption by driving a single-ended ADC. In addition to that, the 7 b-to-10 b configurable ADC [9] digitizes ECGout and FEout via a current-multiplexed (CMPX) buffer to avoid the use of power-consuming channel buffers and ADC drivers.

Note that the ASIC is a highly integrated solution offering all of the functionality of acquiring the ECG signal without any external passive components. A sub-1 V bandgap reference is completely integrated without any external capacitor for noise filtering to provide on-chip stable bias signals, and a clock generator delivers all necessary clock signals from a single 32 kHz quartz crystal for ADC sampling and accurate signal filtering. In addition, the ASIC provides wide scale programmability and can be tailored to a wide dynamic range signal acquisition. Through externally controllable configuration registers, the ASIC can select different settings for channel gain, bandwidth, and ADC resolution. 11 bit (10 bit data and 1 bit channel ID) parallel ADC outputs are provided for further digital signal analysis in a DSP platform such as beat detection and classification.

A. Readout Channel With Embedded Feature Extraction (FE)

The IA is the first active block in the complete signal readout chain and the design is critical as it determines for a large part performances such as noise, dynamic range, CMRR, input impedance, and the capability to filter out large DC offset at inputs. Fig. 3 shows the on-chip rail-to-rail capacitive-coupled IA utilized in this ASIC. A fully differential folded cascode amplifier together with capacitive feedback divider provides a closed-loop gain of 20 dB. At the outputs of the amplifier, source followers together with 20 MΩ resistors act as common mode detector. With 20 nA bias current flowing through each source follower, the outputs of the IA support a large signal swing as high as 1.1 V_{p-p} without significant distortion (total harmonic distortion (THD) $<$1%). The extracted common mode (CM) signal is then compared with $VREF_{IA}$, to set the output CM voltage to mid-supply. Note that the output CM voltage also biases the inputs of the amplifier through 2 pseudo resistors in parallel to the feedback capacitors (21.5 pF). The IA consumes only 150 nA while showing 400 $nV/\sqrt{Hz}$ input noise floor.

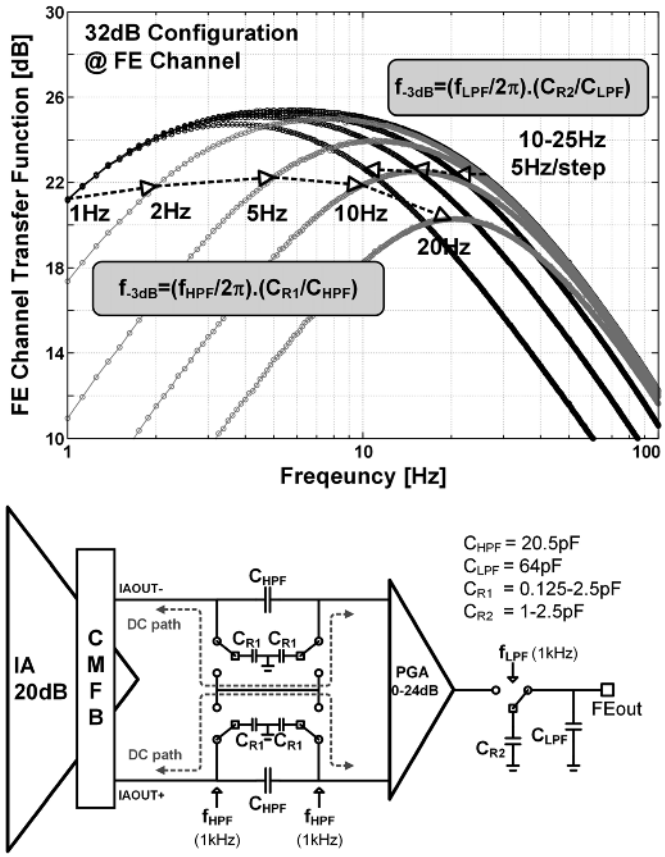

Fig. 4. (a) Measured transfer functions of the FE channel and (b) its detailed implementation.

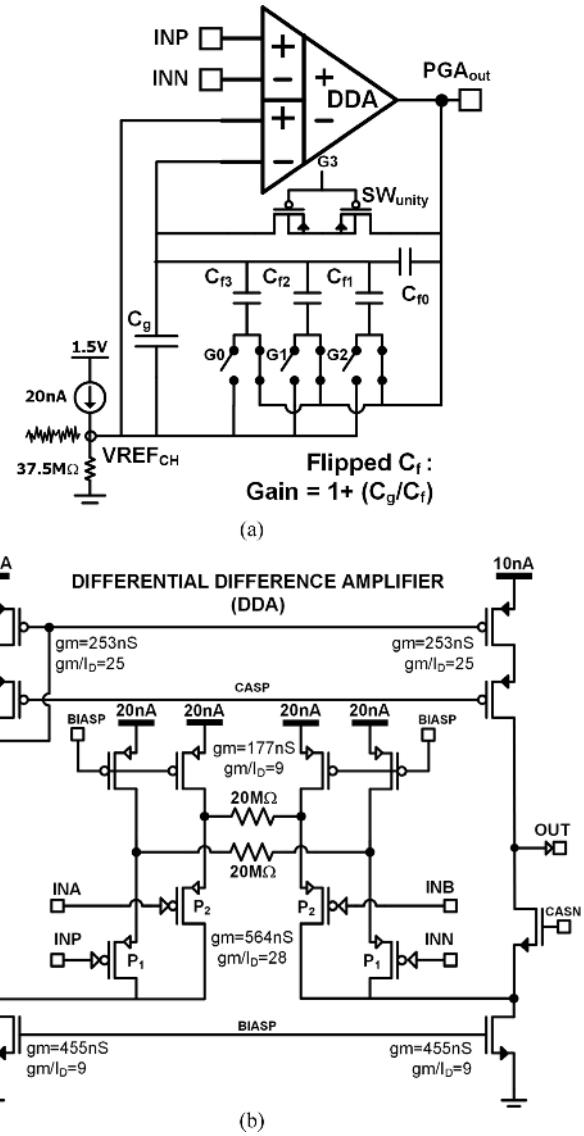

Fig. 5. (a) Programmable Gain Amplifier (PGA) based on Differential Difference Amplifier (DDA) with flipped capacitors. (b) Detailed implementation of DDA.

The IA drives 2 switched-capacitor high pass filters (SC-HPF) in the ECG channel and FE channel, respectively. Fig. 4 shows the details of FE channel. Unlike the ECG channel that provides a HPF corner frequency of 1 Hz, the FE channel is normally configured to 10 Hz to reject low-frequency T-waves as well as electrode motion artifacts. The SC-HPF utilizes a floating structure which has a unity gain at DC while providing an accurate and flexible cutoff frequency of 1 Hz, 2 Hz, 5 Hz, 10 Hz, or 20 Hz by adjusting the value of $\mathrm{C_{R1}}$. Benefitting from switching the small capacitors $(\mathrm{C_{R1}})$, the filters consume small silicon area but provide large enough input impedance more than 400 MΩ. Thanks to the floating HPF, the IA not only can bias the HPFs and the following PGAs (DC gain $= 1$) in ECG and FE channels but can drive them directly without additional analog buffers and bias circuits. In the FE channel, a 10 Hz–25 Hz (5 Hz/step by adjusting the value of $\mathrm{C_{R2}}$) flexible switched-capacitor low pass filter (SC-LPF) is further integrated after the PGA to attenuate high-frequency out-of-band interferences.

Followed by the HPF, a PGA translates the differential signal to an amplified single-ended output (Fig. 5), thus saving power by half in the later stages. One differential pair in the differential-to-difference amplifier (DDA) receives the differential signal from the HPF. The other differential pair sets the DC output value to $\mathrm{VREF_{CH}}$ (0.75 V) and configures the gain $(1+\mathrm{C_g/C_f})$. The capacitor $\mathrm{C_g}$ is always connected to $\mathrm{VREF_{CH}}$ instead of ground. According to the different gain settings, the feedback capacitors $\mathrm{C_{f1,2,3}}$ are flipped from the side of $\mathrm{C_{f0}}$ to the side of $\mathrm{C_g}$. The advantage to do so is that the noise from $\mathrm{VREF_{CH}}$ is not anymore amplified by the high gain of the PGA. This is especially important in the case when the PGA needs to provide high gain and reject relatively high noise that is present at the power supply simultaneously. The PGA provides 0 dB to 24 dB (6 dB/step) variable gain on top of the IA gain (20 dB). The PGA can also be used as a buffer (0 dB) by enabling feedback switch $(\mathrm{SW_{unity}})$. The switch consists of 2 PMOS transistors facing each other to ensure sufficiently high off-resistance not to deteriorate the low frequency cutoff of the PGA.

B. Power-Efficient Data Conversion

Shifting the feature extraction to the analog domain increases the number of channels to be acquired by the single ADC. The design is driven by the speed considerations on the channel multiplexing between ECG and FE. Furthermore, those time-multiplexed signals must be precisely sampled by the ADC.

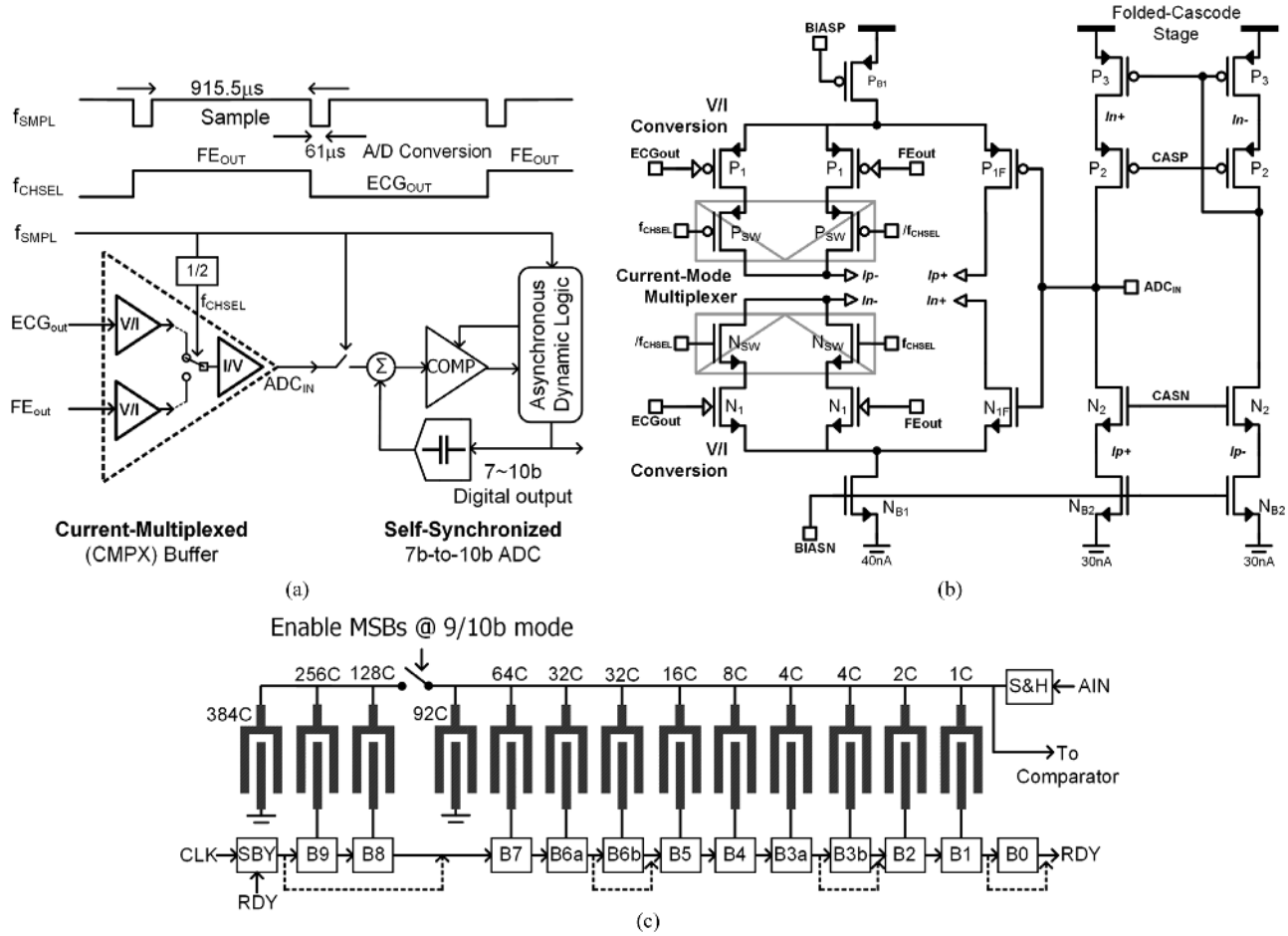

Fig. 6. (a) Power efficient data conversion based on Current-Multiplexed (CMPX) buffer and self-synchronized 7 b-to-10 b ADC. (b) Details of CMPX buffer. (c) CDAC implementation in the ADC.

Typical readout systems [6], [7], [10]–[12] consume significant power in the back end as they employ power consuming channel buffers and analog switches (16% of channel power in [6]) to ensure the analog signal settles within sufficient accuracy. In contrast, signal multiplexing before the filters and the PGA can save power but limits the programmability between the channels [13]. A low-power buffer that multiplexes the input signals in the current domain is introduced in Fig. 6(a) and (b). The CMPX buffer employs a folded-cascode amplifier with complementary inputs to provide high input impedance and to accommodate amplified large signals from the PGA stages. Transistors P_1 and N_1 convert the ECGout and FEout signals into current, and they are multiplexed by P_{SW} and N_{SW} at low impedance nodes in the folded-cascode stage. Part of the bias current through P_1 and N_1 is recycled as the multiplexed branches are active alternatingly at a rate of f_{CHSEL} (half of the ADC sampling rate, $f_S = 1024$ Hz). The multiplexed current flows to the folded-cascode stage, creating an output voltage signal at ADC_{IN}.

A self-synchronized ADC implementing a successive approximation algorithm with asynchronous dynamic logic uses the comparator and DAC to approximate the time-multiplexed signal from the CMPX buffer. The flexible-resolution ADC outputs a 7 b-to-10 b digital code dependent on the configured resolution. As shown in Fig. 6(c), a 9 bit capacitor array acts both as sampling capacitor and as feedback DAC. The DAC is

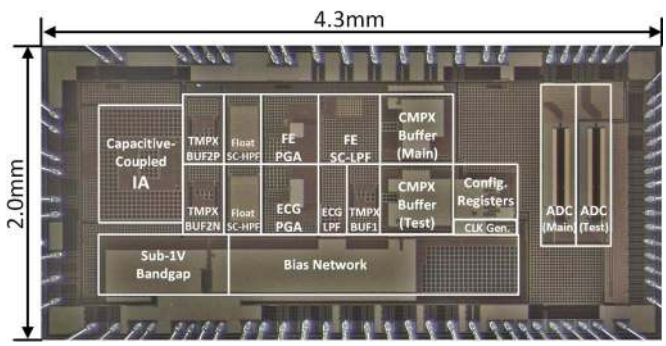

Fig. 7. The ASIC chip micrograph.

controlled by the digital bits B9–B1, generated during the SAR bit cycles. A 9 bit DAC is sufficient for a 10 bit ADC as the LSB bit cycle doesn't need to update the DAC anymore. An additional capacitor of 32 C is inserted to add redundancy, which relaxes DAC settling requirements and saves comparator power [9]. The DAC is implemented based on custom designed capacitors which utilize the parasitic fringing capacitance between 3 different metal layers (metal layers 3, 4, and 5 are placed in parallel to increase capacitor density while metal layer 1 is placed underneath for shielding). Note that absolute value of the capacitor is not very critical in the presented DAC topology

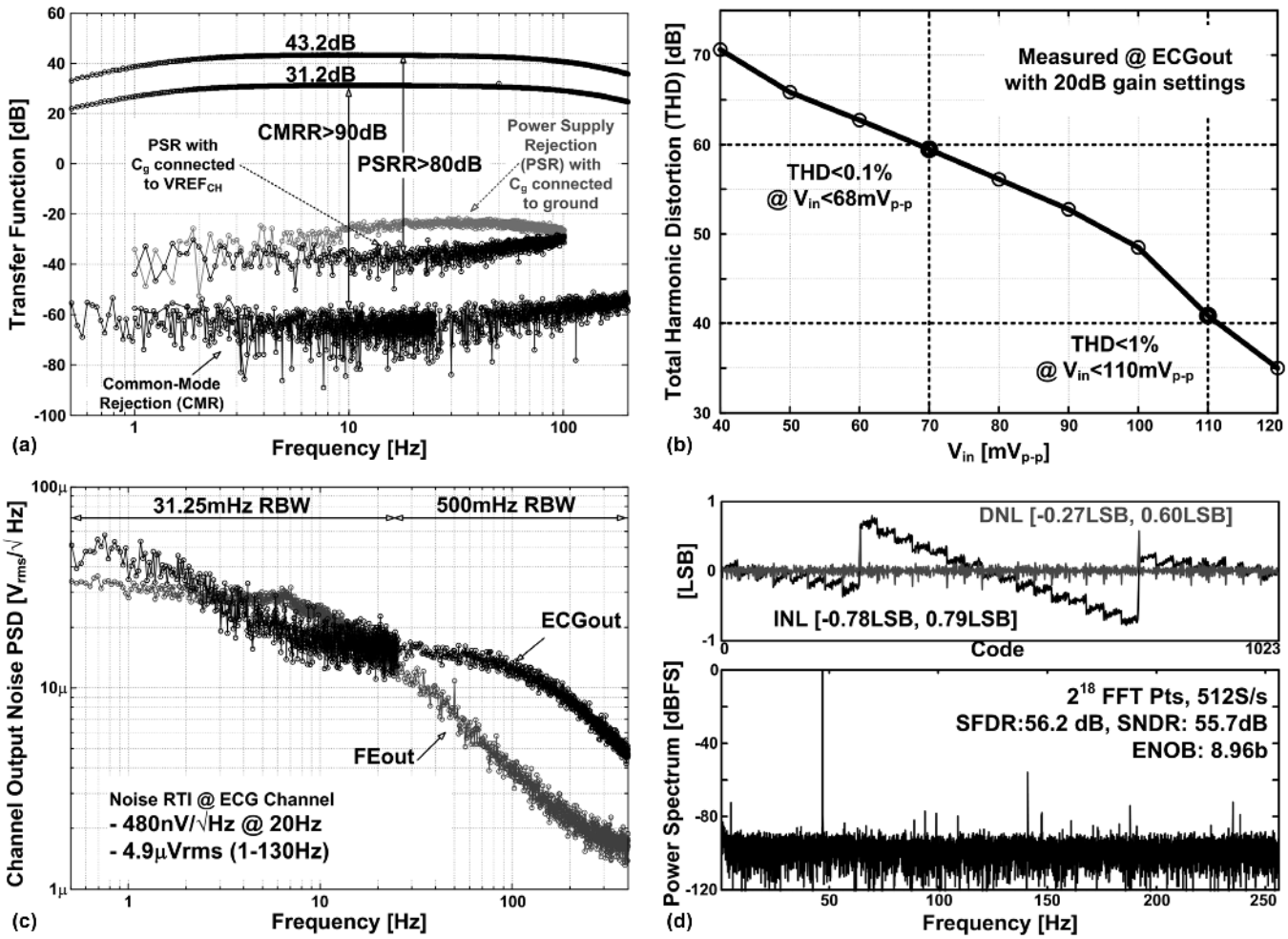

Fig. 8. Measured performance of readout channel and ADC. (a) PSRR and CMRR measured at ECGout. (b) THD (up to 10th harmonic power) measured at ECGout with 7 Hz input signal. (c) Measured channel output noise at FEout (BW = 10–15 Hz) and ECGout (1–130 Hz) with their PGA gain of 6 dB. (d) Measured ADC performance at 10 bit mode.

but the important aspect is to maintain relative matching in order to maintain linearity. To achieve sufficient matching, all capacitors (except the LSB which is implemented with a 2 fF unit element) are based on identical 4 fF unit elements and manual dummy-metal filling is performed around the array to maintain perfect symmetry. Based on Calibre extractions, the maximum capacitor error turns out to be 0.05 LSB, which is acceptably small. Mismatch studies in [14] and measurement results in [15] also confirm that the customized capacitors provide sufficient matching performance.

According to the selected resolution, the comparator and DAC are adjusted so that the lower resolution can save power while the higher resolutions can benefit from higher accuracy. Even in 10 bit resolution mode, the small input capacitance of the ADC (only 2 pF, which still provides $\mathrm{SNR}_{\mathrm{KT/C}} > 70$ dB) and the fast data conversion time allow the CMPX buffer to settle down analog signals within 0.1% accuracy while consuming only 100 nA.

III. Measurement Results

The ASIC is fabricated in a 0.18 μm CMOS process and occupies 8.6 mm^2 as shown in Fig. 7. Without any dynamic offset cancellation technique, the ECG channel can sufficiently rejects any in-band common mode noise at inputs as it shows CMRR more than 90 dB with a channel gain of 31.2 dB. With the help of the PGA improving supply noise rejection at high gain, the entire ECG channel achieves a PSRR more than 80 dB at the gain of 43.2 dB as shown in Fig. 8(a). This is 14 dB PSRR improvement by avoiding $\mathrm{VREF}_{\mathrm{CH}}$ noise amplification in the PGA without consuming additional power and area. The supply noise immunity of the channel allows using single power supply pin in the IC package. As shown in Fig. 8(b), the ECG channel can amplify (minimum channel gain = 20 dB) up to 110 $\mathrm{mV}_{\mathrm{p-p}}$ input signals with THD <1%. This can be improved to THD <0.1% by reducing the input signal below 68 $\mathrm{mV}_{\mathrm{p-p}}$. The ECG channel achieves 4.9 $\mu\mathrm{V}_{\mathrm{rms}}$ input referred noise in a 130 Hz bandwidth [shown in Fig. 8(c))] which translates to an input SNR ($\mathrm{SNR}_{\mathrm{in}}$) of more than 70 dB. As shown in Fig. 8(d), 9 bit ENOB is achieved with a DNL and INL less than 1 LSB which is sufficient for accurate heartbeat detection in the DSP. Compared to [6], [7], the ASIC shows similar performance while consumes 10 times lower power [7] On the other hand, the ASIC performs better in terms of $\mathrm{SNR}_{\mathrm{in}}$, CMRR, and PSRR while consumes similar power to

TABLE I
ASIC PERFORMANCE COMPARISON WITH STATE OF THE ARTS

	This Work	[6] TBCAS'13	[7] JSSC'11	[16] VLSI'10	[10] ISSCC'10	[13] ISSCC'13
Tech. & Supply	0.18μm, 1.3V-1.8V	0.18μm, 1.7V-1.9V	0.5μm, 2.0V	0.18μm, 0.6V	0.35μm, 1.0V	0.18μm, 0.45V
Current /Channel	680nA @512S/s/Channel	*8550nA @256S/s/Channel	*6900nA @64-1kS/s /Channel	*4700nA @ 10kS/s/Channel	690nA @312.5S/s/Channel	*2118nA @ 2kS/s/Channel
Ext.Passives	No	Yes	Yes	Yes	Yes	N/A
CMRR/PSRR	90dB/80dB	100dB/90dB	105dB	70.4dB	83.2dB/75dB	73dB/80dB
Vin,max (THD <1%)	$110mV_{p-p}$	$60mV_{p-p}$	$35mV_{p-p}$	$8mV_{p-p}$	$1mV_{p-p}$	N/A
Vn,in	4.9μVrms (130Hz)	2μVrms (100Hz)	1.1μVrms (170Hz)	3.4μVrms (156Hz)	1.15μVrms (150Hz)	3.2μVrms (10kHz)
$^{**}SNR_{in}$	70.6dB	73.2dB	73.7dB	51.9dB	42.4	N/A
Resolution	7b, 8b, 9b, 10b	10b	11b	9b	10b	10b
Analog QRS extraction	Yes	Yes	Yes	No	No	No

* Calculated from the performance reported, $^{**}\mathrm{SNR_{in}} = 20 * \log 10[\mathrm{Vin,max}/(\mathrm{Vn,in} * 6.6)]$

TABLE II
HEARTBEAT DETECTION EVALUATION RESULTS WITH CWT AND BAND POWER ALGORITHMS

Record	Total beats	CWT [19]					Band-Power (This work)				
		TP	FN	FP	Se (%)	PP (%)	TP	FN	FP	Se (%)	PP (%)
100	2272	2272	1	1	99.96	99.96	2269	3	2	99.87	99.91
101	1857	1855	2	13	99.89	99.3	1853	4	15	99.78	99.2
102	2119	2182	63	67	97.11	96.94	2111	71	75	96.75	96.57
103	2077	2077	0	6	100	99.71	2071	6	7	99.71	99.66
119	1880	1880	0	0	100	100	1873	7	132	99.63	93.42
202	2126	2120	6	10	99.72	99.53	2099	27	18	98.73	99.15
209	2958	2958	0	49	100	98.37	2956	2	50	99.93	98.34
212	2733	2733	0	14	100	99.49	2731	2	15	99.93	99.45
215	3326	3323	3	39	99.91	98.84	3296	30	63	99.1	98.12
219	2003	1998	5	156	99.75	92.76	1956	47	212	97.65	90.22
Total (average)	23414	23398	80	355	99.66	98.51	23414	199	589	99.15	97.53
Total (median)	23414	2151	2	14	99.91	99.35	1950	7	34	99.67	98.41

$Se(\%) = TP/(TP + FN)$, $PP(\%) = TP/(TP + FP)$ where TP stands for true positive (the number of true beats that have been detected), FN stands for false negative (the number of true beats that have not been detected), and FP stands for false positive (the number of false beats that have been marked as true beats).

[16], [10]. The total current consumption of the ASIC is only 680 nA. Among those, channels (1 IA + 2 PGAs) consume 350 nA (44%), the CMPX together with the ADC consumes 110 nA (17%), and the other supporting circuits (bias and digital) consume 220 nA (32%).

IV. HEARTBEAT DETECTION SYSTEM EVALUATION

The heartbeat detection system is evaluated with the help of an external DSP [17]. An ECG test signal from the MIT-BIH arrhythmia database [18] is acquired by the ASIC with the 26 dB gain for both ECG channel (1–130 Hz) and FE channel (10–15 Hz). The ADC digitizes ECGout and FEout into 10 bit digital codes at a rate of 512 Hz. A low-power band-power (BP) beat detection algorithm [6] is implemented in the DSP with fixed point C language. To detect a peak, 64 samples each for ECGout and FEout are used to calculate $(\mathrm{FEout})^2$, and a threshold value (TH) (shown in Fig. 1). Similar to [6], the peak is detected by comparing $(\mathrm{FEout})^2$ to the TH value where the lower limit for TH is optimized as 25% of the maximum peak of $(\mathrm{FEout})^2$ within the threshold crossing region. Once the peak is detected, a 8 ms searching window is applied to ECGout to classify the heartbeat.

Table II compares the heart beat detection accuracy to the high performance CWT [19] By detecting nearly 20,000 beats across 10 different records from MIT-BIH arrhythmia database, the average Se and PP are evaluated to be 99.15% and 97.53%, respectively, while the median Se and PP are evaluated to be 99.67% and 98.41%, respectively. The system is also evaluated for its robustness in the presence of noise such as muscle noise and additive white Gaussian noise (AWGN) with respect to different SNRs from 24 dB to 0 dB on top of a clean ECG signal (record 101). As shown in Fig. 9, the system performs Se and PP above 90% even with the muscle noise stress test for SNR >6 dB. With respect to the AWGN stress test, the system maintains the Se and PP above 90% for SNR > -8 dB. Although the heartbeat detection based on the BP algorithm performs less

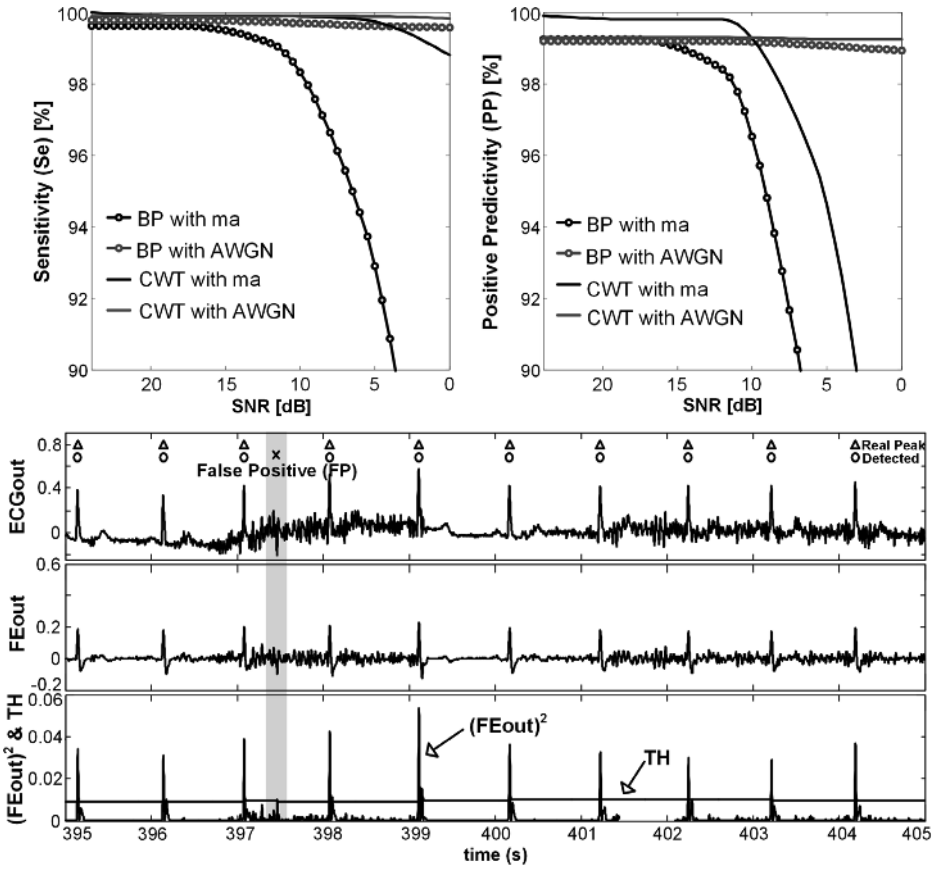

Fig. 9. Upper figure shows Se and PP performance of the heartbeat detection in the presence of muscle noise (ma) and additive white Gaussian noise (AWGN) as a function of signal to noise ratio (SNR) compared to the results of CWT based algorithm reported in [19]. Lower figure shows time domain representation with ECG signal from record 101 superimposed with muscle noise ($\mathrm{SNR} = 12$ dB).

accurate than the CWT based approach when the SNR is low, the BP approach is much more power efficient as it spends only 5.5% execution cycles of the CWT approach. It is worth to mention that the noise stress tests didn't include the noise caused by motion artifacts which is another critical noise source in practice further degrading the classification accuracy. Due to the external DSP consuming 30 μA, the complete test system consumes 31 μA. The entire system power efficiency can be further improved to implement a custom DSP like a SoC [20]

V. Conclusion

A sub-μW ECG acquisition IC integrating analog feature extraction is presented for a single-chamber leadless pacemaker application. The ASIC advances the state-of-the-art ECG readout front-end by consuming only 680 nA without compromising important performances such as CMRR $>$90 dB, PSRR $>$80 dB, and SNR $>$70 dB. To evaluate heartbeat detection, the ASIC assists an external microcontroller to implement a low-power BP beat detection algorithm. Across more than 20,000 beats in 10 different records from the MIT-BIH arrhythmia database, the average Se and PP show more than 90% for muscle noise stress test when the input SNR $>$6 dB.

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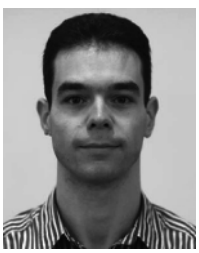

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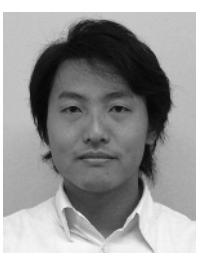

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Dr. Yazicioglu was the corecipient of the Best Student Paper Award at the IEEE International Symposium on Circuits and Systems (ISCAS) 2013, the IEEE Biomedical Circuits and Systems Conference (BioCAS) 2011, the Smart Systems Integration Conference (SSI), 2008, and the "Sensors & Transducers Journal: 10 Best Articles Published in 2008" award. He serves on the technical program committees of European Solid State Circuits (ESSCIRC) and the International Solid State Circuit Conference (ISSCC). He was cochair of the Biomedical Circuits and Systems Conference (BioCAS) 2013 in Rotterdam, The Netherlands.