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Research Article

A 69-dB SNR 89-μW AGC for Multifrequency Signal Processing Based on Peak-Statistical Algorithm and Judgment Logic

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A novel peak-statistical algorithm and judgment logic (PSJ) for multifrequency signal application of Autogain Control Loop (AGC) in hearing aid SoC is proposed in this paper. Under a condition of multifrequency signal, it tracks the amplitude change and makes statistical data of them. Finally, the judgment is decided and the circuit gain is controlled precisely. The AGC circuit is implemented with 0.13 μm 1P8M CMOS mixed-signal technology. Meanwhile, the low-power circuit topology and noise-optimizing technique are adopted to improve the signal-to-noise ratio (SNR) of our circuit. Under 1 V voltage supply, the peak SNR achieves 69.2 dB and total harmonic distortion (THD) is 65.3 dB with 89 μW power consumption.

1. Introduction

In the twenty-first century, as China entered the aging society gradually, hearing damage has become a major disease that is prevalent in elderly people. In this group, more than 90% of patients can compensate and repair their hearing ability by wearing a hearing aid device. A digital hearing aid SoC includes Autogain Control Loop (AGC), ADC, digital signal processing platform (DSP), power amplifier driver, and EEPROM [1–3].

As the most significant part of SoC, the performance and power consumption of AGC are decisive for the SoC. Traditional AGCs use analog peak envelop-detection method which limits the resolution and dynamic range of gain adjustment. It also consumes extra power and worsens the noise performance [2–4]. In more complex occasions, the microphone output contains a number of different frequency sine waves, and the amplitude of them may be located in any interval of V_{peak} and V_{act}. If still using peak envelop-detection algorithm, AGC may process only one signal of a certain frequency and cause others to malfunction. Hence, we need a new algorithm for more accurate gain control.

According to the characteristics of audio signal, a novel peak-statistical algorithm and judgment logic (PSJ) for AGC are proposed in this paper. It extracts the amplitude statistical characteristics of most signal and adjusts AGC gain precisely, which ensure that most signal remains in the best receiving range. The algorithm is realized by mixed-signal design method. As a logic circuit, the PSJ circuit consumes less power compared with its analog opponent. Also by adopting low-power topology, the power consumption of circuit is optimized and high performance of SNR and THD is achieved.

2. Basis of Proposed PSJ

Previous research proves that the sound pressure level (SPL) received by human beings ranges from 60 dB SPL to 100 dB SPL, and the safe sound level is about 80 dB SPL to 90 dB SPL [5–9]. So the gain of AGC in hearing aid SoC must be adjusted in a wide range of about 40 dB. The proposed AGC structure with PSJ is shown in Figure 1. The programmable gain amplifier (PGA) varies from −6 dB to 30 dB with 3-dB/step.

Firstly, the microphone signal is acquired and amplified (or attenuated) by PGA. Then, the PGA output is compared with peak-threshold (V_{peak}) and active threshold (V_{act}) through two comparators and 2-bit digital code is generated.

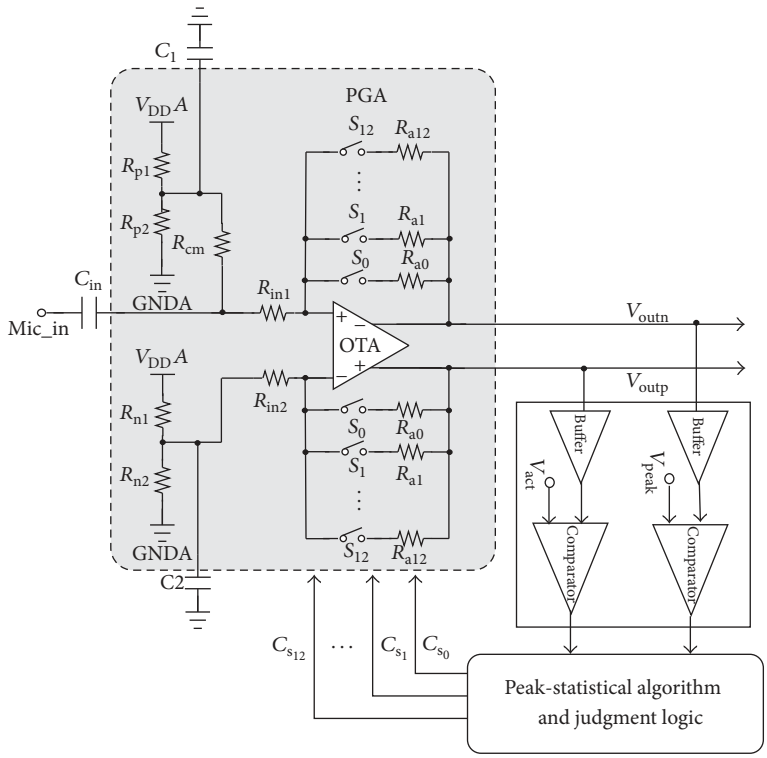

Figure 1: Block diagram of AGC circuit.

When the signal is greater than V_{act} and less than V_{peak}, we think that the signal is in the best reception range of the human ear. After that, 2-bit digital code is analyzed by PSJ logic. Finally, a 13-bit control code is transmitted to PGA by PSJ logic, which modifies the gain of PGA to process the signal amplitude until it is located between V_{peak} and V_{act}.

The motivation of the new algorithm is as follows: Taking single-frequency input signal for example, V_{peak} and V_{act} are the two comparators' peak and active amplitude threshold of AGC, respectively.

Since AGC's sampling clock frequency is much higher than the sound signal frequency, even if the input (V_{in}) is greater than V_{peak}, logic "11" and logic "00" (or 10, 01) coexist in the comparator output as shown in Figure 2(a). If we still use simple digital peak detection logic, it is not able to accurately judge the right magnitude range of input signal, which may make AGC error operation. And the same condition happens when V_{in} is between V_{peak} and V_{act} as shown in Figure 2(b). Only in the case of Figure 2(c), when V_{in} is less than V_{act}, the comparator outputs "00." AGC can amplify the input. Therefore, in Figures 2(a) and 2(b) case, we need to make statistics of the comparator output. Only when the number of right logic codes of comparator output is greater than the minimum number for judgment, the PSJ logic can output precise control code for PGA gain adjustment.

In a more complex multifrequency signal environment as Figure 3, some of the signals may be located between V_{peak} and V_{act}, and others are greater than V_{peak}. At this time, the situation is much the same as single-frequency input when the comparator output also has a number of different logic values. Therefore, we also need to do a statistical analysis of comparator output, to complete the precise control of the majority of the signals.

The statistical properties of the output signal are derived as follows: when the AGC input is the sine wave, the probability of PSJ is calculated as

$$V = A \sin \omega t. \tag{1}$$

And for a given voltage, the probability density of a sine wave is

$$P(V_x) = \frac{1}{\pi \sqrt{A^2 - V_x^2}}. \tag{2}$$

Then, the signal probability between V_a and V_b is

$$\begin{aligned} P(V_a, V_b) &= \int_{V_a}^{V_b} \frac{1}{\pi \sqrt{A^2 - V_x^2}} dV_x \\ &= \frac{1}{\pi} \left[\sin^{-1}\left(\frac{V_b}{A}\right) - \sin^{-1}\left(\frac{V_a}{A}\right) \right]. \end{aligned} \tag{3}$$

Based on $\cos(\sin^{-1}(V_x/A)) = \sqrt{A^2 - V_x^2}/A$, the cosine function is put on both sides of (3); then,

$$\begin{aligned} V_b^2 - \left(2V_a \cos\left(\pi P\left(V_a, V_b\right)\right)\right) V_b \\ - A^2 \left(1 - \cos^2\left(\pi P\left(V_a, V_b\right)\right)\right) + V_a^2 = 0. \end{aligned} \tag{4}$$

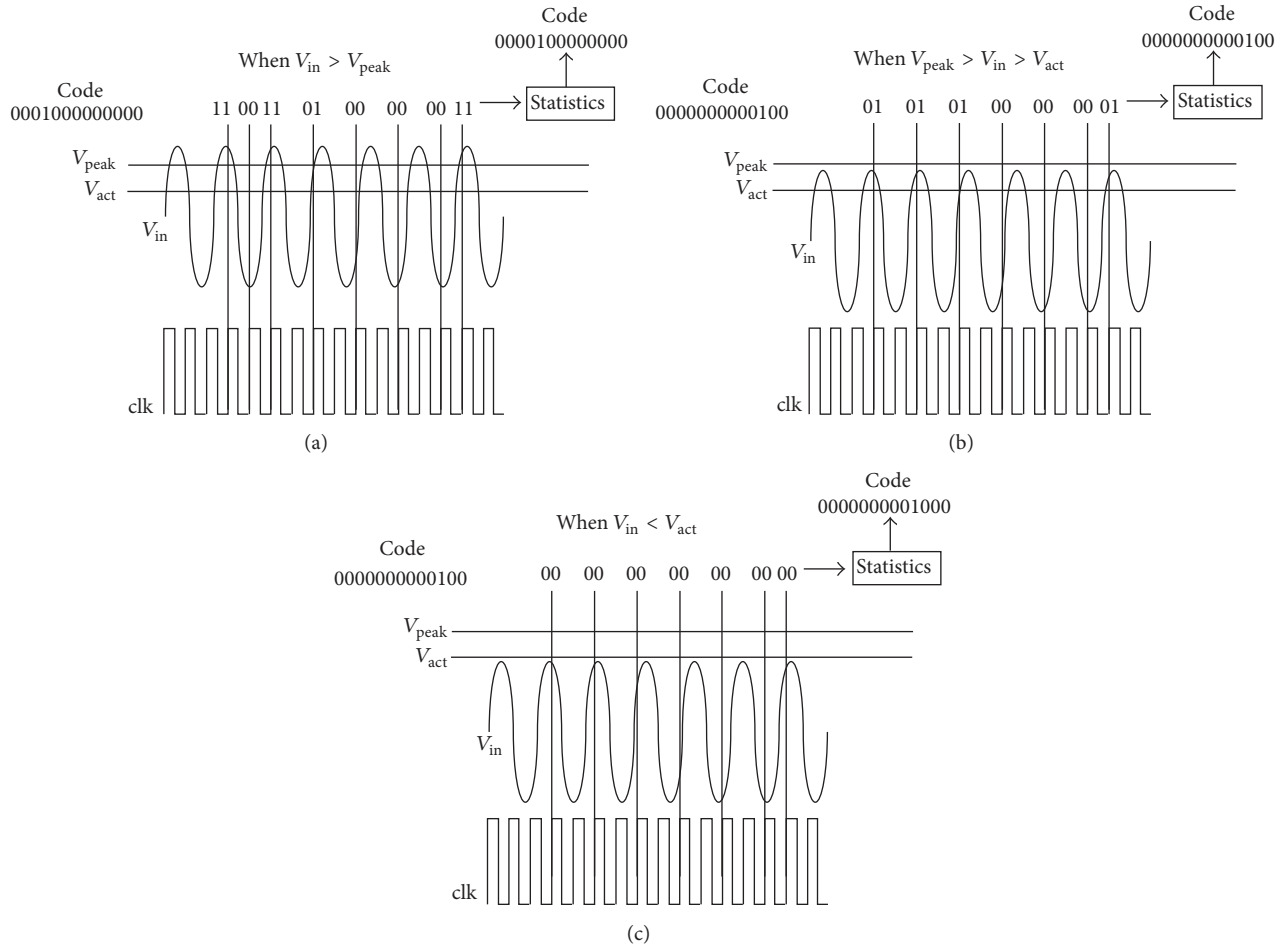

Figure 2: Basis of PSJ logic with single-frequency input. (a) When $V_{in} > V_{peak}$; (b) when $V_{peak} > V_{in} > V_{act}$; (c) $V_{in} < V_{act}$.

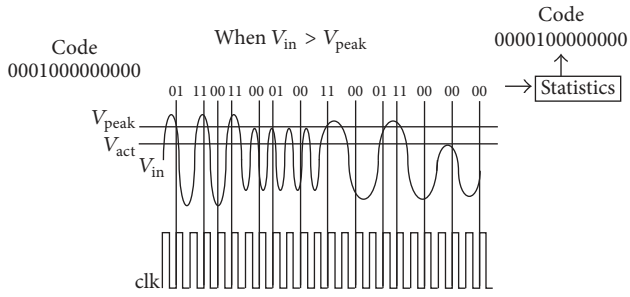

Figure 3: Basis of PSJ logic with multifrequency input.

When voltage supply is 1 V and the full input swing of Sigma-Delta modulator is 400 mV, in order to avoid output distortion, the optimized modulator input is about 250 mV. So V_{peak} is set as $V_{DD}/4$. In case of input noisy signal, the amplitude may be as large as 70~80 mV. To maintain a certain dynamic range, the modulator input amplitude is not less than 90 mV which means V_{act} is $9V_{DD}/100$. Assuming V_{DD} ($A = V_{DD}$) is the power supply voltage, the PGA optimum output is between $(9{\cdot}V_{DD})/100$ (V_{act}) and $V_{DD}/4$ (V_{peak}). Then, put $V_a = (9{\cdot}V_{DD})/100$ and $V_b = V_{DD}/4$ into (3); we get that the $\cos(\pi P(V_a, V_b))$ is 0.98682. So the signal probability $P(V_a, V_b)$ is 0.05175 in the range of $(9 \cdot V_{DD})/100 \sim V_{DD}/4$.

Through simulation, to get precise signal information, it needs to be sampled 600 times for a gain adjustment cycle. On the basis of the probability calculation, we have to get at least 31 sampling points characteristics to judge the right amplitude range of input signal. It means that when more than 31 sampling points output logic "11," the signal amplitude is considered greater than V_{peak}; similarly, meanwhile, when more than 31 sampling points output logic "01," we know the signal amplitude is between V_{peak} and V_{act}. Finally, according to these statistical results, the PSJ logic outputs 13-bit control code to PGA for gain adjustment.

3. Circuit Design

Under low voltage supply such as 1 V, the OTA design is always a great challenge [10–13]. In this paper, the OTA circuit is as shown in Figure 4. It is a full differential Class-AB and Miller compensation structure, including the main amplifier and 2nd-stage common mode feedback (CMFB) amplifier. The main advantage of the two stage structure is the combination of high gain and wide output swing, and it also has better

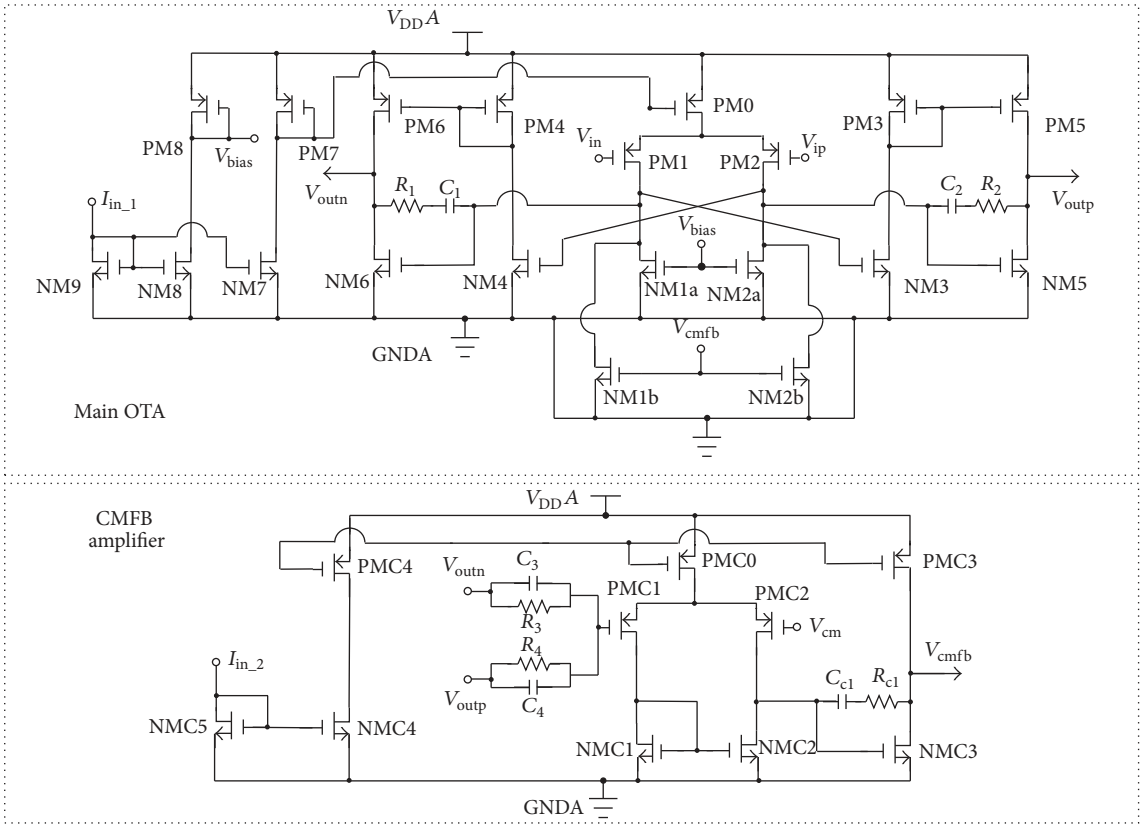

Figure 4: OTA circuit.

noise performance. The first stage amplifier is a five-transistor structure with PMOS input transistors. The load transistors are split into two pairs of transistors NM1a, NM2a and NM1b, NM2b. The NM1a, NM2a are biased at a fixed voltage, and NM1b, NM2b are driven by CMFB amplifier. This scheme effectively reduces the load capacitance of CMFB amplifier, which is conducive to improving the OTA phase margin and frequency characteristics.

Also, the input PMOS transistors can minimize the equal input noise due to its low flick noise, which means for the same output amplitude level the SNR is improved [6–10]. In the second stage, Class-AB composition optimizes the output quiescent current, while achieving a larger output swing.

In this paper, a 2nd-stage CMFB amplifier is adopted for OTA design. In this OTA, the first and second pole are in the drain of PM2/NM2 and PMC2/NMC2, respectively. And they are also very close. Since the third pole is located in the drain of PM5/NM5, the zero-resistance R1/R2 is significant for offsetting the third pole influence to ensure enough phase margins. Finally, the designed OTA demonstrates 83-dB DC gain, 29-MHz unity gain bandwidth, and 61-degree phase margin for a 2-pF load.

For high-resolution comparator design, the dynamic comparator with preamplifier is used in this paper [14]. The main comparator is a regeneration structure that consists of input pairs of PMOS (M2/M3), CMOS latch (M4–M9, M13/M14), and SR latch. NMOS transistor M11 is the reset switch, and the M10 and M12 as assistant transistors are used to reduce the impact of charge injection when M11 is on. The comparator circuit is shown in Figure 5.

4. Measurement Result

Fabricated with SMIC 0.13 μm 1P8M mixed-signal CMOS technology, the AGC chip microphotograph is shown in Figure 6, which occupies the area of 1.127 mm^2.

When input 1 kHz, 200 mVpp sine wave and sampling clock is 1 MHz, the output of AGC is tested in time domain. As Figure 7 shows, the output is adjusted twice to 100 mVpp while the V_{peak} and V_{act} are set as 125 mV and 50 mV, respectively.

Figure 8 shows the measured AGC output FFT spectrum with 2 kHz sinusoidal input and 200 mV output. In this condition, the measured peak SNR is 69.2 dB and the peak THD is 65.3 dB. The results indicate that although it is under the low supply voltage of 1 V, the AGC achieves high output dynamic range.

As the important performance of AGC, the noise performance is also measured. We break the AGC close loop and set the PGA gain manually. Under 2 kHz frequency and 4 mV Vp-p input, Figure 9 indicates the relationship between PGA gain and noise floor.

The result shows that the minimum and maximum noise floor are −111 dBm and −73 dBm, respectively, which are low enough to maintain a high resolution of AGC.

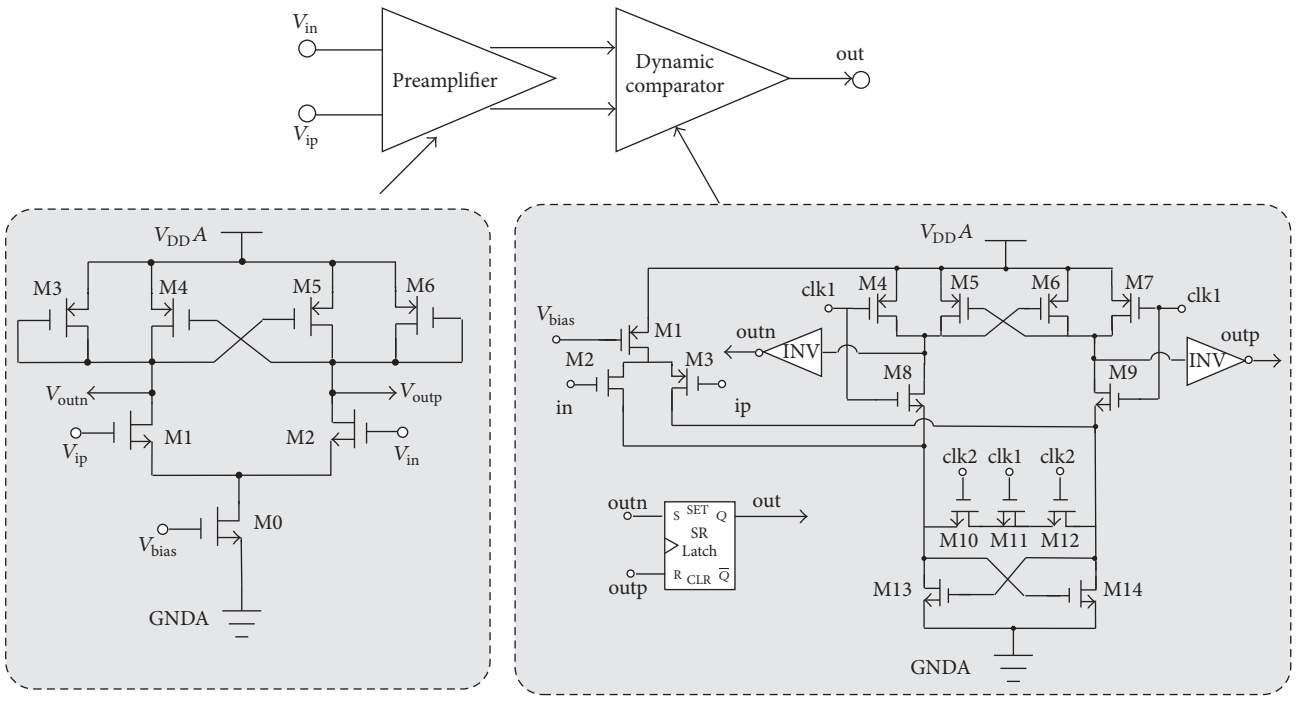

Figure 5: Comparator circuit.

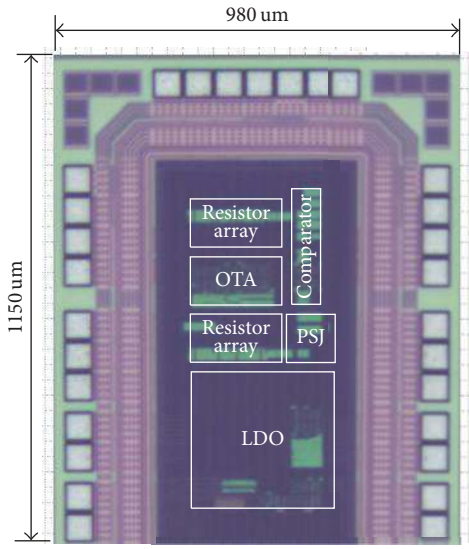

Figure 6: The chip microphotograph of AGC.

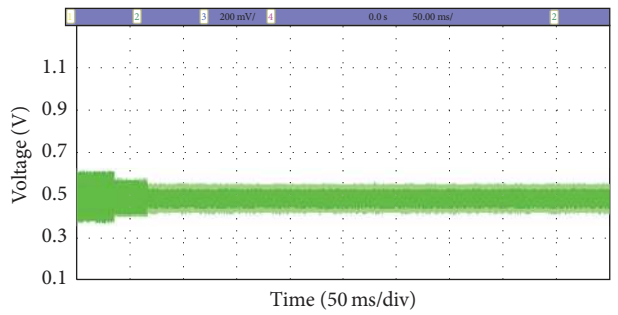

Figure 7: AGC output in time domain.

Table 1: AGC performance summary.

Parameter	AGC
Process	SMIC 0.13 μm 1P8M
Supply voltage	1 V
Signal width	8 kHZ
Minimum noise floor	−111 dBm
SNR peak	69.2 dB@200 mVp-p
THD peak	65.3 dB@200 mVp-p
Power consumption	89 μW
Area	1.15 × 0.98 mm^2

Figure 10 shows the measured SNR as a function of the input signal of 2 kHz. When output amplitude is larger than 300 mV, the SNR reduces.

The proposed AGC performance summary is concluded in Table 1.

The performance comparison of our AGC with previous works is shown in Table 2. Our AGC shows the highest THD of 65.3 dB under 1 V power supply. However, compared with [9], the increase in peak THD is limited. The circuit in [9] used traditional analog envelop detector for gain adjustment, so it can only realize simple peak amplitude control and can not be used in high-resolution multifrequency input condition.

Table 2: Performance comparison of AGC.

Ref	Technology	Supply voltage (V)	Peak THD (dB)	Power consumption (uW)
[6]	1.5 um BiCMOS	2.8	40	34
[7]	0.25 um CMOS	1	44.4	60
[8]	0.35 um CMOS	1	41	100
[9]	0.13 um CMOS	0.8	64	40
This work	0.13 um CMOS	1	65.3	89

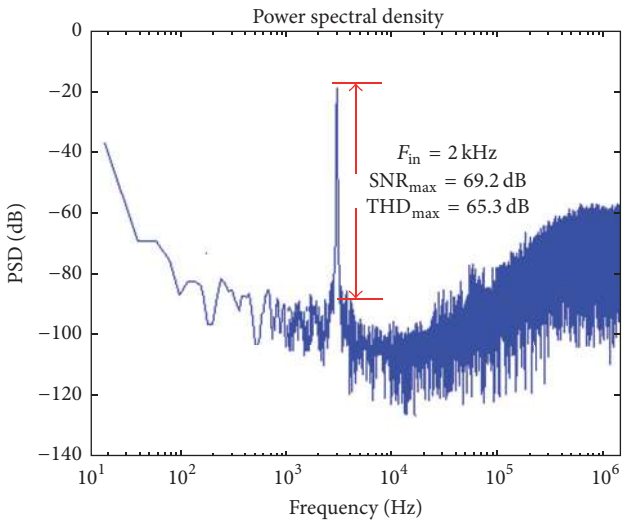

Figure 8: FFT result of output spectrum.

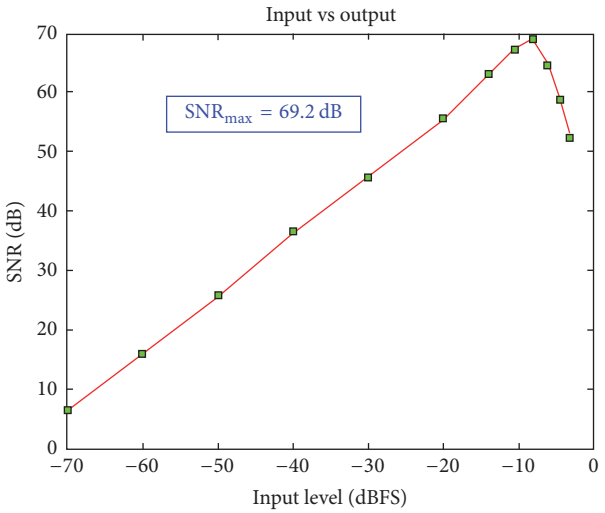

Figure 10: Measured SNR versus input.

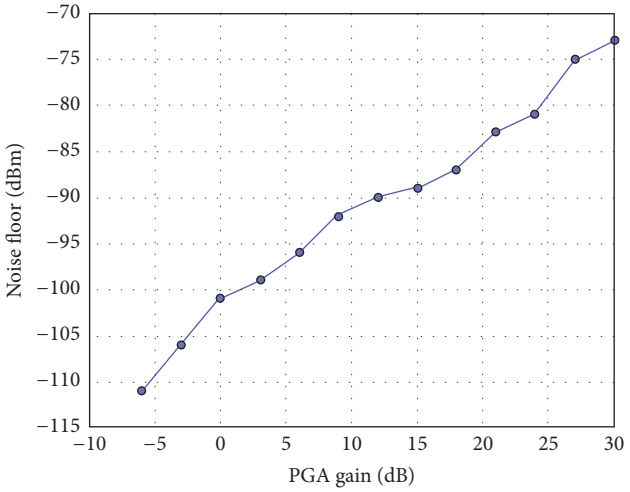

Figure 9: The relationship between PGA gain and noise floor.

5. Conclusion

In this paper, a novel PSJ feedback logic for multifrequency signal application of AGC is proposed. In complex audio signal condition, compared with traditional analog peak envelop-detecting method, it can adjust the gain precisely with 3 dB/step, total 36 dB dynamic range. The PSJ algorithm is implemented in an AGC with 0.13 μm 1P8M CMOS mixed-signal process. In 1 V power supply, the peak SNR of AGC achieves 69.2 dB and total power is 89 uW with 1.127 mm^2 core area. Measurement results satisfy the low-power and high-performance application of hearing aid SoC.

Competing Interests

The authors declare that they have no competing interests.

Acknowledgments

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