A 6X-Voltage-Gain 13-Level Inverter With Self-Balanced Switched-Capacitors

Kasinath JENA, Chinmoy Kumar PANIGRAHI, and Krishna Kumar GUPTA

***Abstract*—In this work, a 13-level inverter is proposed based on the switched-capacitor (SC) technique. The proposed topology (PT) consists of thirteen power switches, four capacitors, and two diodes and achieves a voltage gain of six. The circuit design, operation, and power losses analysis of the PT are described in detail. The most significant features of the PT include: capacitors' voltages are inherently self-balanced, high voltage gain, low component count per level, and ability to supply an inductive load. A simple logic-based multicarrier pulse width modulation technique has been utilized to control the switching operation. More importantly, the overall merit of the PT in terms of the cost function is established using a comparative study with the prior art topologies. Finally, simulation and experimental results have been presented for a rated output of 1.4 kW to validate the performance of the PT at steady-state and dynamic conditions.**

***Index Terms*—Boosting factor, cost function, multilevel inverter, switched-capacitor.**

I. Introduction

MULTILEVEL inverters (MLIs) play a significant role in the power conversion processes in various low, medium, and high power applications. MLIs continue to attract attention from the industry and academia due to their features such as lower dv/dt stress, much-improved waveform, low total harmonic distortion (THD), lower electromagnetic interference, and the possibility of low and high switching frequency operations and higher-efficiency, etc. The classical MLIs are of three types: cascaded H-bridge, neutral point clamped, and flying capacitors MLIs [1], [2]. Classical topologies, on the other hand, are frequently employed in a wide range of industrial applications.

Despite this, they have a number of drawbacks, including unity voltage gain (the ratio of the amplitude of the multilevel output voltage to the amplitude of the input dc voltage), capacitor voltage balancing, and the requirement for a large number of active and passive components due to the increased number of available output levels. To address these issues, several novel topologies have been developed. A recent approach based on the switched-capacitors (SC) technique offers several advantages [3]–[18]: self-balancing of capacitors' voltages as they are brought in parallel with the input source by appropriate switching inherent voltage boosting, and absence of magnetics for voltage boosting. These outstanding features overcome the drawbacks of traditional MLIs. Furthermore, SCMLIs are primarily divided into two types: two-stage SC inverters and single-stage SC inverters.

Two-stage topologies necessitate the use of a back-end H-bridge for the creation of bipolar voltage. As a result, the voltage stress on the H-bridge switches experiences a voltage equivalent to the peak values of the load voltage. As a consequence, two-stage topologies are inappropriate for high voltage applications [3]–[5].

On the other hand, single-stage topologies generate bipolar voltage without using any full-bridge circuit at the back end. In these topologies, in general, the power switches experience low voltage stresses [6]–[20]. Nine-level SC topologies presented in [6]–[8] have effectively reduced voltage stress on the individual switches. The gain, however, is restricted to four times the supply voltage. Additionally, numerous 13-level SC topologies have been proposed recently to provide a cost-effective solution by utilizing several sources or reducing the number of isolated sources, reducing switching components, and reducing the overall cost per level [9]–[18], [23]–[29]. The multi-source 13-level topologies proposed in [9]–[11], [24]–[26], [29] feature a low voltage gain and a high number of active and passive components, which makes them less efficient. Furthermore, the voltage stresses on most individual switches are equivalent to the peak values of the load voltage, and higher levels can be attained by adding an additional number of switched-capacitor cells, resulting in more complex and expensive topologies. [12] proposes a single- source 13-level inverter with a voltage gain of less than twice the input voltage. The topologies discussed in [13], [15] generate $2^{n+1}+1$ levels of the output voltage by the series/parallel configuration of the SC cell. Topology [14] offers the advantage of developing $2n+3$ levels of output voltage while also experiencing minimal voltage stress.

Recently, researchers have focused on the development of cost-effective solutions to achieve higher output voltages levels. For example, few 13-levels topologies based on the SC technique with a gain of six times the supply voltage are presented in [16]–[18]. However, these topologies have higher total standing voltage, maximum blocking voltage, and a significantly high count of the switching components. In view of these discussions, it can be seen that there is ample scope of

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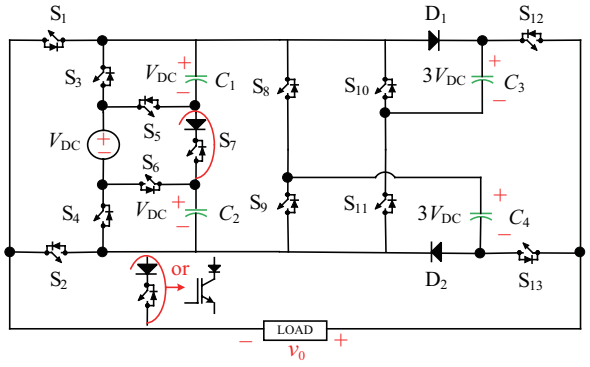

Fig. 1. Proposed 13-level switched capacitor topology.

development of SCMLIs with reduced voltage stress on the switching components, low total standing voltage, and low cost per level, high voltage gain, and capability of handling inductive loads.

In the light of these considerations, a novel SCMLI is proposed in this word. The proposed topology (PT) has the following salient features:

(a) ability to boost the input voltage by a factor of six (i.e., a 6X-voltage-gain)
(b) To generate 13-level waveform, it is necessary to use a single dc power supply.
(c) a lower value of total standing voltage
(d) self-balancing of capacitors' voltages
(e) It can be operated under different load power factors.

Next to this section, the PT and self-balancing mechanisms of the capacitors are presented. A control strategy for the switching of the PT is described in Section III. Section IV presents a comparative analysis with the existing 13-level inverter to prove the merits of the PT. Section VI covers the simulation and experimental results. Concluding remarks are presented in Section VII.

II. The Proposed 13-Level Switched Capacitors Based Inverter

A. Circuit Description

Fig. 1 displays the structure design of the proposed 13-level switched-capacitor inverter topology. The PT consists of 13 switches (S_1–S_{13}), four capacitors (C_1–C_4), two diodes (D_1, D_2), and a single dc source (V_{DC}). It has two kinds of switches. One type comprises a transistor with an antiparallel diode, and the other type comprises a transistor with a series-connected diode. It is noted that only the switch S_7 is of the second type. It is also worth mentioning that among 13 switches, six pairs of switches {S_1, S_2}, {S_3, S_5}, {S_4, S_6}, {S_8, S_9}, {S_{10}, S_{11}} and {S_{12}, S_{13}} and operate in complementary mode and the PT requires only seven driver circuits (dual). The PT synthesizes 13-symmetrical levels at the output, i.e., $\pm 6V_{DC}$, $\pm 5V_{DC}$, $\pm 4V_{DC}$, $\pm 3V_{DC}$, $\pm 2V_{DC}$, $\pm V_{DC}$, and zero. The peak-inverse-voltage (PIV) of all individual switches are tabulated in Table I. Table II Shows the valid switching states of the suggested structure. The output voltage is designated as "v_0". The direction of the load current and charging path of capacitors are marked by red and blue arrow headlines.

TABLE I
Voltage Stress on the Individual Switches

Switch	Voltage stress ($*V_{DC}$)
S_{12}, S_{13}	6
S_1, S_2, S_8, S_9, S_{10}, S_{11}	3
S_3, S_4, S_5, S_6, S_7	1

TABLE II
Valid Switching Combination

States	Active switch	v_0($*V_{DC}$)	Capacitor effects C_1	C_2	C_3	C_4
1	S_1, S_5, S_6, S_8, S_{11}, S_{12}	0	D	D	C	C
	S_2, S_5, S_6, S_8, S_{11}, S_{13}	0	D	D	C	C
2	S_2, S_4, S_5, S_7, S_8, S_{13}	1	D	C	-	D
	S_2, S_4, S_5, S_7, S_8, S_{13}	1	C	D	-	D
3	S_2, S_3, S_4, S_8, S_{13}	2	D	C	-	D
4	S_1, S_5, S_6, S_8, S_{11}, S_{13}	3	D	D	-	C
5	S_1, S_3, S_4, S_9, S_{13}	4	C	D	-	D
6	S_1, S_3, S_6, S_7, S_9, S_{13}	5	C	D	-	D
	S_1, S_4, S_5, S_7, S_9, S_{13}	5	D	C	-	D
7	S_1, S_5, S_6, S_9, S_{13}	6	D	D	-	D
8	S_1, S_3, S_6, S_7, S_{11}, S_{12}	−1	C	D	D	-
	S_1, S_4, S_5, S_7, S_{11}, S_{12}	−1	D	C	D	
9	S_1, S_3, S_4, S_7, S_8, S_{11}, S_{12}	−2	C	D	D	-
10	S_2, S_5, S_6, S_8, S_{11}, S_{12}	−3	D	D	C	-
11	S_2, S_3, S_4, S_{10}, S_{12}	−4	D	C	D	-
12	S_2, S_3, S_5, S_7, S_{10}, S_{12}	−5	D	C	D	-
	S_2, S_4, S_6, S_7, S_{10}, S_{12}	−5	C	D	D	-
13	S_2, S_5, S_6, S_{10}, S_{12}	−6	D	D	D	-

Output voltage $v_0 = (*V_{DC})$, C = charging, D = discharging, "-"idle

B. Working Principle and Self-Balancing Mechanisms of the Switched-Capacitor

The only positive half-cycle has been considered to facilitate the working analysis because the proposed topology has a symmetrical operation. Fig. 2 and Table II illustrate the investigation of various operating conditions for the positive half cycle. Using series-parallel connections, the voltage across the capacitors C_1–C_2 and C_3–C_4 is maintained at V_{DC} and $3V_{DC}$, respectively. In other words, capacitors are self-balanced without the need for any additional sensor or balancing circuit. This the prominent feature ensures the self-balancing properties of the capacitors. In detail, the input source is combined with the voltages of the capacitors C_1–C_2 to charge C_3–C_4 (i.e., $3V_{DC}$ each) during the zero levels. $\pm 1V_{DC}$ and $\pm 2V_{DC}$ generated by the capacitor C_3 or C_4. The voltage levels $\pm 3V_{DC}$ are generated by adding the capacitors C_1–C_2 voltage with the input source. Afterward, the capacitors (C_3 or C_4) voltage is added with the input source to produce $\pm 4V_{DC}$ levels. $\pm 5V_{DC}$ levels can be generated by adding the capacitors voltage C_3 or C_4 with the voltage of the capacitor C_1 or C_2 along with the input source.

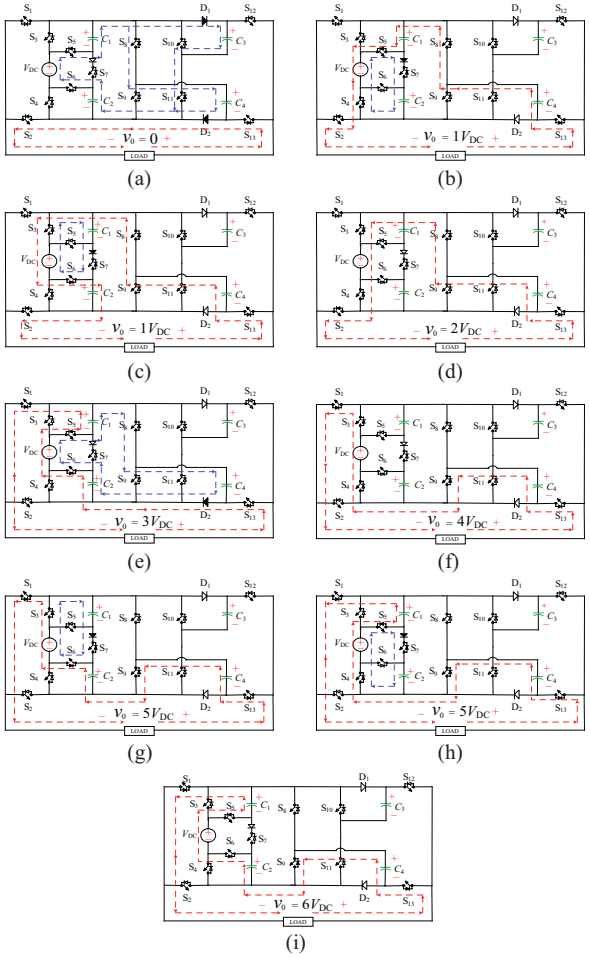

Fig. 2. Various operating states for the positive half cycle of the proposed topology.

$\pm 6V_{DC}$ Levels are produced by adding the capacitors voltage C_1–C_2 and C_3 or C_4 with the input source.

C. Determination of Capacitance

When the capacitor is charged, the voltage ripples occur. These voltage ripples cause extra power losses in the SCMLIs. Therefore, it is necessary to design the SCMLIs with an appropriate capacitance value to reduce the voltage ripple. The importance of capacitance depends upon the following factors: voltage ripple (ΔV_C), peak values of load current (I_l), and the power factor of the load (φ) [3].

The maximum discharging amount of charge (ΔQ_i) of the capacitor can calculate as:

$$\Delta Q_i = \int_{t_x}^{t_y} I_1 \sin(\omega t - \varphi) \mathrm{d}t \tag{1}$$

Where, ($t_x - t_y$) is the longest discharging period.

The values of t_1, t_2, t_3, t_4, t_5, shown in Fig. 3 can be expressed as [14]

$$t_1 = \frac{\sin^{-1}(\frac{1}{6})}{2\pi f_0} \tag{2}$$

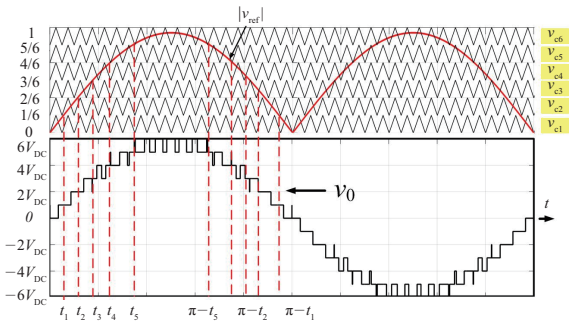

Fig. 3. Reference, carrier wave and output voltage.

$$t_4 = \frac{\sin^{-1}(\frac{4}{6})}{2\pi f_0} \tag{3}$$

$$t_5 = \frac{\sin^{-1}(\frac{5}{6})}{2\pi f_0} \tag{4}$$

Assume the inverter is operated for a resistive load (R), the load current $I_1 = \frac{v_o}{R}$ and the voltage ripples can be expressed as:

$$\Delta V_{C1} = \frac{V_{DC}}{2\pi R f_0}(6\pi - t_1 - t_2 + 3t_3 - 5t_4 - 7t_5) \tag{5}$$

$$\Delta V_{C2} = \frac{V_{DC}}{2\pi R f_0}(6\pi + t_1 - 3t_2 - t_3 + 4t_4 - 7t_5) \tag{6}$$

$$\Delta V_{C3} = \Delta V_{C4} = \frac{V_{DC}}{2\pi R f_0}(6\pi - 2t_1 - 2t_2 - 4t_3 - t_4 - 7t_5) \tag{7}$$

Therefore, the capacitance C_i can be calculated as [14]

$$C_i > \frac{\Delta Q_i}{\Delta V_{Ci}} \tag{8}$$

III. Control Strategy

There are several control strategies implemented for multilevel inverters. In this paper, the multicarrier level-shifted PWM has been employed. The switching pulse is determined by comparing twelve carriers (v_{c1}–v_{c12}) signals with a sinusoidal signal (v_{ref}). Each carrier has the same peak to peak amplitude and frequency. The reference, carrier wave, and output voltage waveform are shown in Fig. 3. Fig. 4 illustrates a simplified logic-based LS-PWM scheme for the positive half cycle, and a similar arrangement may be created for the negative half cycle. A simple logical operation that generates the switching pulses is expressed in the equation (4)–(16). The modulation index is defined as the magnitude of the reference signal divided by the amplitude of the carrier signal.

$$S_1 = y_1 + x_3 + y_4 + x_4 + y_5 + x_5 + y_6 + x_6 + x_{11} + y_{22} + x_{22} + y_{33} \tag{9}$$

$$S_2 = y_{11} + x_1 + y_2 + x_2 + y_3 + x_{33} + y_{44} + x_{44} + y_{55} + x_{55} + y_{66} + x_{66} \tag{10}$$

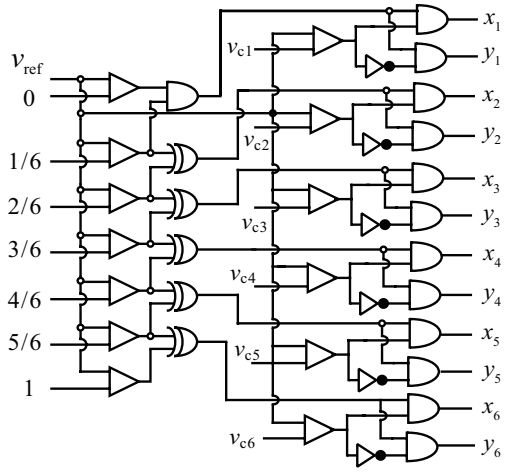

Fig. 4. LS-PWM modulation scheme.

$$S_3 = x_2 + y_3 + x_4 + y_5 + x_5 + y_6 + x_{44} + y_{55} + x_{11} + y_{22} + x_{22} + y_{33} + x_{55} + y_{66} \quad (11)$$

$$S_4 = x_1 + y_2 + x_2 + y_3 + x_{22} + y_{33} + x_{44} + y_{55} \quad (12)$$

$$S_5 = y_1 + y_{11} + x_1 + y_2 + x_3 + y_4 + x_6 + x_{33} + y_{44} + x_{66} + x_{55} + y_{66} \quad (13)$$

$$S_5 = y_1 + y_{11} + x_1 + y_2 + x_3 + y_4 + x_6 + x_{33} + y_{44} + x_{66} + x_{55} + y_{66} \quad (14)$$

$$S_6 = y_1 + y_{11} + x_3 + y_4 + x_5 + y_6 + x_6 + x_{11} + y_{22} + x_{33} + y_{44} + x_{66} \quad (15)$$

$$S_7 = x_1 + y_2 + x_5 + y_6 + x_{11} + y_{22} + x_{22} + y_{33} + x_{55} + y_{66} \quad (16)$$

$$S_8 = y_1 + y_{11} + x_2 + y_3 + x_3 + y_4 + x_{22} + y_{33} + x_{33} + y_{44} \quad (17)$$

$$S_9 = x_4 + y_5 + x_5 + y_6 + x_6 \quad (18)$$

$$S_{10} = x_{44} + y_{55} + x_{55} + y_{66} + x_{66} \quad (19)$$

$$S_{11} = y_1 + y_{11} + x_3 + y_4 + x_{11} + y_{22} + x_{22} + y_{33} + x_{33} + y_{44} \quad (20)$$

$$S_{12} = y_1 + x_{11} + y_{22} + x_{22} + y_{33} + x_{33} + y_{44} + x_{44} + y_{55} + x_{55} + y_{66} + x_{66} \quad (21)$$

IV. Comparative Study With the Existing Topologies

The comparative study has been accomplished in this section to assess the merits in terms of voltage gain, blocking voltage, DC links, per unit total standing voltage (TSV_{pu}) and cost function against similar topologies. The brief comparative studies have been highlighted in Table III. Table III shows that the topologies [3] and [5] require a back-end H-bridge and more active and passive components than the PT.

The topologies introduced in [10]–[12] capable of generating 13-level exhibit a voltage gain less than the PT; thus, an additional voltage boosting device/circuit is needed. Moreover, the topologies [10]–[11] require multiple DC sources, making them complex and costly. By comparing the whole design to previous topologies in terms of TSV_{pu} and cost function gives an improved design for the PT. The cost function determines the cost per level of the output voltage. Mathematically it can be written as [22]

$$CF = \frac{(N_{sw} + N_d + N_{dri} + N_c + \alpha TSV_{pu}) \times N_s}{N_l} \quad (22)$$

And part count per level ($F_{C/L}$) can be defined by

$$F_{C/L} = \frac{N_{sw} + N_c + N_d + N_{dri}}{N_l} \quad (23)$$

The per-unit total standing voltage may be defined as the ratio of the sum of the total blocking voltage of all the switches and peak inverse voltage of the diode to the peak values of the load voltage. The cost function depends upon both components and per unit total standing voltage. When components counts are given more priority than the per-unit total standing voltage, the weight factor (α) is taken as less than one, otherwise greater than one. However, when both the components count and per unit total standing voltage are given equal importance, then the weight factor is considered as $\alpha = 1$.

As per Table III, the topologies [3], [5]–[8], [10]–[12], [14], [19] have a higher cost function per gain. Moreover, topologies [10]–[11], [19] has multiple input source; henceforth these topologies are bulkier and complicated. Even though topology [17] has the lowest cost function, it necessitates a more significant number of uncontrolled power switches.

The reference [20]–[22] has a cost function per gain higher than the PT for the values of $\alpha = 0.5$ and $\alpha = 1.5$. Moreover, the PT has a higher gain than [20]–[22]. As a result, the suggested topology eliminates the need for an additional boosting circuit.

As per Table III, the topology [16] has the same power semiconductor switches and diodes. However, the requirements of the gate driver circuit are more for the [16]. This feature makes part counts per level more than the PT, which justified the topology [16] bulkier. Moreover, when $\alpha = 0.5$, the PT has a lower cost function per gain and hence more cost-effective. Moreover, there is the continuous discharge of capacitor C_3 to the load, for the level of $\pm 4V_{DC}$ to $\pm 6V_{DC}$ i.e., both in the positive and negative half cycle, which in turn makes higher voltage ripples across C_3.

The same level topologies [23]–[29], indicating that the PT has a lower *CF/G* ratio. Additionally, the topologies [23], [25], [28], [29] include a more significant number of $(TSV + PIV)_{pu}$ than the PT. The input source [24]–[26], [29], has various input sources, making the system large and expensive.

V. Loss Analysis

There are three types of losses in the PT: switching losses, conduction losses, and capacitor ripple losses.

A. Switching Losses(P_s)

The power loss due to semiconductor switches' turn-on/turn-off processes is known as switching losses [4]. The sum of switching losses during turn-on and turn-off is known as overall switching losses. Therefore, it can be written as :

$$P_{sw\_on} = \frac{1}{6} f_0 V_{on} I_{on} t_{on} \quad (24)$$

TABLE III
COMPARATIVE ANALYSIS WITH RECENT TOPOLOGIES

Ref	N_l	N_{sw}	N_c	N_d	N_{dri}	N_s	B	G	$(PIV+TSV)_{pu}$	$F_{C/L}$	$GF/G[\alpha=0.5]$	$GF/G[\alpha=1.5]$
[6]	9	12	2	-	9	1	2	4	5.25	2.55	0.711	0.857
[7]	9	8	3	3	4	1	4	4	5.75	2	0.579	0.718
[8]	9	12	3	-	9	1	4	4	6	2.66	0.75	0.916
[3]	13	19	5	-	12	1	6	6	7.33	2.77	0.508	0.602
[5]	13	10	5	10	7	1	6	6	8.16	2.48	0.462	0.567
[10]	13	16	4	2	9	2	6	3	6	2.38	1.743	2.051
[11]	13	14	2	-	7	2	6	2	7.5	1.77	2.057	2.634
[12]	13	14	4	-	6	1	1	1.5	5	1.84	1.358	1.615
[14]	13	29	5	-	22	1	1	6	10.5	4.31	0.852	0.919
[17]	13	10	4	4	5	1	6	6	6	1.77	0.333	0.410
[19]	13	10	-	-	8	4	6	1.5	5.33	1.38	4.238	5.33
[20]	7	12	2	-	7	1	2	3	5.33	3	1.127	0.538
[21]	9	10	2	-	6	1	2	2	6	2	1	1.555
[22]	11	8	-	-	4	3	5	1.65	4.4	1.09	2.347	3.074
[16]	13	13	3	2	9	1	3	6	4.5	2.1	0.375	0.384
[23]	13	24	5	-	17	1	2	6	7	3.53	0.589	0.724
[24]	13	18	6	6	9	3	4	2	5	3	1.596	1.788
[25]	13	16	4	4	8	2	4	3	6	2.46	1.794	2.102
[26]	13	13	2	-	9	2	6	1.5	4.67	1.84	1.59	3.18
[27]	13	25	6	-	16	1	6	6	5.83	3.61	0.639	0.714
[28]	13	14	4	-	6	1	6	3	6	1.84	0.692	0.846
[29]	13	10	1	-	9	2	6	2	6.5	1.53	1.788	2.288
[P]	13	13	4	2	7	1	6	6	5.83	2	0.346	0.445

N_l: No. of level, N_{sw}: No. of switches, N_c: No. of capacitors, N_d: No. of diodes, N_{dri}: No. of the driver unit, N_s: No. of sources, B: Max. blocking ,voltage, G: Gain, $(PIV+TSV)_{pu}$: Per unit total standing voltage, $F_{C/L}$: component count per level, CF: Cost factor, [P]: Proposed topology.

$$P_{sw\_off} = \frac{1}{6} f_0 V_{off} I_{off} t_{off} \tag{25}$$

$$P_s = \sum [P_{sw\_on} + P_{sw\_off}] \tag{26}$$

Where, V_{on}, V_{off} be the voltage across the switches before turn-on and after the turn-off, respectively. I_{on}, I_{off} be the current flowing through the switches after turn-on and before the turn-off, respectively, and t_{on}, t_{off} be the turn-on and turn-off time of the switch.

B. Conduction Losses(P_c)

When current flows through a transistor or a diode, the internal resistance of the transistor or diode cause losses, and this loss is known as conduction losses [14], [4]. As a result, these conduction losses are represented as:

$$P_{c\_s} = V_{on\_s} I_{s\_avg} + R_{on\_s} I^2_{s\_rms} \tag{27}$$

$$P_{c\_d} = V_{on\_d} I_{d\_avg} + R_{on\_d} I^2_{d\_rms} \tag{28}$$

C. Capacitor Ripple Losses (P_{rip})

The capacitors become charged when they are connected in parallel with the input source. During this time of charging, capacitor ripple losses occur. In the switched capacitor with current i_{c_i}, the voltage ripple is calculated as [3]:

$$\Delta V_{c\_i} = \int_{t_x}^{t_y} i_{c\_i} dt \tag{29}$$

As a result, ripple losses can be stated as follows:

$$P_{rip} = \frac{f_{ref}}{2} C(\Delta V_c^2) \tag{30}$$

VI. RESULTS AND DISCUSSION

The results of experiments and simulations are presented in the following sections to demonstrate the theoretical analysis feasibility and precision.

A. Simulation Results

MATLAB/Simulink environment has been used to verify the theoretical concept of a 13-level boost inverter. The values of the parameters utilized in the circuit modeling and experiments are listed in Table IV.

TABLE IV
CIRCUIT SIMULATION & EXPERIMENTAL PARAMETERS

Device/Conditions	Units
DC voltage	100 V, 200 V
Capacitor $C_1 = C_2$	6000 µF
$C_3 = C_4$	4700 µF
Inductive load	120 mH,160 mH
Resistive load	50 Ω,100 Ω
Load frequency	50 Hz
Switching frequency	2 kHz
Modulation index	0.95

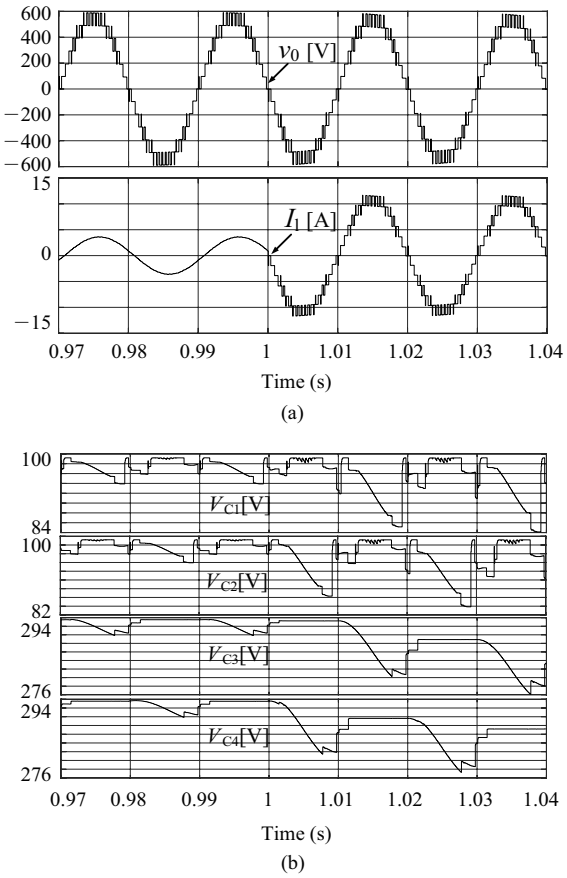

Fig. 5. Shows the simulation results (a) load voltage and load current (b) capacitors voltage.

The simulation results of the suggested inverter are depicted in Fig. 6. The 13-level staircase output voltage and load current waveforms under a step-change load are shown in Fig. 5(a). When the load is suddenly switched from resistive-inductive (R = 100, L = 120 mH) to pure resistive (R = 50), the amplitude of the output voltage waveform and the number of levels remain stable. The capacitor charging and discharging characteristics during the dynamic/step-changing load is depicted in Fig. 5(b). It can be observed that the capacitors maintained their nominal values under various loading conations without the need for any external control mechanism.

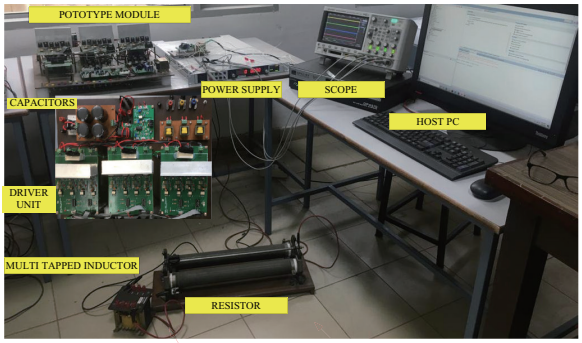

Fig. 6. Experimental setup.

TABLE V
LOSS DISTRIBUTION

Switch	Switching losses (W)	Conduction losses (W)
S_1	1.53	1.181
S_2	1.426	1.208
S_3	3.147	0.1617
S_4	3.148	0.1617
S_5	2.549	1.963
S_6	2.601	1.963
S_7	2.153	0.935
S_8	2.186	0.2636
S_9	1.054	1.044
S_{10}	1.055	1.044
S_{11}	1.885	0.2429
S_{12}	0.4196	1.289
S_{13}	0.3188	1.314

The PT has been simulated on the PLECS environment to determine the switching and conduction losses. The loss distributions are shown in Table V. According to the FFT analysis, a resistive, inductive load (R = 100 Ω, L = 120 mH) provides the rms values fundamental voltage v_0 = 385.4 V with THD (total harmonic distortion) 10.74% and fundamental values of rms current i_0 = 3.605 A with THD (total harmonic distortion) 10.74%. In addition, the suggested topology capacitor ripple losses may be calculated using (25), which is 16.71 W. As a result, the recommended topology's overall efficiency is 96.3%.

B. Experimental Results

To prove the feasibility of the proposed topology, a laboratory prototype module shown in Fig. 6 has been built for experimental validation, and their performances are judged through steady-state and dynamic conditions. The parameters used for the experimental setup are listed in Table IV.

1) Steady-State Analysis

The performances of the proposed inverter are tested under the steady-state condition with a resistive –inductive load (100 Ω, 120 mH). The experimental waveforms for the steady-state

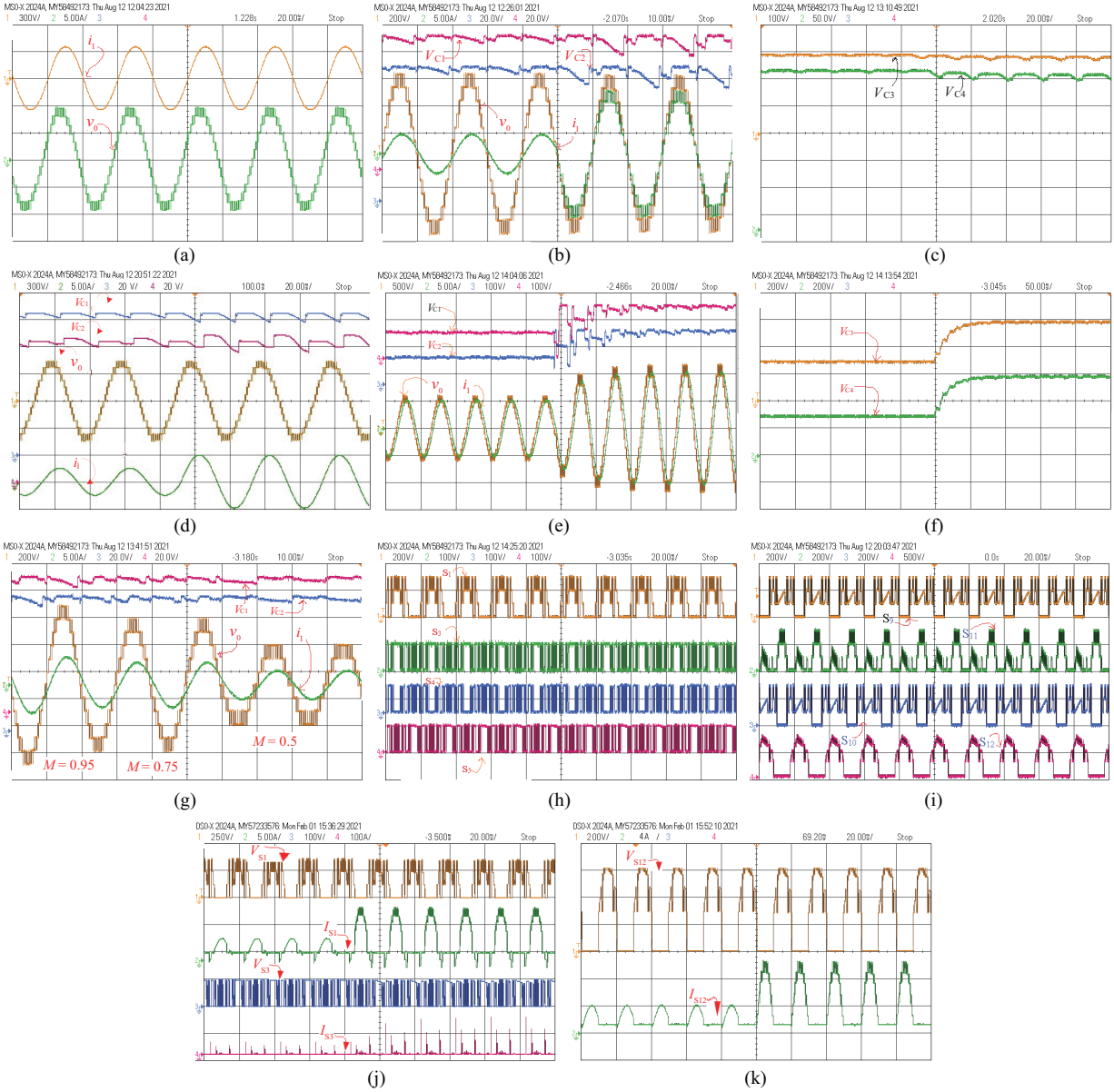

Fig. 7. Shows the Experimental outcomes (a) steady state load voltage, load current, (b–c) dynamic response of output voltage current and capacitor voltage for resistive inductive load, (d) dynamic response of voltage current and capacitor voltage for inductive load, (e–f) dynamic response voltage current for supply voltage, (g) dynamic response of voltage current when amplitude of modulation index change, (h–i) voltage stresses of S_1–S_4, and S_9–S_{12}, (j–k) voltage and current stresses of S_1, S_3, and S_{12}.

are shown in Fig. 7(a). It has been seen that the output voltage is a staircase waveform. Each step of the output voltage is identical in magnitude, and the output voltage's peak value is six times the input voltage, demonstrating the voltage boosting capacity.

2) Dynamic Results Analysis

Fig. 7(b–c) introduced dynamic condition results under step change in load (100 Ω, 120 mH to 200 Ω). It has been seen from Fig. 7(b), that the SC topology synthesizes a 13-level staircase output voltage waveform with a peak value six times the input voltage, and its values remain unchanged when a sudden change in load is applied. It has also been observed that the capacitor's voltage maintains its self-regulating properties. Fig. 7(d) shows the step change in load (100 Ω,120 mH to 100 Ω,160 mH). These experimental results prove that's the proposed inverter is capable of supply inductive load.

Further investigation of change in supply voltage is shown in Fig. 7(e–f). It has been observed that when the supply voltage change from 100 V to 200 V, the proposed inverter performs well during the change in supply voltage condition and quickly reached the new steady-state value.

The experimental results for the change in amplitude of modulation index are shown in Fig. 7(g). When the amplitude of the modulation index is adjusted from 0.95 to 0.75 and 0.75 to 0.5, it can be seen that the output voltage changes its voltage level from 13 to 11 and 11 to 7. This change in modulation

index completes the transient response very fast and shows excellent performance of the proposed 13-level inverter.

Moreover, voltage stresses across S_1–S_4, S_9–S_{12} are displayed in Fig. 7(h–i). Voltage and current stresses of S_1, S_3, S_{12} are shown in Fig. 7(j–k)which justifies the theoretical results.

Finally, both the simulations and experimental results agree with the theoretical results and prove the feasibility and correctness of the proposed topology.

The suggested topology has an experimental efficiency of 95.8%, somewhat lower than the PLECS-based model. This is due to the drivers' units ,have suffered some losses.

VII. Conclusion

This paper presents a high gain 13-level SC inverter. The topology description, modes of operation, the self-balancing effect of capacitors, modulation strategy, and power losses analysis have been addressed in detail in this paper. A fair comparative study with multiple selective topologies proves the merits and competitiveness of the PT in terms of reduced switching components, drivers, cost function per gain, and high gain. These essential features of the PT make it more advantageous than other existing topologies. Finally, simulation and experimental studies have been used to determine the effectiveness and practicality of the PT under steady-state and transient situations.

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