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A 7.9 mW, 5.6 GHz digitally controlled Variable Gain Amplifier with Linearization

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***Abstract*—This paper presents the design and validation of a compact high performance digitally controlled variable gain amplifier (DVGA). By using MOS switches and a linearizer, the designed DVGA demonstrates high linearity and gain flatness over a wide gain control range. The 6-bit DVGA is designed in a commercial 0.18 μm SiGe BiCMOS technology achieving a variable gain range from -16.5 dB to +6.5 dB, a 3-dB bandwidth from DC to 5.6 GHz, a ± 0.75-dB gain flatness from DC to 4 GHz, both input and output return loss greater than 15 dB, consuming 7.9 mW over the entire gain control range and has a core circuit area of 170 μm x 60 μm.**

***Index Terms*— Digitally controlled, Linearizer technique, Low power design, Millimeter-wave, Silicon Germanium (SiGe) BiCMOS, variable gain amplifier, VGA, 60 GHz Communication**

I. INTRODUCTION

AUTOMATIC gain control (AGC) is extended to Radio Frequency transceivers to provide constant signal strength to the analog to digital converters (ADC) in digital baseband, even with varying signal strength across the channel between the transmitter and receiver [1]. The variable gain amplifier (VGA) circuit in the AGC performs the key function of varying the gain and attenuation in accordance with the input signal strength acquired by the digital baseband portion as shown in Fig. 1. By using the feedback control mechanism, the AGC holds its output signal strength to a predetermined fixed level [2], [3]. In a RF transceiver, the VGA is required to achieve a stable gain control without altering the DC power consumption, bandwidth, stability, input/output return loss and maintain the signal power strength for digital baseband.

Based on the techniques for gain variation, the VGA can be classified as continuous or analog gain control VGA (CVGA) [1]-[10] and discrete step or digital gain control VGA (DVGA) [11]-[14]. In CVGA the digital baseband requires a digital to analog converter (DAC) to control the gain, increasing the circuit complexity. DVGA can be interfaced directly with the digital baseband without the need for a DAC

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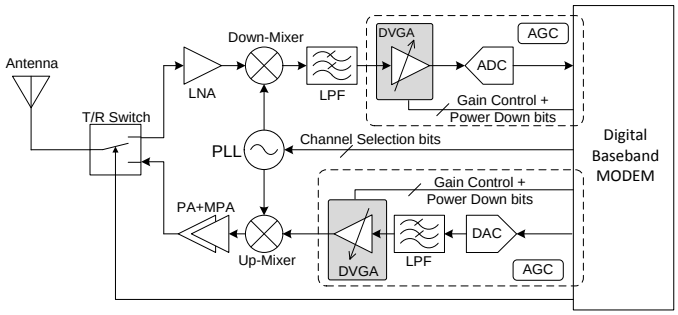

Fig. 1. RF Transceiver architecture

to accept digital gain control information as shown in Fig. 1. From the literature, a DVGA can be implemented by switching between various fixed gain stages [12] or by using binary weighted arrays of circuit components selected discretely using switches [11], [13], [14]. This switching either by gain stages or by circuit components is finally reflected in VGA gain step variation. While the switching gain stage DVGA consumes more power and larger die area due to design redundancy, the DVGA with switching between circuit components are compact consuming less power and die area. Although the state of art VGA designed in CMOS process [2]-[4], [6]-[11], [13], [14] have a few advantages, such as large dynamic range with low power consumption, they also possess the transconductance [8] with square law characteristics as shown in (1).

$$g_{m,CMOS} = \frac{\delta I_D}{\delta V_{GS}} = \sqrt{2\,\beta\, I_D} \tag{1}$$

where, I_D and V_{GS} are the bias point drain current and the gate to source voltage, with β as MOS transistor process parameter.

To achieve linear gain variation based on the transistor bias current (I_D), the CMOS DVGA requires additional corrective circuits. The proposed DVGA is based on the bipolar devices and simplifies the gain control technique by varying the bias current using digital switches. This method ensures the advantage of implementing a DVGA with simple topology, direct switch control using current mirrors and avoiding additional corrective circuits. Also, in a CMOS VGA the DC offset saturates the next stage amplifier, limiting the bandwidth to start from a higher frequency than DC (f = 0 Hz). To overcome these limitations, the CMOS VGA needs additional corrective circuits [8].

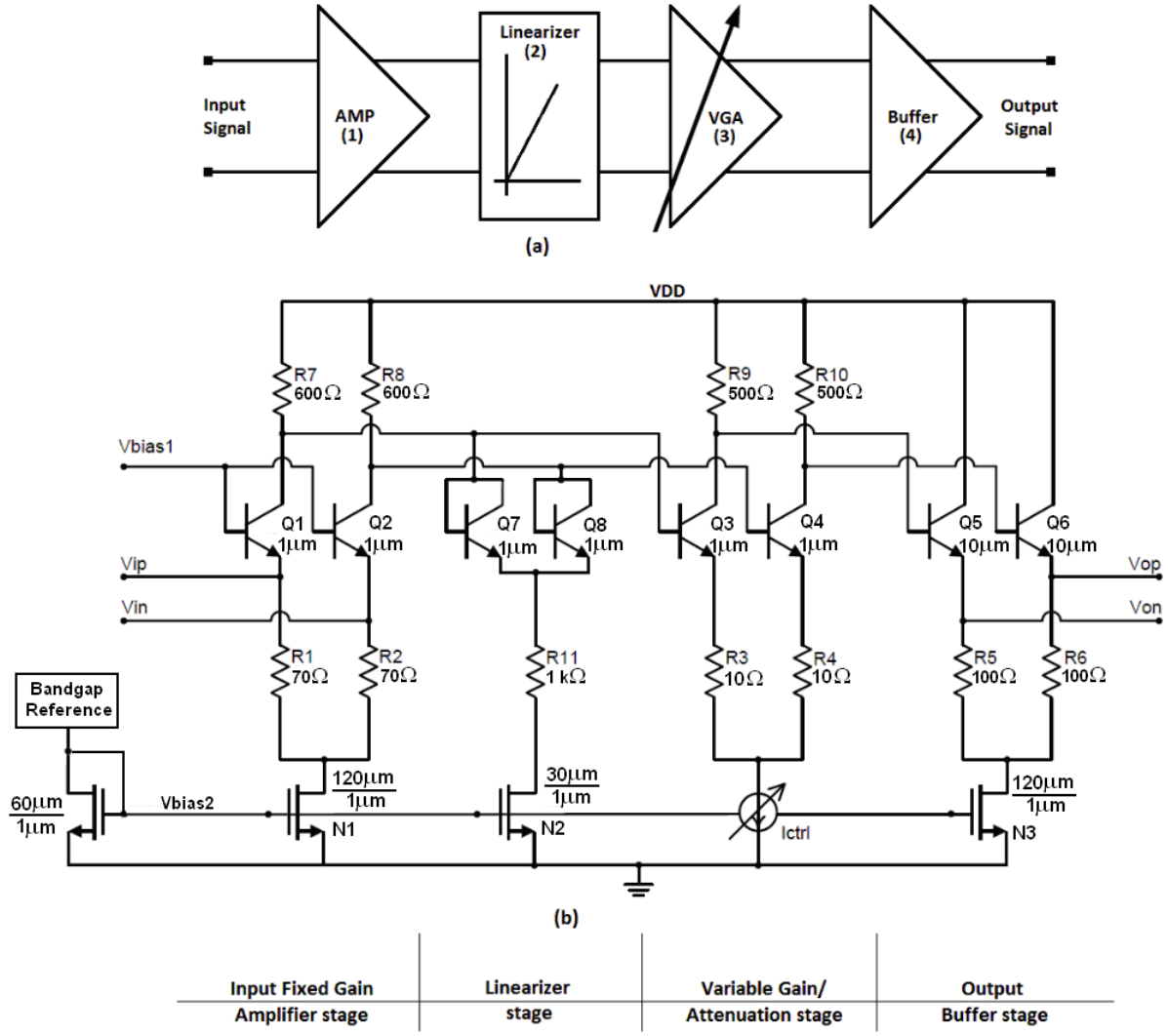

Fig. 2. Proposed DVGA (a) Block diagram (b) circuit schematic

A desirable quality of an amplifier is higher linearity, which determines the maximum signal level that can be amplified without any distortion in the output signal. The distortion is caused due to the circuit components entering their non-linear operating region due to large input signal. The technique of diode-connected linearizer used in power amplifier designs [15]-[17] improves the linearity of the amplifier, although they require an additional reference voltage that may be higher than the supply voltage to bias the linearizer diode.

The proposed design's simulation performance was described in [18]. This paper proposes the design of a high performance DVGA based on the digital gain control by using SiGe BiCMOS HBT as the amplifying device and the amplifier transconductance is varied in steps by using NMOS switches. In this design, the technique of diode-connected linearizer is further extended to improve linearity of the proposed DVGA by eliminating additional reference voltage. The proposed DVGA utilizes the circuit architecture advantages of both HBT and MOS devices to easily generate linear gain variation, large dynamic range, wide bandwidth, low power consumption and compact die size.

This paper is organized with Section II describing the circuit topology and deducing the analysis of the proposed design, Section III provides the experimental results that are proven using on-wafer measurement and the conclusion of paper is in Section VI.

II. Circuit Topology And Analysis

A. Circuit Description

Fig. 2 (a) shows the block diagram of the proposed fully differential DVGA comprises of four cascaded stages –input fixed gain stage, linearizer stage, variable amplifier/attenuator stage and output buffer stage. The four stages are biased using the NFET current sinks (N1, N2, I_{ctrl} and N3) as depicted in Fig. 2 (b). Each stage for the proposed DVGA is selected thoughtfully to meet the stringent design requirement.

The current sink transistors (N1, N2, I_{ctrl} and N3) provide a stable DC bias point with fixed drain current and drain to source voltage (V_{DS}) making the design stages insensitive to process variations. In the transceiver system, the current for biasing the DVGA amplifier stages and the gain control switches is derived from the common bandgap reference that provides a PVT (Process-Voltage-Temperature) insensitive current. This current is mirrored using MOS transistors to

obtain the DVGA bias (Vbias2) as shown in Fig. 2 (b), ensuring the biasing current and the V_{DS} of the current sink transistors are constant under the PVT variations. With current mirror biasing, we can either power ON or power down the whole circuit using a digital MOS switch. This power down option helps to switch off the corresponding DVGA when either the transmitter or receiver chain is non-functional. This prevents power drain and enables low power transceiver designs. In this design, a digital pin (Pwr_Dwn) is provided externally to shutdown (Pwr_Dwn = 1.8 V) or power ON (Pwr_Dwn = 0 V) the DVGA.

Since the differential CE stage consumes smaller DC current compared to the DC current consumption of the overall proposed DVGA, the DC power dissipated across R3 and R4 resistors are insignificant. One of the benefits of the resistors R3 and R4 in the design is to provide a small bandwidth improvement.

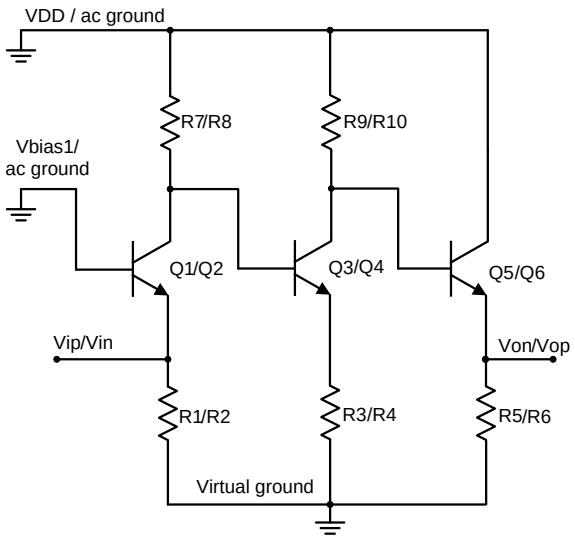

Fig. 3. AC equivalent half circuit schematic

B. Small signal analysis of fixed and variable gain stages

The AC equivalent half circuit of Fig. 2 (b), excluding the 2nd stage linearizer is shown in Fig. 3. Since the linearizer affects only the large signal performance, it can be neglected for small signal analysis. The small signal model for analysis is shown in Fig. 4. This proposed design is analyzed for small signal performance parameters for the cascaded gain stages.

The input common base (CB) stage of the DVGA provides a return loss greater than 15 dB over wide bandwidth and a fixed gain independent of DVGA gain settings.

Since the resistance (50 Ω) looking into transistor's emitter terminal (2) is small, the input pole due to emitter-base junction capacitance (18.4 fF) is shifted to very high frequency (greater than 100 GHz). The base terminal is set to AC ground nullifying the Miller capacitive contribution and the input impedance becomes resistive over a wide bandwidth with the smaller resistance (2) achieving a return loss greater than 15 dB for the proposed DVGA.

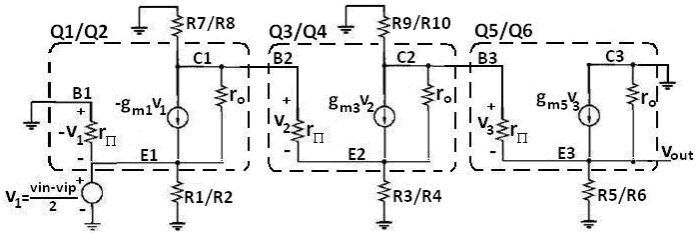

Fig. 4. Small signal model of the proposed DVGA half circuit

$$R_{in} = \frac{v_{input}}{i_{input}} = R_{1,2} \parallel \frac{r_\pi}{(\beta+1)} = R_{1,2} \parallel \frac{1}{g_{m1}} \tag{2}$$

where it is assumed that all the HBT transistors have the same base resistance r_π, output resistance r_o and transistor current amplification factor β. g_{mi} represents the transconductance of Qi (i = 1 to 6) transistors.

The common emitter (CE) variable gain stage (third stage of DVGA) is designed with the option to vary the transconductance g_{mi} of transistors Q3/Q4 that eventually sets the DVGA gain.

The DC collector current of Q3 and Q4 is set by NFET current sinks (I_{ctrl}) as shown in Fig. 5. The variable gain and attenuation of this stage is achieved by varying the current biasing point of the HBT pair Q3/Q4. The total DC emitter current and collector current of the transistors are given by,

$$I_{ET} = \frac{I_{CT}}{\alpha} \tag{3}$$

$$I_{CT} = I_0 . e^{\left(\frac{Vbe}{\eta . V_T}\right)} \tag{4}$$

where the common base current amplification factor α, reverse saturation current of the base emitter junction I_0, ideality factor η and thermal voltage V_T are for transistor pair (Q3/Q4).

The CE stage transconductance is given by,

$$g_{m3} = \frac{\delta I_{CT}}{\delta V_{be}} = \frac{I_0 . e^{\left(\frac{Vbe}{\eta . V_T}\right)}}{\eta . V_T} = \frac{I_{CT}}{\eta . V_T} \tag{5}$$

Since the DVGA stages are cascaded, its small signal gain is also determined by the voltage gain of the CE stage given by,

$$A_{v2} = \frac{g_{m3} R_{9,10}}{(1 + g_{m3} R_{3,4})} \tag{6}$$

When, $g_{m3} . R_{3,4} << 1$, the voltage gain is reduced to,

$$A_{v2} = g_{m3} R_{9,10} \tag{7}$$

From (3), (5) and (7), it can be deduced that the overall DVGA small signal gain is determined by current I_{ET}. The

linear DVGA gain variation is achieved by carefully scaling the NFET current sinks (I_{ctl}). The current distribution of I_{ET} determining the linear gain variation based on digital gain control bits is shown in Fig. 5 and is given in (8) and (9),

$$I_{ET} = B_0.I_0.2^0 + B_1.I_1.2^1 + ... + B_5.I_5.2^5 + I_{\min} \quad (8)$$

$$I_{ET} = \sum_{n=0}^{5} B_n.I_n.2^n + I_{\min} \quad (9)$$

where, I_n (n = 0 to 5) are the constant coefficients of the estimated linear gain function, B_n are the digital bit value received from digital baseband and $I_{\min}$ is the DC current corresponding to minimum gain when all the digital control bits B_n are reset.

As shown in Fig. 5, by careful selection of the currents I_n (n = 0 to 5) using the aspect ratio (W/L) of NFET's (λ0 to λ5) and $I_{\min}$ using NFET ($\lambda_{\min}$), the current I_{ET} can be approximated closer to linear gain characteristics for the required range of the proposed DVGA. The DVGA gain and attenuation steps are obtained by selecting the parallel current sources of I_{ctrl} based on the transistor switches that are controlled using 6 bit digital information, B_n (n = 0 to 5).

The maximum gain for the CE variable gain stage is selected smaller in comparison to the CB input gain stage, and by digitally controlling the attenuation of this stage using transconductance g_{m3}, the whole DVGA gain range can be covered. The input transformed Miller capacitor, which is multiplied by the CE variable gain, determines the dominant pole, and the smaller gain of CE stage moves the dominant pole to higher frequency improving the DVGA bandwidth. The dominant pole is given by,

$$\omega_p = \frac{1}{C_{in} \cdot R_{in}} = \frac{1}{(C_\pi + C_\mu(1 + g_{m3}.R_{9,10})).(r_\pi)} \quad (10)$$

where, C_π and C_μ are the transistor lumped base-emitter and base-collector capacitances respectively.

C. Small signal analysis of output buffer stage

The output stage (last stage) is the emitter follower buffer to drive the signal power to the next transceiver block. This stage is a common collector (CC) amplifier with topological advantage of a smaller output impedance, which is resistive for a wide bandwidth. This improves the output return loss and it is not influenced by the DVGA gain variation as shown in (11). Larger device size (Q5/Q6) for this stage has better driveability, but the resulting larger parasitic capacitance will place a pole at low frequency limiting the bandwidth. Device size for this stage is carefully selected by taking this tradeoff into consideration.

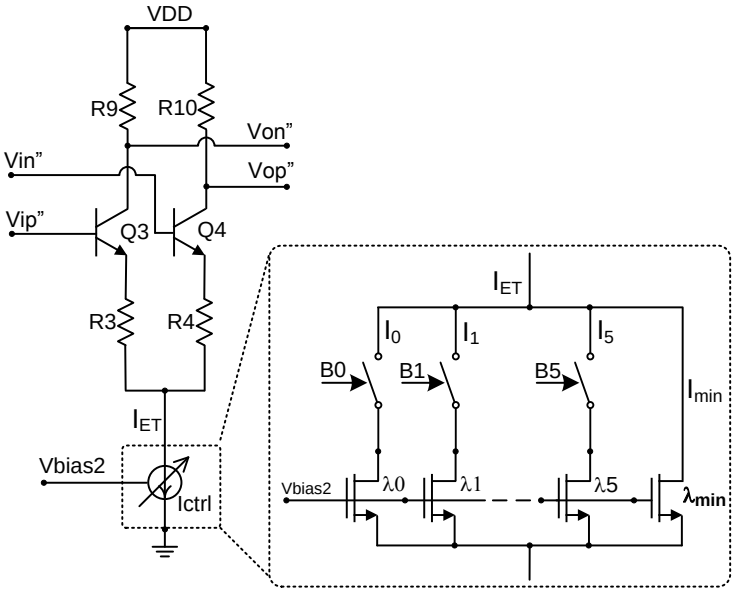

Fig. 5. Linear gain variation current distribution

Based on small signal model shown in Fig. 4,

$$R_{out} = \frac{v_{output}}{i_{output}} = \frac{r_\pi}{(\beta+1)} \| R_{5,6} = \frac{1}{g_{m5}} \| R_{5,6} \quad (11)$$

For the maximum power transfer, the best scenario is to achieve the conjugate matching between the DVGA stages. The wide bandwidth requirement of the proposed DVGA that starts from DC enforces the design to avoid using decoupling capacitors and the matching circuits between the cascaded stages. Although to minimize the power loss due to inter-stage mismatch and also to meet the special requirement of the wide bandwidth of the proposed design, the cascaded DVGA stages are chosen in such a way that the real parts of the internal impedances between the DVGA stages are larger and comparable than the reactive impedances.

D. Large signal analysis of the linearizer stage

Signal pre-distortion is a widely used linearization technique for improving the linearity of power amplifiers that compensates for the distortion and suppresses adjacent channel interference. This technique ensures that the large signal and small signal transistor transconductance are made equal. One such pre-distortion technique is the base emitter junction diode linearizer using HBT [16]. Due to the change in bias point of the amplifying HBT, proper design of base bias circuit is key to achieve high linearity for amplifiers [17].

Unlike the diode-connected linearizers described in [15]-[17] that are connected between a reference voltage and the base of amplifying HBT, the proposed linearizer is also a diode connected HBT shunted across the amplifying HBT to stabilize the base-emitter voltage bias point as shown in the Fig. 2 (b).

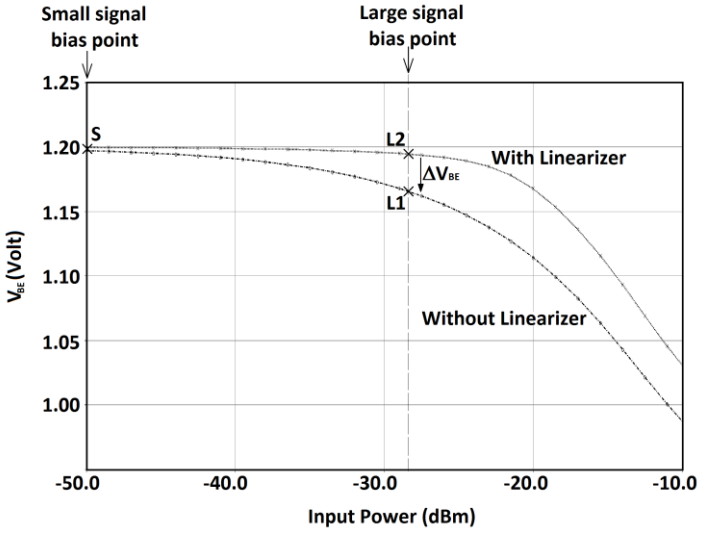

Fig. 6. Simulated HBT voltage bias point against input power with and without Linearizer

To explain the operating principle of the proposed linearizer, we first consider the case without linearizer and then determine the linearity improvement after introducing the linearizer. As the input RF signal power increases, the voltage across the base-emitter junction of Q3/Q4 increases and beyond a certain voltage the signal peak gets saturated. This results in an average DC voltage drop at the base of the HBT from bias point S to L1 as shown in Fig. 6. This reduced base voltage bias point ΔV_{BE} decreases the large signal transconductance and results in gain compression. To compensate for this compression and to equate the large signal transconductance with the small signal g_{m3}, the base bias point must be moved from L1 to L2 [16]. The same operation can be achieved by fixing the V_{BE} DC voltage of Q3/Q4 at the point S that is same as at L2 in Fig. 6.

The diode-connected transistors Q7/Q8 holds the base bias point (V_{BE}) of HBTs Q3/Q4 to a constant value (≈1.2 V) even for large input power levels as shown in Fig. 6 and improves the linearity of the DVGA. The DVGA linearity simulation shown in Fig. 7 demonstrates the advantage of the proposed linearizer to improve the circuit linearity. From Fig. 7, input P1dB is improved by about 12 dB (improved from A to B) and output P1dB is unaltered. The gain drop perceived in Fig. 7 is a consequence of introducing the proposed linearizer. The linearizer bypasses a portion of the HBT (Q3/Q4) base current that is determined by the size of the NMOS current mirror N2 as shown in Fig. 2 (b) and results in the gain drop as noticed in Fig. 7. The amount of DC current through the linearizer determines the contribution of the linearizer on the overall linearity by maintaining the fixed base voltage (≈1.2 V) and also on the DC power consumption of the proposed DVGA. By using the proposed linearizer, both the base voltage and the base current for the CE stage are fixed for large input power levels and thus the DVGA linearity is improved. The proposed linearizer utilizes the trade-off of improving the DVGA linearity with simple circuit topology and low DC power consumption over the gain reduction.

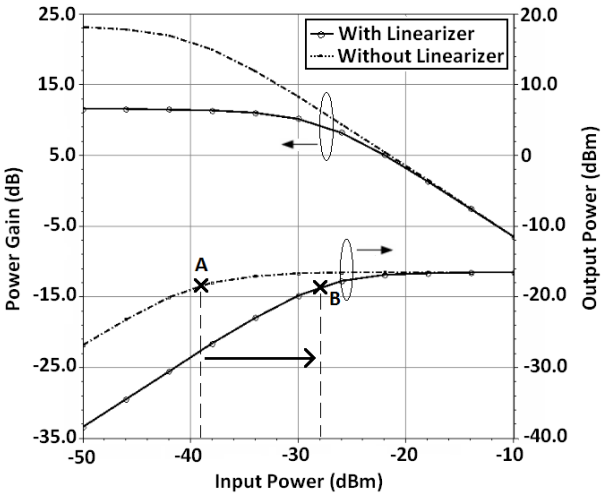

Fig. 7. Simulated maximum gain and Output power against input power with and without Linearizer

Direct coupling between the DVGA stages is necessary for propagation of the signals from DC. In the proposed DVGA, the linearizer is introduced at the nodes joining the CB and CE differential stages. This proposed linearizer improves the linearity of the DVGA without consuming additional dc power and significant die area. The proposed linearizer circuit has a simplified structure and does not require an additional biasing circuit, unlike the linearizers in [15]-[17]. The integrated diode linearizers described in [16] and [17] are based on InGaP / GaAs HBT transistor that has better input P1dB improvement of about 18 dB nevertheless these linearizers are operated at a higher supply voltage of 3.4 V that can provide enough headroom for stacking many transistors. Similarly the

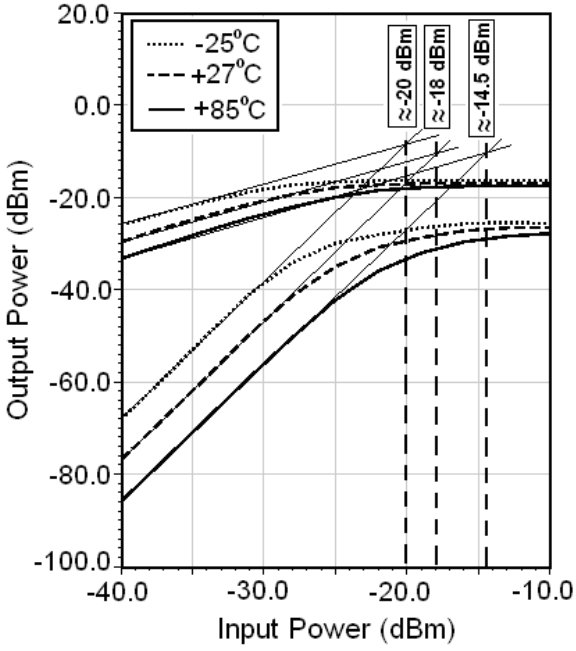

Fig. 8. Simulated P1dB and IP3 plots for maximum gain setting with varying temperature

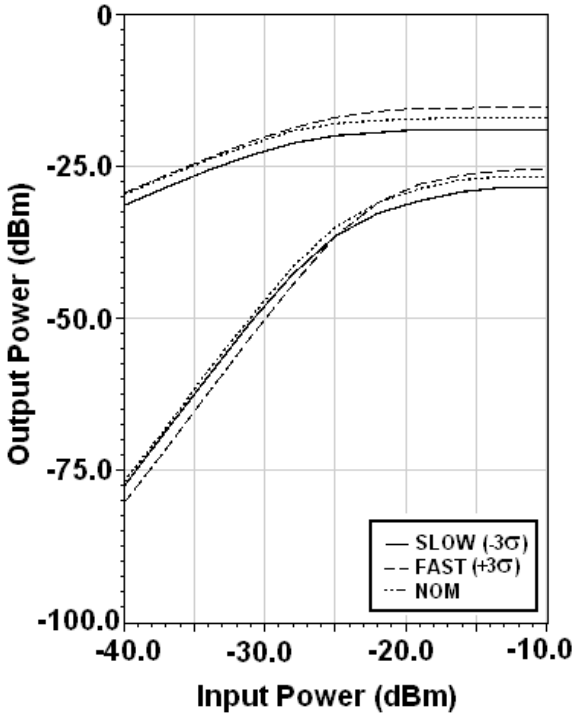

Fig. 9. Simulated P1dB and IP3 plots for maximum gain setting with process variations

linearizer in [15] describes a CMOS equivalent integrated diode linearizer design that has about 0.5 dB input P1dB improvement and is also operated at a higher supply voltage of 2.5 V. The linearizers in [15]-[17] are realized for single ended power amplifier designs and cannot be adapted in our design that requires differential drive. Contrasting the linearizers used in power amplifier designs [16], [17] that require a reference bias voltage that may be higher than the amplifier supply voltage, this proposed linearizer utilizes the DC level that is DC coupled between the CB and CE gain stages. These benefits of the proposed linearizer makes it an apt choice for this low power differential direct coupled DVGA.

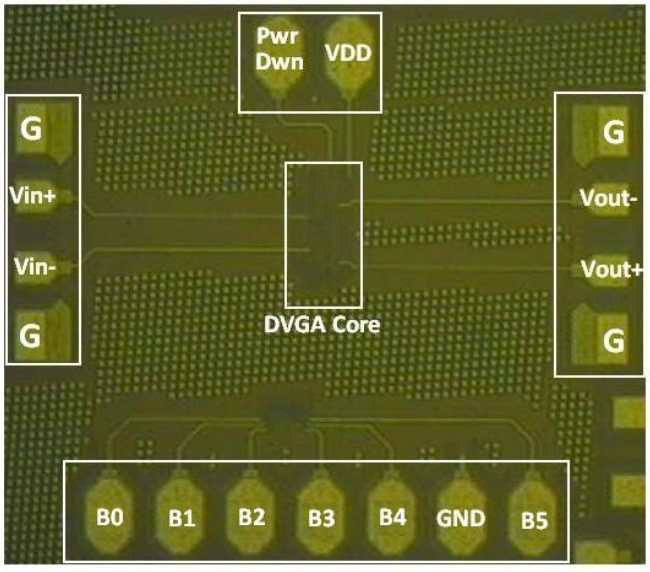

Fig. 10. Microphotograph of the proposed on-wafer DVGA circuit core with I/O pads (GSSG) and digital pads (Core Area: 170 um x 60 um)

Fig. 8 shows the simulation plot of output power along with the third harmonic component against the input power for maximum DVGA gain setting with varying temperature. The plot suggests that the IP3 and P1dB values have minimum change at the output while the temperature variation has an effect on the input IP3 and P1dB. The reason for this behavior can be explained by the V_{BE} temperature sensitivity of the diode-connected transistors in the proposed linearizer that affects the biasing point of the CE stage. The P1dB and IP3 simulation plot for maximum DVGA gain in Fig. 9 shows that the proposed linearizer is less sensitive to process variations. The variation of the DVGA's P1dB and IP3 are within ±1.5 dB from the nominal (NOM/TYP) value. The DVGA linearity characteristics with temperature and process variations is independent of the DVGA gain setting.

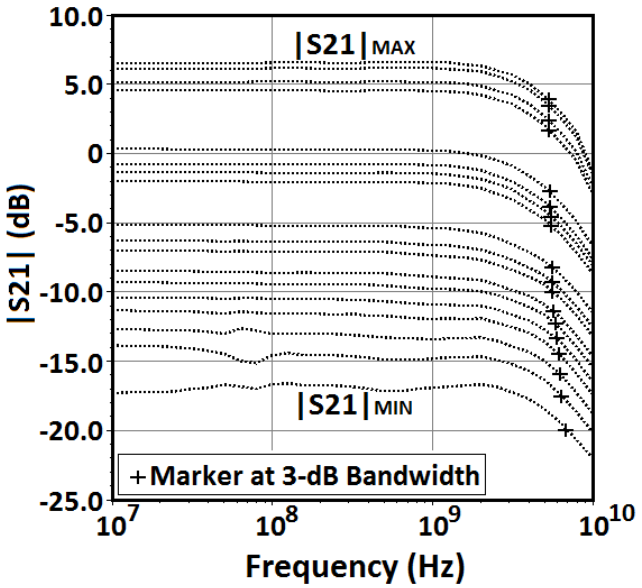

Fig. 11. Measured small signal gain steps of proposed DVGA

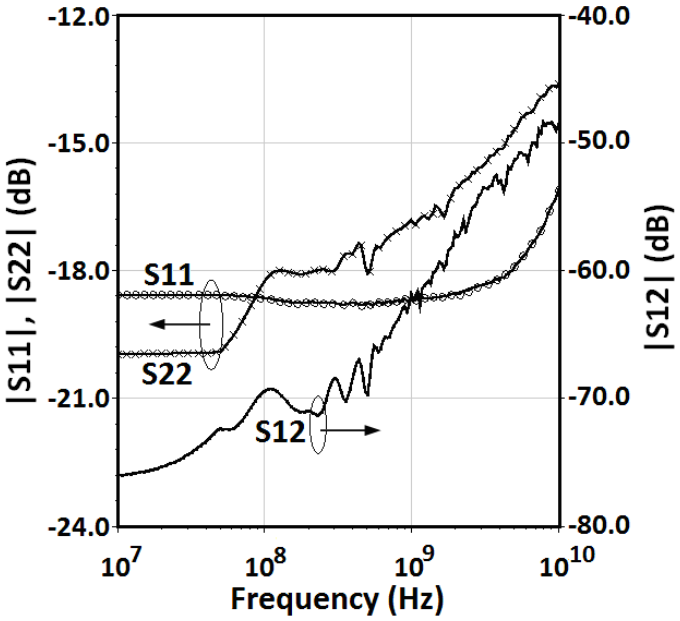

Fig. 12. Measured return loss and reverse isolation

III. Experimental Results

The proposed DVGA is implemented in 0.18 µm SiGe BiCMOS process from Tower Jazz Semiconductor and the design is verified on-wafer using Agilent E8364B PNA Network Analyzer and HP 8970B Noise Figure meter. The die microphotograph is shown in Fig. 10. The compact core area of 170 µm x 60 µm enables easy integration of DVGA transceiver System On Chip (SOC). The DVGA consumes DC current of 4.4 mA from a supply voltage of 1.8 V. During the power down mode all the NFET current sinks (N1, N2, I_{ctrl}, N3) are shut down and the circuit consumes current in the range of few nanoAmpere (nA) with outputs disabled.

The measurement setup comprises of two GSSG probes for input and output RF differential pads. Only 5 DC probes were available in test setup and two are used for VDD and Pwr_Dwn leaving only 3 probes for digital gain bits that could be set at a particular time. Hence the plots could not be taken for the entire gain variation steps and gain range was limited from B_n<5:0> = D5...D0 = "000000" for attenuation (minimum gain) to B_n<5:0> = D5...D0 = "111000" for maximum gain as shown in Fig. 11. The measured results are summarized in Table I and the small signal S-parameters are plotted in Fig. 11 and Fig. 12. From Fig. 11, the small signal gain has a good gain flatness for the measured gain steps covering a gain range from -16.5 dB to +6.5 dB and it is evident that the bandwidth increases with the decrease of the

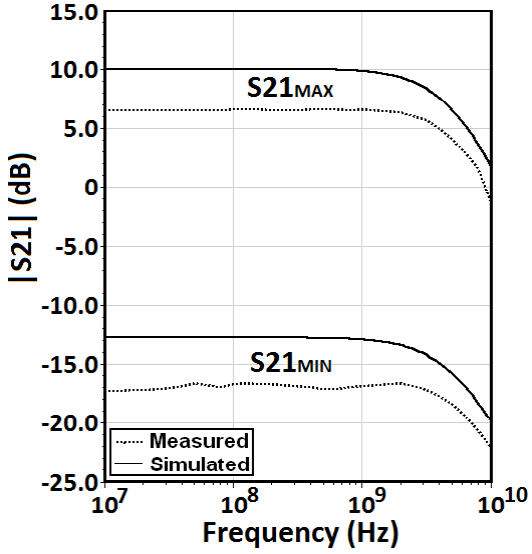

Fig. 13. Measurement and simulation of maximum and minimum gain

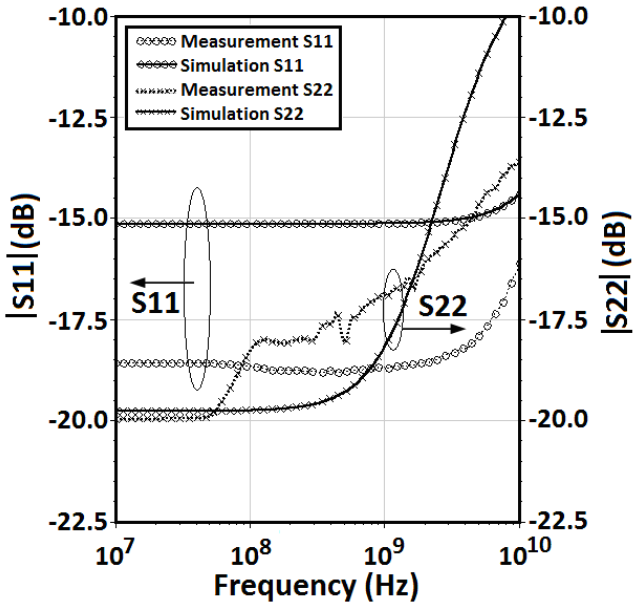

Fig. 14. Measurement and simulation of |S11| and |S22|

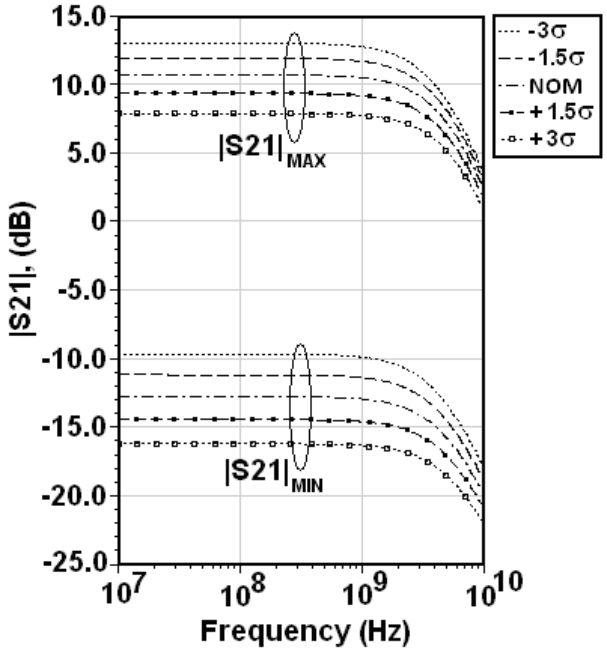

Fig. 15. Simulation of maximum and minimum gain against process variation of the polysilicon resistors (NOM: nominal resistance value and σ: process variation parameter of the polysilicon resistors)

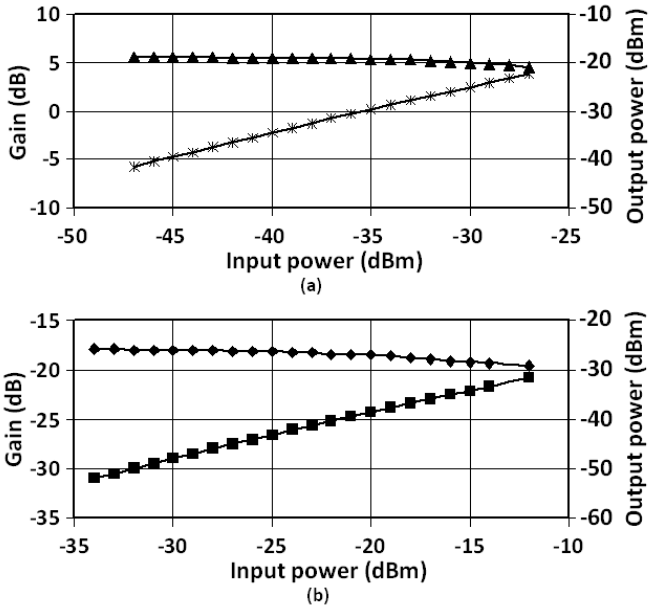

Fig. 16. Measured power output and Gain against input power for (a) Maximum Gain and (b) Minimum Gain bit

TABLE I
PERFORMANCE SUMMARY OF VARIABLE GAIN AMPLIFIERS

Reference	Technology	-3dB Bandwidth [Hz]	Gain Range [dB]	Input P1dB [dBm]	Noise Figure [dB]	Power [mW]	Active Area [mm x mm]	Gain Control
[4]	0.18 µm CMOS	0.4 M to 2 G	-16 to 34	-	-	40	0.7 ***	Analog
[5]	SiGe BiCMOS	DC to 3 G	-46 to 18.5	-14	7.5 to 55	117	1.51	Analog
[6]	90 nm CMOS	0.1 M to 2.2 G	-10 to 50	-13 to -55	17 to 30	2.5	0.014 ***	Analog
[7]	0.18 µm CMOS	32 M to 1.05 G	-52 to 43	-17 to -48	-	6.5	0.40	Analog
[8]	0.18 µm CMOS	0.9 G	-38.8 to 55.3	-10.8 to -59.1	6.8 **	20.5	0.195 ***	Analog
[9]	0.18 µm CMOS	0.38 G to 2.2 G	-13.5 to 13.5	-5 *	6.5 to 28.6	19.8	0.108 ***	Analog
[10]	0.18 µm CMOS	0.43 G to 2.33 G	-3.3 to 9.5	-9 *	6.3 to 7.9	16.2	0.409	Analog
[13]	0.18 µm CMOS	0.03 G to 1.4 G	-6.5 to 15.5	-	5.8 to 17.5	6.5	0.034	Digital
[14]	0.18 µm CMOS	0.048 G to 0.86 G	-34 to 16	+11 to -15	2.4 to 24.5	30.6	0.25	Digital
[20]	0.13 µm CMOS	0.12 G	-10 to 36	-	-	16	0.8	Digital
[21]	90 nm CMOS	0.29 G	28 to 46	-6	-	14	0.03 ***	Digital
[22]	0.13 µm CMOS	3 G to 9.4 G	12	-6	1.8 to 4.7	30	0.83	Fixed
[23]	0.13 µm CMOS	0.8 G to 9 G	0 to 2.5	+1.0	9.5	40	1.5	Digital
[24]	0.13 µm SiGe BiCMOS	0. 2 M to 7.5 G	-10 to 30	-	-	72	1.0	Analog
[25]	0.18 µm SiGe BiCMOS	0.2 G to 2.5 G	50	-	-	102	1.8	Analog
This work	**0.18 µm SiGe BiCMOS**	**DC to 5.6 G**	**-16.5 to +6.5**	**-17 to -27**	**16.5 to 27.1**	**7.9**	**0.01 *** **	**Digital**

* minimum measured P1dB ** simulation noise figure
*** Core die area (excluding I/O pads)

DVGA gain as discussed in (10). From the measurement plots in Fig. 12, both the input return loss (S11) and the output return loss (S22) are greater than 15 dB over the complete operational frequency range independent of the DVGA gain setting. Fig. 13 and Fig. 14 shows the comparison of simulation versus measured S-parameter gain (S21) and return losses (S11 and S22) respectively. We observe that the measured gain is dropped by 3.5 dB from the simulation gain while the bandwidth is increased by 1 GHz. The main contribution for this difference is ascertained to the process variation of the polysilicon resistors that are used as the load for the proposed DVGA amplifier stages. Fig. 15 shows the corner simulation plot for the DVGA gain variation against the statistical process parameter variation of the polysilicon resistors. The plot suggests that the consequence of reduction in the resistance value causes the gain to drop and bandwidth to increase, which is the behavior observed in the measurement results shown in Fig. 13. In addition, the interconnect losses from the differential traces connected from the core DVGA to GSSG measurement pads are partly responsible for the gain drop. The linearity improvement is noticeable in the measurement plot shown in Fig. 16 for maximum and minimum gain setting. The measured results are summarized and compared with high performance VGAs in Table I. The proposed DVGA has widest bandwidth of 5.6 GHz, finer gain control range from -16.5 to +6.5 dB using 6 bits, consuming less power of 7.9 mW for a fully differential architecture and a compact core area of 0.17 mm x 0.06 mm. The newly introduced linearizer has improved the input P1dB maintaining output P1dB in the range of -5 dBm to -2 dBm.

The measured noise figure is plotted for different DVGA gain settings against frequency as shown in Fig. 17. The plot in Fig. 18 is obtained with the measured gain and the noise figure at 3 GHz for different DVGA gain setting. The digital gain

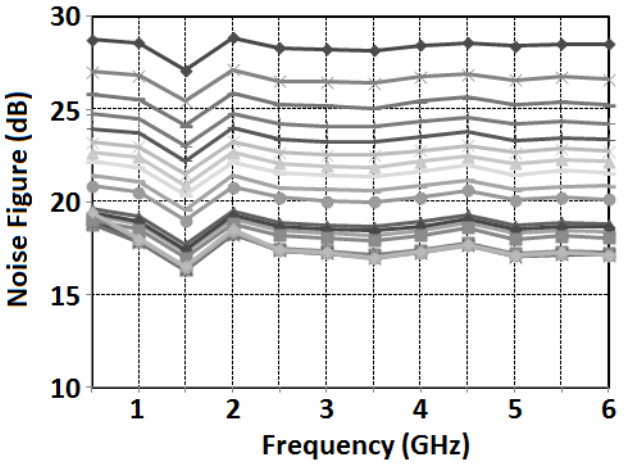

Fig. 17. Measured noise figure for various DVGA gain steps

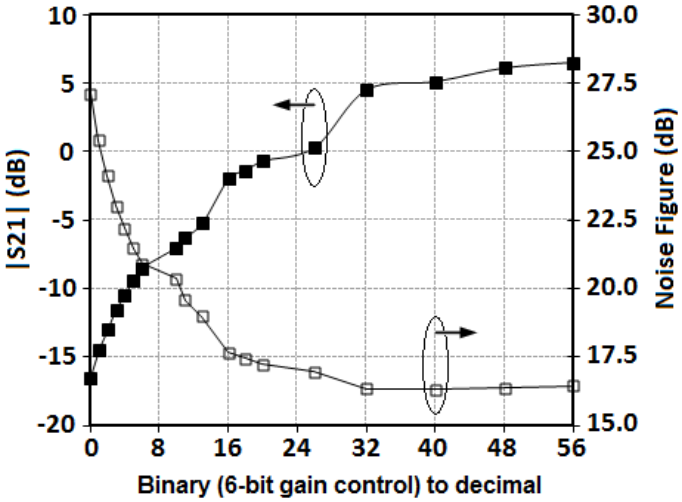

Fig. 18. Measured gain and noise figure at 3 GHz for various digital gain control

control word depicted along the x-axis in the Fig. 18 indicates the decimal value representation of the 6-bit binary word with B5 as the MSB (most significant bit) and B0 as the LSB (least significant bit).

The plot in Fig. 18 indicates that the noise figure for the amplifier gain setting (gain ≥ 0 dB) is almost constant mainly because the input is a fixed gain amplifier CB stage. The noise figure becomes larger as the DVGA gain becomes smaller and operates as an attenuator (gain < 0 dB). The DVGA noise figure is given by (12),

$$NF_{DVGA} = NF_1 + \frac{NF_2}{A_{V1}} + \frac{NF_3}{A_{V1} \cdot A_{V2}} \quad (12)$$

where, NF_i and A_{Vi} (i = 1, 2 and 3) are the noise figure and the voltage gain of the cascaded CB, CE and CC amplifier stages of the proposed DVGA. In our transceiver system, since the stages before the DVGA of the receiver chain have enough gain and low noise figure, according to the Frii's formula of the cascaded stages, the contribution of the proposed DVGA's noise figure is not significant on the overall receiver's noise figure.

IV. Conclusion

A compact digitally controlled VGA using 0.18 μm SiGe BiCMOS technology designed for a wide 3-dB bandwidth of 5.6 GHz, a large gain range from -16.5 to +6.5 dB and consuming only 7.9 mW is presented. The diode linearizer stage improves the circuit linearity without increasing the circuit's DC power consumption and die area. Excellent small signal performance with flat gain steps over the entire bandwidth and return loss at both input and output reference planes greater than 15 dB is achieved. The die area occupied by the core DVGA is only 170 μm x 60 μm.

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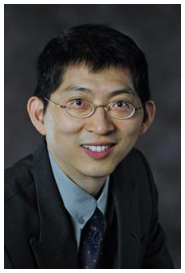

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