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A +70 dBm IIP3 Electrical-Balance Duplexer for Highly-Integrated Tunable Front-Ends

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***Abstract*— An electrical-balance duplexer achieving state-of-the-art linearity and insertion loss performance is presented, enabled by partially depleted RF silicon-on-insulator (SOI) CMOS technology. A single-ended configuration avoids the common-mode isolation problem suffered by topologies with a differential low-noise amplifier (LNA). Highly-linear switched capacitors allow for impedance balancing to antennas with <1.5:1 voltage standing wave ratio (VSWR) from 1.9 to 2.2 GHz. +70 dBm input-referred 3rd-order intercept point (IIP_3) is achieved under high transmitter (TX) power (+30.5 dBm max.). TX insertion loss is <3.7 dB and receiver insertion loss is <3.9 dB.**

***Index Terms*—Electrical-balance, duplexer, frequency-division duplexing, hybrid transformer, silicon-on-insulator, CMOS integrated circuits, linearity, tunable capacitors.**

I. Introduction

Next-generation front-end modules (FEM) for wireless transceivers in compact, hand-held devices require an ever-increasing number of bands to be supported [1]. Although the transmitter (TX) and receiver (RX) portions of the communications chain become more digital-intensive and reconfigurable on-the-go [2],[3],[4], the key frequency-division duplexing (FDD) building block of the FEM, the duplexer, is still based on fixed-frequency surface-acoustic wave (SAW) filters. Therefore, the FEM architecture needs an overhaul to enable scaling and frequency flexibility.

One recent innovation in this regard is the electrical-balance (EB) duplexer. The EB duplexer concept is based on hybrid transformers providing signal cancellation through the electrical balancing of two impedances – the antenna and an on-chip dummy load called the balance network (Z_{BAL}). This concept was initially used to enable point-to-point isolation between telephony nodes [5]. It recently re-gained interest as a technique to provide isolation directly at RF between the TX and RX, which enables frequency-flexible duplexer operation and replaces the fixed-frequency SAW counterparts [5]-[16].

While the potential payoff is tantalizing, several challenges must still be solved before EB duplexers can become commercially viable. Specifically, the duplexer must provide high isolation and high linearity in both the TX and RX bands across wide signal bandwidth (BW), with low insertion loss (IL) in the TX and RX paths, all in the presence of an antenna whose impedance constantly varies due to user interactions.

In particular, linearity requirements for EB duplexers are as stringent as their non-tunable counterparts, due to the fact that the large TX signal may cause inter- and cross-modulation distortion when external unwanted interference is absorbed by the antenna. Since the tuned passives needed in the EB duplexer rely on switches for discrete-step impedance tuning, limited linearity can be achieved. Recent prototypes [7],[9],[14] have been unable to achieve the necessary levels of linearity in bulk CMOS technology. RF silicon-on-insulator (SOI) CMOS technology is an economically attractive technology option which has shown particularly apt for implementation of highly-linear RF multi-throw switch devices, since the floating body devices allow for much better switch stacking than bulk CMOS [17].

This work extends upon [16], where an electrical-balance duplexer implementation in partially depleted 0.18 µm RF SOI CMOS addresses two key challenges in EB duplexer design: linearity and insertion loss. The prototype supports up to +30.5 dBm at its TX input without degradation effects. Over +70 dBm input-referred 3rd-order intercept point (IIP3) is measured, which means it withstands the most critical standard-defined jammers without generating too much distortion in the RX band. Less than 3.7 and 3.9 dB IL is measured, for the TX- and RX-path respectively. The duplexer has 4-dimensional Z_{BAL} tuning and supports <1.5:1 voltage standing wave ratio (VSWR) for 1.9 to 2.2 GHz.

Compared to [16], this work contributes the following. Critical large-signal measurement results for EB duplexers, such as TX-RX isolation and chip temperature versus TX power, as well as extensive distortion tests for LTE bands are provided for the first time in this paper (Section V). In addition, Section II provides extra context through an example transceiver architecture and considers technology trade-offs. Section III adds a discussion on linearity requirements and derives performance limits for EB duplexers. Section IV provides details on designing highly linear EB duplexers. Finally, the Appendix provides details on duplexer distortion tests, including a method for IIP3 tests up to +85 dBm.

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II. Combining RF Silicon-on-Insulator and Bulk CMOS for a Frequency-Flexible Transceiver Architecture

Present-day cellular handset FEMs still use an extensive number of SAW filters and other non-bulk CMOS components, such as power amplifiers (PA) – commonly implemented in Gallium-Arsenide (GaAs) or Silicon-Germanium (SiGe) – and usually RF SOI CMOS multi-throw switches. Integration of the FEM components to minimize the system's total on-board area is a major point of attention during handset design. Indeed, some components in today's FEM may likely still shrink, to allow either reduced total cost or added functionality for the same footprint. For example, more band combinations for intra- and inter-band carrier aggregation could then be added. Clearly, even existing FEMs are a multi-technology solution, where the best technology is selected for each building block in order to achieve optimal performance in the overall system.

However, a tunable solution for the duplexer would significantly simplify the current FEM architecture. In fact, if the technology that would enable such a tunable duplexer in a cost-effective manner could be integrated with other FEM components, the reduction in footprint and cost would be substantial. Beyond sufficiently low loss and high linearity as key specifications, the key FEM functionalities for any supported FDD band are:

- prevent the TX from leaking to the RX through isolation,
- reduce spurious TX emissions at harmonic frequencies,
- filter unwanted external interference in the RX-path,
- match the antenna impedance to improve TX efficiency.

Fig. 1 shows an (example) tunable FEM/TRX architecture based on a frequency-flexible EB duplexer. The architecture uses just two technologies for simplification, namely RF SOI CMOS for the FEM components including low-noise amplifier (LNA), antenna tuner, EB duplexer, TX balun and PA, and bulk CMOS (e.g. 28nm) to implement an N-path-based software-defined receiver (SDR) and digital-intensive TX, both co-integrated with the digital baseband (BB).

The antenna tuner improves TX efficiency and simplifies the duplexer Z_{BAL} tuning requirements by reducing variability of the antenna impedance [18]. Even though GaAs or SiGe alternatives are still more attractive at this time, it is not unrealistic to assume that PAs in SOI CMOS will become competitive, as PA implementations in RF SOI have recently gained interest and improvements in performance have been reported [19].

On the RX-side, bringing the LNA on-chip with the duplexer in SOI CMOS offers cascaded noise figure (NF) benefits through a high-Z interconnect [5],[9]. A co-integrated LNA can also provide proper matching and compensates losses when driving the signal onto the transceiver CMOS die. Also, it can provide a low-loss high-Z interface when flip-chip and other packaging technologies are used, offering benefits to both the RF designer in terms of design freedom and the handset architect in terms of the available integration choices.

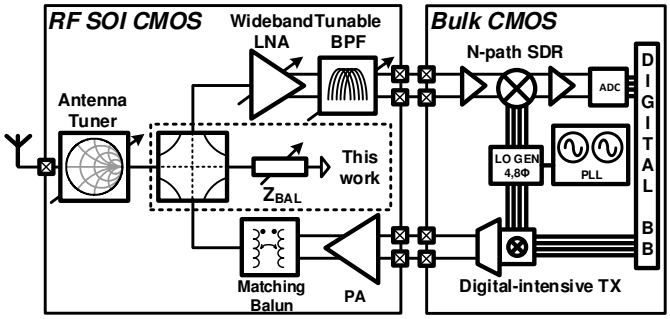

Fig. 1. Highly-integrated re-configurable transceiver front-end architecture.

An important limitation of the EB duplexer is that it does not provide filtering, in the TX- or the RX path. Therefore, even with very linear LNA implementations in SOI CMOS [20],[21], some kind of pass-band filtering could still be required within the FEM. Tunable RF band-pass filters could be implemented on-chip by N-path techniques [22], or off-chip with tuned SAW resonators [23]. While tuned SAWs have higher loss than fixed-frequency SAW filters, their specs might be attractive for a tunable FEM solution, when the EB duplexer takes care of TX-RX isolation. Tuned capacitors for those resonators can then be implemented in conjunction with the other circuitry in the SOI CMOS die.

In bulk CMOS, a high f_T implies high-speed switching is available at low power, which enables low-power buffers required to drive the N-path filters at N times the LO frequency. Compared to 4-path filters, higher-order (e.g. N=8) N-path mixers offer extra harmonic rejection (HR) and improve the overall RX chain noise performance. This drastically reduces the HR requirements for the FEM compared to the case where N=4 or the case where classical active mixers are used. Additionally, the generation of multi-phase signals using multiple integrated oscillators and phase-locked loops can be done efficiently and robustly in bulk CMOS [24], while bulk CMOS ADCs benefit significantly from scaling, and keep breaking their previous performance records [25],[26]. On the TX-side, having a digital-intensive TX [4],[27] can help to increase scalability towards future generations, and with improved architectures they also provide out-of-band noise and linearity performance comparable to fully analog implementations. In fact, when such a bulk CMOS TX operates with such performance at high output power [28],[29], the PA requirements are relaxed as it needs to provide less gain. In addition, the impedance interface between the TX and PA can be designed for better overall efficiency, just like on the RX-side.

In conclusion, trading off the specifications by designing each block in the technology that provides the best overall performance may change radio architectures significantly to enable a truly software-defined radio - frequency-flexible from antenna to baseband. The key block which is needed to enable that, however, is the tunable duplexer at the heart of the FEM. In this work, the focus is thus on the duplexer itself, starting with an analysis of linearity requirements for such a tunable electrical-balance duplexer.

III. Required Linearity to Support 3GPP Jammers

The concept of EB duplexers is thus very attractive for an integrated FEM, but due to the high-power PA signal, distortion performance in the presence of interferers is specifically critical. When an external out-of- or in-band jammer (Fig. 2 and Fig. 3) and a large-swing TX signal transfer to the balance network, nonlinear distortion is generated due to the finite linearity of the switched passives.

Two jammer cases are critical for duplexer operation:
(1) the full-duplex-spaced (FDS) out-of-band jammer (Fig. 2),
(2) and the co-channel (CC) in-band jammer (Fig. 3).

In the CC-jammer case, problematic cross-modulation distortion (XMD) products are generated exactly at the RX channel frequency. In this case, the worst-case 3GPP-specified jammer level is -43 dBm at the antenna. This is also referred to as the *triple-beat test* [30].

In the FDS-jammer case, 3rd-order intermodulation distortion (IMD) generated in the balance network transfers directly to the RX port with little attenuation. The worst-case FDS jammer level is specified at -15 dBm at the antenna in 3GPP. Due to the difference of 28 dB in jammer level, the FDS jammer case is the most stringent, as will now be shown.

A linear approximation of the hybrid transformer transfer functions can be defined using the S-parameter (SP) matrix:

$$\begin{bmatrix} b_{ANT} \\ b_{TX} \\ b_{RX} \\ b_{BAL} \end{bmatrix} = \begin{bmatrix} S_{AA} & S_{AT} & S_{AR} & S_{AB} \\ S_{TA} & S_{TT} & S_{TR} & S_{TB} \\ S_{RA} & S_{RT} & S_{RR} & S_{RB} \\ S_{BA} & S_{BT} & S_{BR} & S_{BB} \end{bmatrix} \begin{bmatrix} a_{ANT} \\ a_{TX} \\ a_{RX} \\ a_{BAL} \end{bmatrix} \quad (1)$$

where A, T, R, B imply respectively the antenna, TX, RX and balance network ports, all with the nominal port impedances [5], i.e. Z_A=Z_B=50 Ω, Z_T=25 Ω and Z_R=100 Ω.

Using these transfer parameters, the distortion power resulting from a finite $IIP3_{BAL}$ can be derived. $IIP3_{BAL}$ can be defined from the 2-tone power delivered to Z_{BAL} from a 50 Ω source and the IM3 power generated by Z_{BAL} that is absorbed by the source. In the following equations, the distortion power is referred to the RX port to evaluate the impact on RX sensitivity.

For the FDS-jammer case, the IM3 distortion product $P_{FDS,IM3}$ present at the RX port due to nonlinearity in the balance network is:

$$P_{FDS,IM3} = 2P_{TX} + P_J - 2IIP3_{BAL} + 2S_{BT} + S_{BA} + S_{RB} \quad (2)$$

where P_{TX} is the (single-tone equivalent) TX power (+27 dBm) and P_J is the (narrow-band) jammer power (-15 dBm).

Similarly, for the CC-jammer case, the cross-modulation distortion product $P_{CC,XMD}$ is:

$$P_{CC,XMD} = 2P_{TX} + P_J - 2IIP3_{BAL} + 2S_{BT} + S_{BA} + S_{RB} \quad (3)$$

here, P_{TX} is the average total TX power of a 2-tone (+27 dBm), and P_J is the jammer power (-43 dBm).

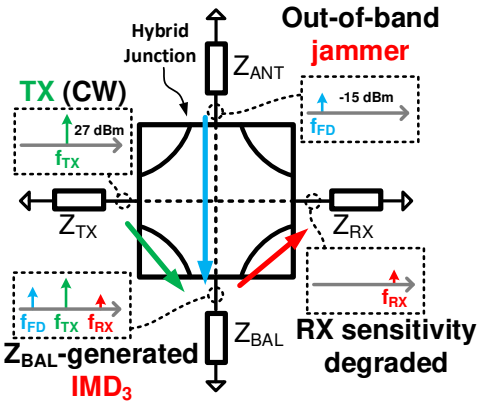

Fig. 2. External *full-duplex-spaced jammer* linearity requirements. The 4-port symbol in the center represents the hybrid transformer.

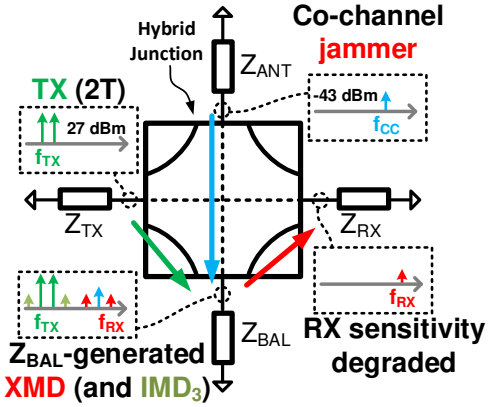

Fig. 3. External *co-channel jammer* linearity requirements.

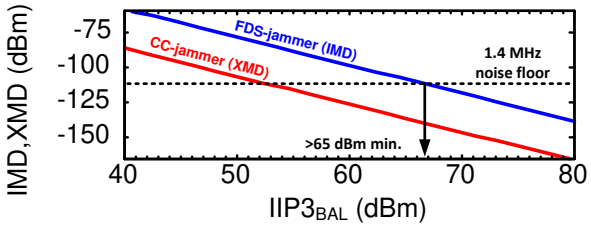

Fig. 4. IMD ($P_{FDS,IM3}$) and XMD ($P_{CC,XMD}$) for 3GPP-defined jammers.

Finally, this can be converted to a more meaningful IIP3 requirement for the TX-path, which is readily observed using the TX-port as an input and the antenna port as an output:

$$IIP3_{TX} = IIP3_{BAL} - \frac{3}{2}S_{BT} + \frac{1}{2}S_{AT} - \frac{1}{2}S_{BA} \quad (4)$$

Assuming a symmetric, non-skewed, lossless hybrid transformer (i.e. S_{AT}=S_{RA}=S_{TA}=S_{AR}=3 dB) with limited S_{BA} due to parasitic coupling (e.g. 10 dB), Fig. 4 shows the calculated IMD and XMD for a given $IIP3_{BAL}$. Clearly, very high Z_{BAL} linearity is required, in order not to degrade the RX noise floor, e.g. at least +65 dBm. Note that this analysis applies to Z_{BAL} only, but similarly strict specifications can be derived for distortion generated on the antenna side, e.g. the antenna tuner. Finally, since the distortion is generated within the duplexer, post-duplexer RX-path filtering does not help.

IV. Highly-Linear EB Duplexer Design

In [9], the common-mode isolation achievable by a hybrid transformer with a differential LNA is investigated. In that case, both common- and differential-mode transfer paths from TX to RX exist. The balance network can provide a differential balance condition, but is unable to guarantee good common-mode isolation due to capacitive coupling between the transformer coils. As a result, a common-mode TX leakage component will be present at the differential input of the LNA and can significantly reduce the RX sensitivity through either compression or intermodulation generated in the LNA due to external jammers.

The common-mode isolation can be improved by shorting the common-mode tap of that winding to ground, but in most cases this technique will still not provide satisfactory common-mode isolation [7],[14]. Therefore, a fully differential hybrid transformer structure has been proposed [8],[9],[11] to achieve both common- and differential-mode isolation, which comes at the price of increased size and loss.

This work proposes a single-ended hybrid transformer topology (Fig. 5) that avoids having both a common- and differential-mode leakage path. Path 1 indicates the main leakage path through the antenna side. The balance network 'copies' the TX signal, and the hybrid transformer inverts that copy by 180° in the current domain (indicated as path 2). At the RX node, these two paths then cancel out through destructive interference. Therefore, the balance network enables electrical-balance and provides complete TX-RX suppression.

Fig. 5 also illustrates the capacitive coupling present between the windings in the hybrid transformer. When one end of the secondary winding is shorted to ground, the two paths require impedance compensation to maintain electrical-balance such that both paths can cancel out. Similarly, when the hybrid transformer is skewed, i.e. its TX input-tap is placed off-center on the winding, an increased real part for Z_{BAL} is required similar to prior hybrid transformer topologies [7],[14] to maintain impedance balance, at the cost of a small NF penalty as explained in [9].

The final hybrid transformer layout is shown in Fig. 6. The primary winding is skewed off-center towards the antenna for improved TX loss. Table I shows its simulated performance.

Fig. 7 shows the balance network topology, which consists of four equal-valued 8-bit tunable capacitor banks and two integrated inductors with a dc-inductance of 1.8 nH and a peak Q of 20. The network is terminated with a fixed 50 Ω polysilicon slab resistor, sized at 345 by 53 µm. This sizing avoids that electro-migration problems occur even when the network absorbs +27 dBm of signal power. The resistor is chosen to be a non-tunable component, as orthogonal tunability is possible with capacitors only, while tuned resistors were found to be the linearity bottleneck [14]. When all four capacitors are set to their middle code, the network provides an impedance balance with a 50 Ω antenna-side impedance at 2 GHz, which was used as a center frequency for this design. Some fixed capacitance is also added in parallel with C1 and C2, which centers the tuning range and

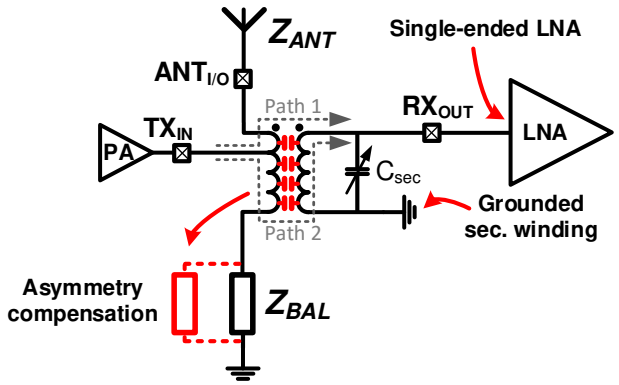

Fig. 5. Single-ended hybrid transformer with compensation for capacitive asymmetry and center-tap skewing offset (from [16]).

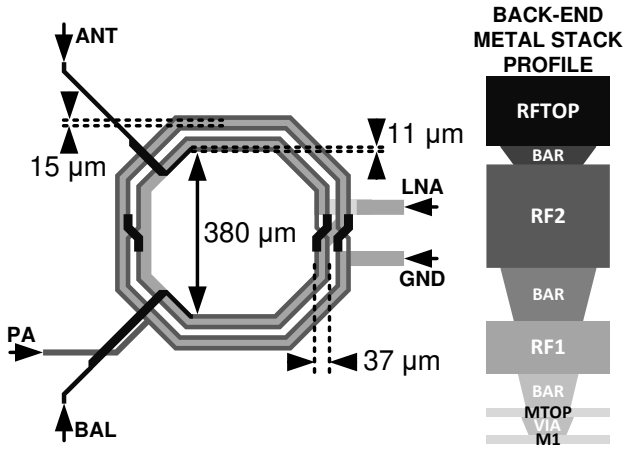

Fig. 6. Hybrid transformer layout and back-end metal stack (from [16]).

TABLE I. Hybrid Transformer Simulated Specifications.

Lprim @ dc	11.7 nH
Lsec @ dc	3.1 nH
Peak Q (Lprim)	16.8
Peak Q (Lsec)	13.5
k @ dc	0.84
Self-resonance frequency	2.3 GHz

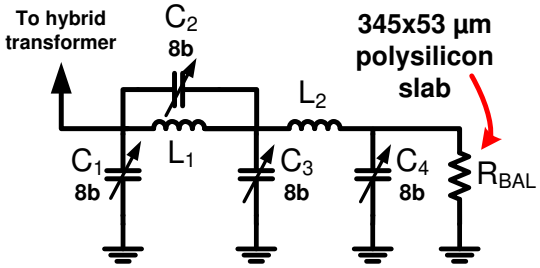

Fig. 7. Four-dimensional balance network topology (from [16]).

compensates for skewing and capacitive asymmetry. 8b resolution allows for fine-tuning, while sufficient capacitance value overlap versus code (1.8x radix) guarantees impedance coverage without any gaps. To sustain the voltage swing caused by large TX power, switched capacitors in this design use two unit capacitors and a NMOS transistor stack (Fig. 8). Dual unit capacitances avoid the need of negative gate bias.

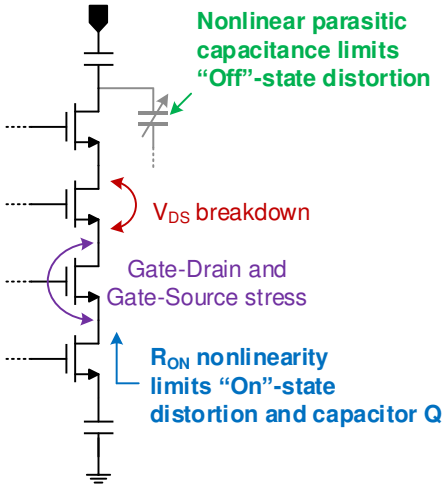

Fig. 8. Design considerations for switched-capacitor design in SOI technology.

Instead, Fig. 9 shows the bias voltages used in the "On" and "Off" states, which are all ≥0 V. The sizing of the stacked switch devices in one of the RF switched capacitor unit cells is constrained by two opposing sources of non-linearity. In the "Off" state, non-linearity is generated by the voltage-dependent parasitic (junction) capacitances present in the switch layout. When the transistor width increases, these parasitics increase, and linearity degrades. So, "Off" state operation prefers small-sized switches. In the "On" state, the non-linearity of the V_{DS} / I_{DS} transfer characteristic (R_{ON}) of the switches generates distortion. R_{ON} decreases for increased width. So, the "On" state prefers large switches. Thus, some specific width exists for which the distortion trade-off equalizes for the "On" and "Off" states. Since the inductors are the main Q bottleneck in this design, high capacitor Q is not of prime importance. Therefore, the capacitor cells were optimized according to the transistor sizing that leads to equivalent distortion in both the "On" and "Off" states. Design and analysis was aided by PSP transistor models, which allows for accurate simulations of nonlinearity in the case where V_{DS} is often close to 0.

Fig. 9 shows the switched capacitor unit cell, which uses two base unit capacitances C_U and a switch consisting of four stacked SOI NMOS devices, sufficient to avoid exceeding the drain-source breakdown voltage for +27 dBm signal swings. Through the proposed bias voltages, switch resistance is minimized in the "On" state and linearity is maximized in the "Off" state. R_G, R_B and R_{SD} are dc-biasing resistors.

Ignoring drain- and source-to-substrate parasitics and assuming linearly scaled switch widths for a SOI CMOS switch stack with N stacked transistors, R_{ON}/C_{OFF} will be independent of N [31]. In reality however, the increasing parasitic capacitances from drain/source to substrate mean that R_{ON}/C_{OFF} degrades when N and the width per switch increases. These parasitics also cause an uneven distribution of voltage swing across each switch, so that the top switch experiences the highest voltage stress [31]-[33]. Therefore, coupling capacitors (C_C in Fig. 9) are placed in parallel with each of the switches to improve the equalization of ac voltages and better

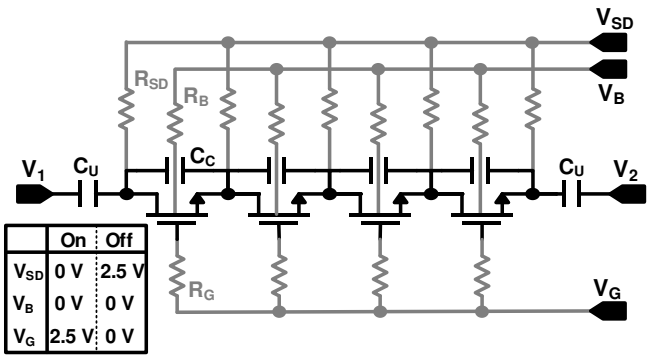

Fig. 9. Switched capacitor unit cell with four stacked switches (from [16]).

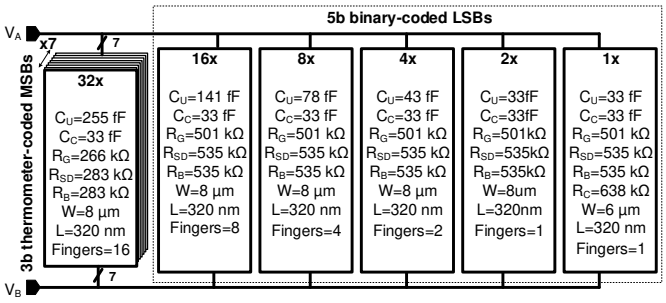

Fig. 10. Sizing parameters for the capacitor bank, which is divided between thermometer-coded MSB cells and binary-coded LSB cells.

utilize each switch in the stack. This explicit coupling adds to the intrinsic coupling, and causes the voltage swing in the "Off" state to be more evenly distributed across all switches, which equalizes gate-drain/gate-source voltage stress (Fig. 8). The downside of this extra equalization is a reduction in the ratio of C_{ON}/C_{OFF}. However, this is compensated by resizing the inductors in Fig. 7. This maximizes the overall impedance coverage of Z_{BAL} while the capacitors also withstand the voltage stress at high TX power.

Minimum-sized C_C is placed on top of the switch transistors in layout, such that the majority of C_C's parasitics will couple into the gate, drain, and source nodes of the underlying transistor, which is what we seek to increase the coupling of. In effect, this leads to zero unwanted parasitics due to C_C.

The values of all the components in the capacitor bank are shown in Fig. 10. The same 8-bit capacitor bank was used for all four of the tunable capacitances implemented in the balance network (C_1, C_2, C_3 and C_4 in Fig. 7). Since two unit capacitances are used in each cell, the same topology may be used both for single-ended and differential connected capacitors. All sub-cells in Fig. 10 are implemented using the circuit of Fig. 9, except for the LSB cell (1x) which stacks two minimum-sized metal-insulator-metal (MIM) capacitors in order to create a unit capacitance that is half of the minimum MIM capacitance allowed by the technology's design rules. The three most significant bits are implemented as unary-weighted elements, and the 5 least significant bits are implemented as binary-weighted elements. Each capacitor bank has a simulated C_{ON}/C_{OFF} of 1.25/0.3 pF/pF and a Q≥19 across settings for 1.8 to 2.2 GHz, similar to the Q of $L_{1,2}$. Finally, the overall tuning range is limited by the 50 Ω R_{BAL}.

V. Measurement Results

The single-ended EB duplexer prototype was implemented in the GlobalFoundries 0.18 µm RF SOI CMOS process. Fig. 11 shows the chip photo, indicating the hybrid transformer (T_M), the switched capacitors (C_1-C_4, C_{sec}), as well as the fixed inductors (L_1 and L_2) and the fixed resistor R_{BAL}. The area occupied by the duplexer measures 1.75 mm^2. For testing purposes, the chip can switch to external bias voltages for all gate, drain-source and body nodes. Therefore, decoupling capacitors were placed on-chip as well. For the results presented in this paper, however, this is never used. Instead, all biasing is routed to the switches directly from a single 2.5 V supply, which also powers the on-chip shift-register used to program the value of all capacitors.

Fig. 12 shows the antenna-referred impedance ranges for a evenly spaced full-range 4x4x4x4 coarse code grid of swept digital codes for the switched capacitors in the balance network. For this measurement, a Maury impedance tuner was used between the antenna port and a 50 Ω termination. The impedance was measured by iteratively selecting a tuning code on the coarse grid and tuning the impedance tuner until >50 dB isolation was found for each code. The impedance for which this occurred, for all 256 swept values, is plotted in Fig. 12. Due to the coarse nature of the sweep, some 'gaps' occur in the impedance domain for higher frequencies. However, when taking LSB steps, no gaps occur between tuning codes.

The single-frequency tuning range this duplexer can cover is 1.5:1 VSWR for any frequency from 1.9 to 2.2 GHz (indicated by the dotted circles in Fig. 12). This implies that an antenna tuner would likely be required to reduce the antenna variation, since antennas are usually specified to <3:1 VSWR.

In order to demonstrate the degrees of freedom that this duplexer design offers, its tuning behavior was observed when connecting a 50 Ω SMD termination to the antenna port through about 10 cm of transmission line, which effectively causes a capacitive change to the load impedance. Then, TX-RX isolation was measured (Fig. 13). As can be seen, multiple isolation peaks are present due to Z_{BAL} aligning with the antenna impedance (Z_{ANT}) across frequency. The peaks can be placed closer together (light shaded line) or further apart (darker lines) to provide either a deep isolation peak or increased isolation BW.

Note that the actual BW measured here is not representative of the isolation BW when a real antenna is connected, because the isolation BW depends directly on the impedance of the antenna across its environmental variations [14]. While extensive tests to verify BW in various environmental conditions were not done, practical tests using various types of off-the-shelf antennas in a laboratory environment indicate that it is not the balance network, but instead the frequency-dependent antenna impedance itself that determines the BW. Generally, a ~10 MHz BW was observed with real-life antennas. In that case, >50 dB isolation can be achieved in under 10 ms, using a particle swarm algorithm [15]. For dual-frequency FDD operation with a real antenna, more complex impedance structures are required, which is left as future work.

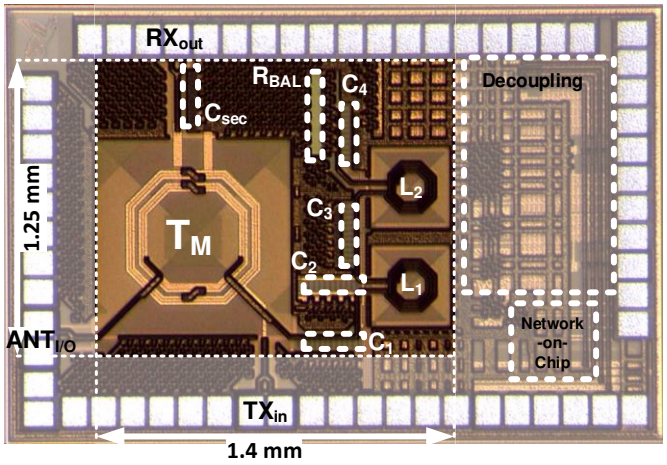

Fig. 11. 0.18µm SOI CMOS chip photo (from [16]).

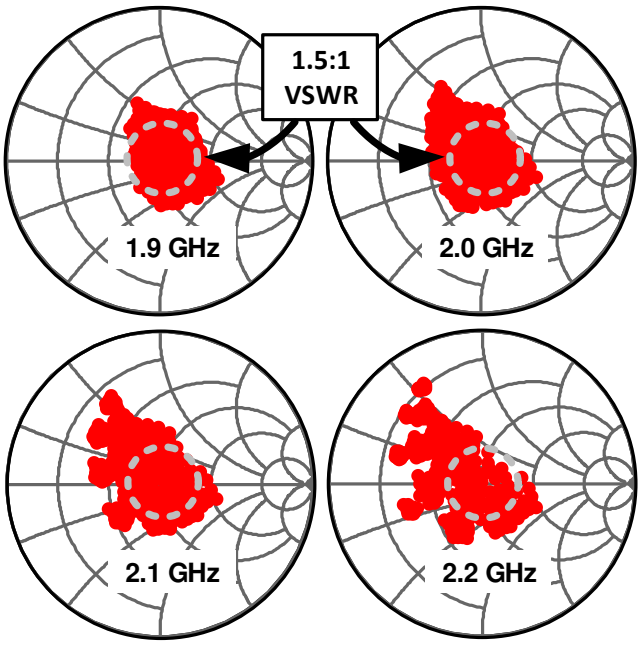

Fig. 12. Measured antenna-referred balance network impedance coverage range versus frequency (from [16]).

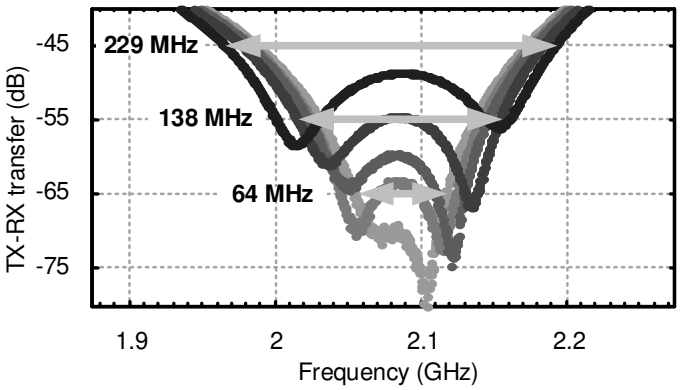

Fig. 13. Measured TX-RX isolation with a 50Ω termination on the antenna port, illustrating the four-dimensional tuning capabilities (from [16]).

In order to demonstrate that isolation can be maintained under typical high-power TX operating conditions, a large signal was applied to the TX port and the TX-RX isolation was observed. First, the balance network was tuned using a constant +5 dBm TX input power continuous wave (CW). Fig. 14 shows the resulting curve when the TX input power is swept. Due to the increased swing experienced by the switches in the balance network, the junction capacitances and channel resistance changes slightly at higher TX levels. This causes the overall network impedance to change with the TX input power. However, the isolation does not drop below 50 dB even up to +27.5 dBm. When re-calibrating the balance condition at this increased level and sweeping the TX power again, the impedances again vary with the input level but the isolation never drops below 50 dB across the entire input range. The authors estimate this change in peak isolation indicates that in fact the center frequency of the isolation peak is slightly offset as the switch impedance changes with the power level. This experiment shows for the first time that the isolation of an EB duplexer changes with the TX power and proves that the achievable impedance delta of an LSB capacitor unit cell is small enough to compensate for this effect.

To evaluate insertion loss and return loss across frequency, the balance network must be tuned to achieve isolation at each frequency point of interest. Fig. 15 shows the TX and RX IL for 5 points for which the impedance balance was tuned to achieve beyond 50 dB isolation and for which the RX loss is centered around the frequency of interest by tuning C_{sec}. The TX IL ranges from 3.4 to 3.7 dB and the RX IL from 3.8 to 3.9 dB. TX/RX return loss is better than -20/-15 dB, respectively. The respective TX and RX results are measured at the same time, under the same conditions and settings.

Also note the impedance variability (Fig. 15 top-right) seen looking into the TX port, due to the fact the TX is loaded by the parallel impedance of the antenna and the balance network. In the nominal case, 25 Ω would thus be the nominal impedance [5], and for these tests an L-C 50-to-25 Ω matching network has been used in series with the TX port to ensure optimal loss. For these tests, the antenna is a 50 Ω reference impedance, but the balance network exhibits significant variations across frequency, visible in the TX S11 profile.

Fig. 16 shows the measured IIP3 in the TX-path, i.e. the TX port is the input and the antenna port is the output. Details on the measurement setup and its limitations can be found in the Appendix at the end of this paper. The IIP3 (2-tone at 1.84/1.98 GHz) was observed for maximum/minimum/middle codes for all capacitors in the balance network: e.g. all switches "On", all switches "Off" and half of the MSB cells set to "Off", half to "On" while using the 01111 code for the binary LSBs. Little variation in the in-band TX loss is observed across code, but IMD3 observed at the antenna port does vary, leading to an IIP3 from +70 to +83 dBm. With 3.5 dB insertion loss, this leads to an OIP3 of approximately +67 to +80 dBm. This IIP3 is clearly high enough to not degrade the TX signal quality, i.e. the adjacent-channel leakage ratio (ACLR) [14].

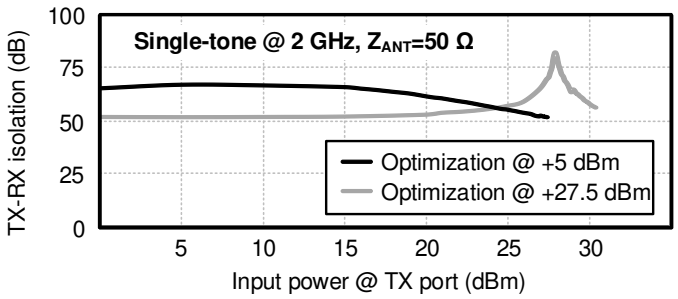

Fig. 14. Measured variation of the TX-RX isolation with TX input power and re-calibration at high TX input power.

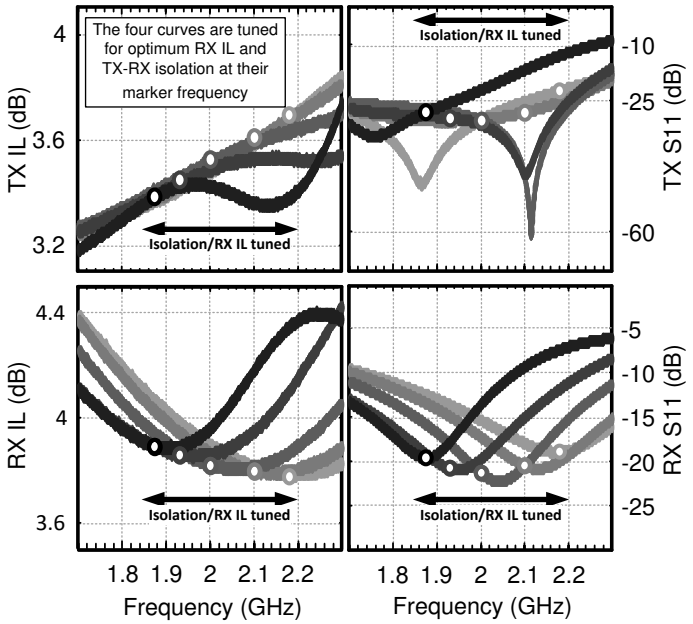

Fig. 15. Measured insertion loss and reflection coefficients (from [16]).

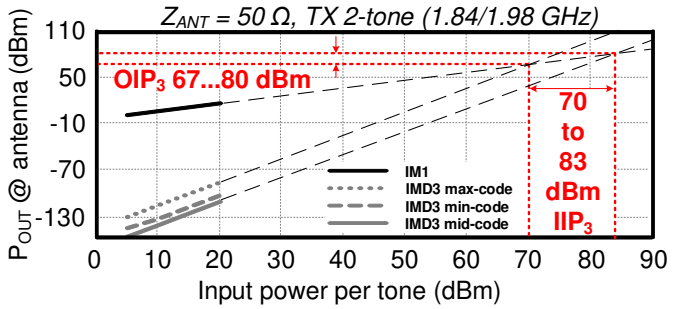

Fig. 16. Measured TX-path IIP3 for max/min/mid codes (from [16]).

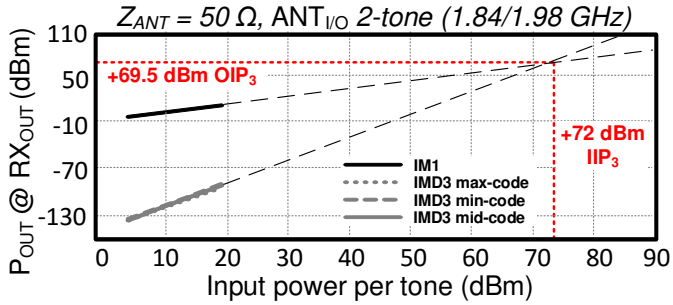

Fig. 17. Measured RX-path IIP3 for max/min/mid codes.

When the network is tuned across its tuning code range, the ratio between "On" and "Off" state capacitors leads to a change in nonlinearity. As mentioned above, the stand-alone capacitor banks are designed for similar distortion in both states, but as the V-I balance changes with code as well, it might be that a particular node inside the network experiences more voltage stress depending on the code.

Fig. 17 shows similar tests for the RX-path, i.e. a 2-tone test was performed with the antenna port as the input and the RX-port as the output. Across codes, much less variation is now observed, and a constant IIP3 of +72 dBm results. This can be explained by the fact that the balance network might no longer be the main linearity limitation: instead, it might be the RX-side C_{sec}, which also has limited linearity. In this test, the 2-tone experiences some attenuation before reaching the balance network (S_{TA} in Equation (1)), which was not the case in the TX-path test, where the 2-tone could transfer to the balance network with little attenuation (S_{BT} in Equation (1)).

Full-duplex-spaced and co-channel jammer tests were also performed and details on the measurement setup can again be found in the Appendix. Fig. 18 shows the results for both tests, showing that an FDS-jammer at the 3GPP maximum for +24 dBm at the antenna still has a margin of about 10 dB to a 1.4 MHz noise floor. The CC-jammer at the 3GPP maximum power level has more than 30 dB margin to the same specification, such that the FDS-jammer is indeed more stringent than the CC-jammer, as expected from Equations (2) and (3). Increased jammer levels are within specification up to 0 dBm (FDS-jammer), assuming a 5 MHz channel BW.

The EB duplexer provides little or no filtering at harmonic frequencies, while LTE transmit mask profile requires a maximum level of -30 dBm or -50 dBm for harmonics (depending on the band and/or harmonic frequency). Therefore, extensive tests for compliance were done.

First, Fig. 19 shows 2nd to 5th harmonic distortion measured at the antenna port for a +23 dBm TX input power for a *continuous wave* signal, again at max/min/mid codes for all capacitors. Second, 3GPP Bands 1, 2, 3 and 4 were tested for IMD2, HD2, IMD3 and HD3 at the antenna port, each time tuning the balance network for >50 dB of TX-RX isolation at the TX frequency. In this case, the harmonics originate from a 20 MHz *LTE-modulated* signal at increased power at +28 dBm. The test results are summarized in Table II, showing a similar range of distortion as in Fig. 18.

These test results shows that this EB duplexer performs better than typical multi-throw switch modules in the market today (e.g. SkyWorks Solutions, Inc. *SKY13488*). However, harmonics generated by the TX at the input of the duplexer still travel to the antenna without attenuation. For example, a typical PA in the market today achieves -50 dBc HD3 at +28 dBm, i.e. -17 dBm (e.g. SkyWorks Solutions, Inc. *SKY77764*). Without attenuation, this would clearly not comply with the LTE transmit mask. For this reason, the previously mentioned 50-to-25 Ω L-C matching network is used, configured as a low-pass network. In practice, e.g. for use with a co-integrated PA, the matching network may be added on-chip and reconfigured to calibrate matching for optimized loss at the

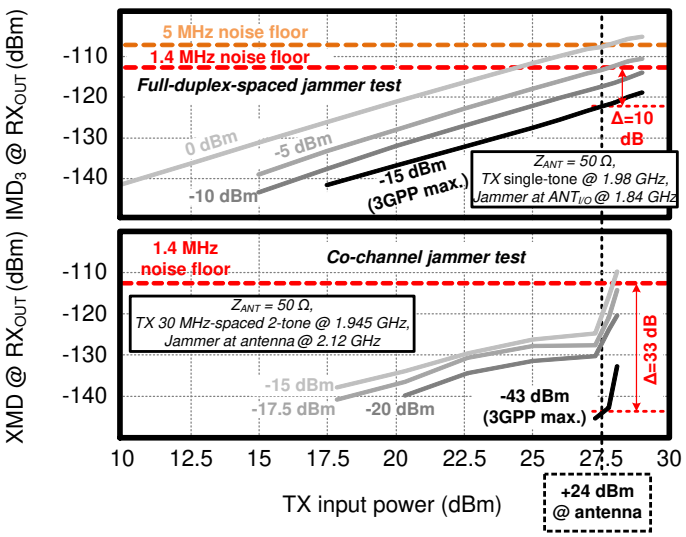

Fig. 18. Measured jammer-caused nonlinearity – full-duplex-spaced jammer (top) and co-channel jammer test (bottom). The jammer level is indicated next to each curve (from [16]).

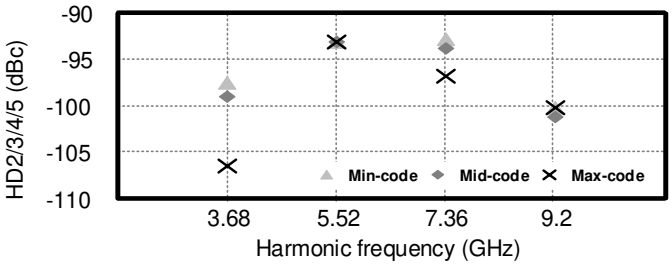

Fig. 19. Measured 2nd, 3rd, 4th and 5th harmonic distortion (output: antenna-port) at +23 dBm TX input power (CW) for max/min/mid codes.

TABLE II. IMD2/3* AND HD2/3** FOR 3GPP BANDS 1,2,3, AND 4.

Band	*IMD2* (dBm)*	*HD2** (dBm)*	*Band*	*IMD3*** (dBm)*	*HD3** (dBm)*
1	-119.4	-75.4	*1*	-111.0	-83.1
2	-108.5	-68.5	*2*	-116.7	-75.4
3	-97.6	-64.8	*3*	† N/A	-78.9
4	-113.7	-72.3	*4*	-113.7	-86.9

* -15 dBm CW jammer located at f_{RX} - f_{TX} and CW TX at +25 dBm.
** 20 MHz LTE-modulated TX signal at +28 dBm.
*** Full-duplex-spaced CW jammer at -15 dBm and CW TX at +25 dBm.
† There was no set of filters available for the Band3 IMD3 test.

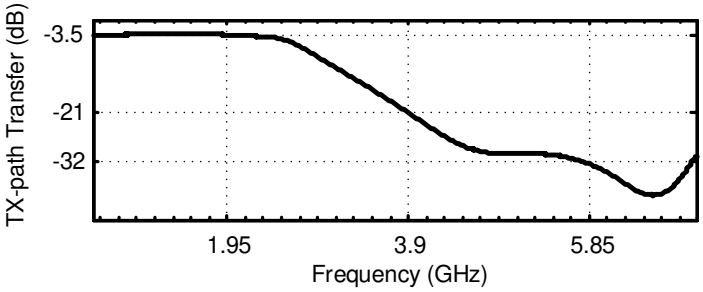

Fig. 20. Measured TX-path harmonic rejection when using a first-order off-chip low-pass matching network on the TX-port.

TABLE III. COMPARISON WITH STATE-OF-THE-ART.

Key specifications	JSSC'13 [7,10]	TMTT'13 [9]	TMTT'14 [12]	ESSCIRC'14 [14]	CICC'14 [13]	This work
Technology (CMOS)	65 nm	90 nm	90 nm	0.18 µm	0.18 µm	**0.18 µm SOI**
Z_{ANT} reference impedance	50 Ω	50 Ω	2:1 VSWR	SkyCross ant.	50 Ω	**1.5:1 VSWR**
Frequency range (GHz)	1.5-2.1	1.7-2.2	1.7-2.2	1.78-2	1.4-2.3	**1.9-2.2**
Z_{BAL} tuning dimensions	2	2	4	4	2	**4**
Area (mm^2)	0.2 incl. LNA	0.6 incl. LNA	2.2 incl. RX	0.67	0.35 incl. LNA	**1.75**
Small-signal operation						
Common-mode isol. (dB)	None (1 winding)	>60	>60	Poor	Single-ended	**Single-ended**
TX-to-RX isolation (dB)	>50	>60	>50	>50	>50	**>50**
Aggregated isol. BW (MHz)	600*	500*	N/A	220	900*	**300***
RX insertion loss (dB)	With LNA	With LNA	With RX	11	With LNA	**<3.9**
RX casc. NF (dB)	5.0	6.7**	6.7**	No LNA	<7.1	**No LNA**
TX insertion loss (dB)	2.5	4.7**	4.5**	3.0	<3.5	**<3.7**
Large-signal operation						
Max. P_{TX} at Antenna (dB)	<+12	+27	+27	+27	+22.6	**+27**
TX-to-Antenna IIP_3 (dBm)	N/A	N/A		>+48	N/A	**>+70**
Z_{BAL} IIP_3 (sim.) (dBm)	N/A	N/A	+54			**+65**
Antenna-to-RX IIP_3 (dBm)	N/A	-5.6 incl. LNA	-4.6 incl. RX	>+32	N/A	**+72**
IM_3 at EBD RX out (dBm)	N/A	N/A	N/A	Poor	N/A	**-124**
FD-spaced jammer						(24 dBm****)
XMD at EBD RX out (dBm)	N/A	-105***	-115***	Poor	N/A	**-145**
Co-channel jammer		(25.3 dBm****)	(17.5 dBm****)			(24 dBm****)

*Only measured with an almost frequency-constant reference impedance. **Assumes a balun with 0.8 dB loss. ***Referred to the LNA input for comparison using: [9] 14 dB LNA gain, [12] 43 dB Rx gain at 2.15 GHz. ****Tx power observed at the antenna port.

TX frequency. Fig. 20 shows the transfer characteristic up to the 3rd harmonic frequency to show that the network significantly improves harmonic rejection: 21/32 dB HR2/3 is observed for 3GPP Band 1 operation at 1.95 GHz. Using the example PA again, -50 dBm of harmonic distortion would result at the antenna when radiating +24 dBm. Therefore, sufficiently low distortion is achieved and the use of additional filters for harmonic distortion are avoided, at the antenna or otherwise.

These extensive linearity tests thus demonstrate the duplexer can comply with LTE in terms of linearity, both in terms of small-signal and large-signal distortion.

Another relevant test for typical operating conditions is chip heating, as the substrate conducts the dissipated TX energy to the main board. Fig. 21 shows the measured peak chip surface temperature versus TX input power, observed using a nano-probe touching the chip surface near the resistor. There, most heating is observed, since most power is also dissipated there. The chip heats up by about 35°C from a 'base' temperature of 27°C, reaching a maximum of 52°C at 30.5 dBm TX input power. This level of heating is much less than e.g. the PA.

Table III summarizes the measured performance and compares the results to other state-of-the-art work. This work presents the first stand-alone EB duplexer that demonstrates feasibility in two critical areas: it is the first to achieve >+70 dBm IIP3 and also achieves <3.7 dB TX insertion loss and <3.9 dB RX insertion loss. At the same time, it provides isolation levels, isolation BW, and impedance tuning abilities competitive with the state of the art. This duplexer withstands 3GPP-defined jammers at 3GPP-compliant TX power, hence indicating that the EB duplexer achieves sufficient linearity performance to operate in real-life conditions with a full-power modulated TX signal.

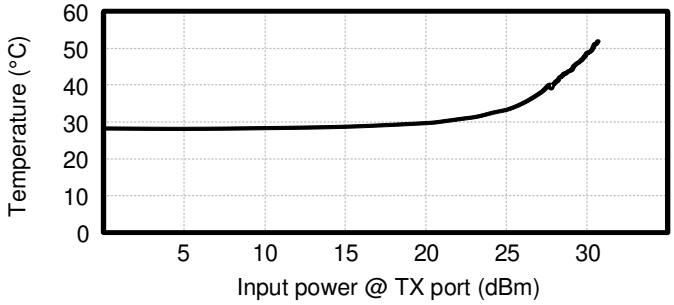

Fig. 21. Measured peak chip surface temperature versus TX input power.

VI. CONCLUSIONS

Electrical-balance duplexers have seen increased interest from industry and research institutions alike, promising to help implement a reconfigurable, frequency-flexible alternative to current-day FEM implementations and reduce the overall system footprint.

This paper presents an EB duplexer implementation in RF SOI CMOS, where high power handling and high linearity can be achieved through the ability to stack switch devices. Such a duplexer would fit in a reconfigurable FEM that can be used with SDR transceiver implementations to replace current non-tunable architectures.

In particular, this paper achieves state-of-the-art in terms of linearity: jammer-proof linearity performance and power-handling is demonstrated, with good stand-alone insertion loss

in both TX and RX paths. To support these claims, measured results of stringent jammer tests are shown to be exceeded, but TX-path harmonics, harmonic rejection and isolation under high TX power are demonstrated as well.

In terms of impedance tuning, future work is still required to enable true dual-frequency Z_{BAL} capability to provide TX-RX isolation at both frequencies simultaneously. Also, a further increase in the tuning range is needed to provide resilience to increased antenna variations. In addition, it is critical that the antenna variations themselves are reduced, e.g. by automated matching networks on the Z_{ANT} side. Practical BW limitations require further investigations, and can only be determined when the EB duplexer is evaluated or co-designed with a real antenna. Finally, demonstrating overall system performance by integrating the EB duplexer with other FEM building blocks is left as future work.

APPENDIX: HIGH-LINEARITY MEASUREMENTS

This Appendix describes the instrumentation setup used to measure and evaluate the duplexer linearity, for both the IIP3 and jammer intermodulation tests.

Passive components are very linear in nature, and can usually considered as 'perfectly linear' when compared to active devices, such as amplifiers. However, the reality is that even very linear passive devices have linearity limitations, and when >+70 dBm IIP3 must be accurately measured, an even higher IIP3 is required in the measurement setup itself. In this Appendix, we detail the required setup to enable accurate IIP3 measurements, which achieves a dynamic range of 131.5 dB at a +21.5 dBm two-tone level, implying a setup IIP3 limit of:

$$IIP3 = \frac{3A - IM3}{2} = \frac{3*21.5+110}{2} = +87.25 \text{ dBm} \qquad \text{(A1)}$$

where A is the two-tone level (e.g. each tone has level A) and IM3 is the IM3 as measured at the output of the DUT.

The key component that enables such a linear measurement setup is a triplexer (Fig. 22) constructed using highly linear *dielectric* filters. In an IIP3 test (e.g. TX-to-antenna path duplexer IIP3 test as shown in Fig. 22), the triplexer is used at the input-side to reduce generator cross-talk and at the output-side to suppress the two-tone, such that the spectrum analyzer (SA) will not be a primary distortion source.

The input network consists of two generators, each generating a single tone at frequencies f_1 and f_2, respectively, connected to the input port of a dielectric duplexer through an amplifier. The third port of the triplexer employs two series-connected dielectric filters at $f_{IM3}=(2*f_1-f_2)$. The main function of the amplifiers is loss compensation. However, the amplifiers also reduce generator cross-talk through S12. The dielectric filter at the IM3 frequency ensures a 50 Ω match at the IM3 frequency such that the setup-generated IM3 will be absorbed instead of leaking into the DUT. Two matching networks (M in Fig. 23) are used between the duplexer and the filter on the board that help to guarantee a 50 Ω impedance at f_1, f_2 and f_{IM3} simultaneously (from the DUT point-of-view)

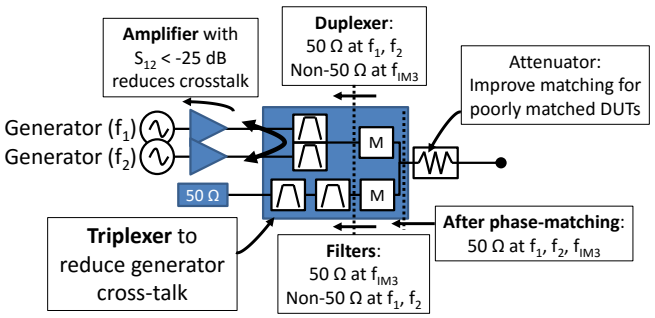

Fig. 22. Triplexer schematic (IIP3 measurement input-side network shown).

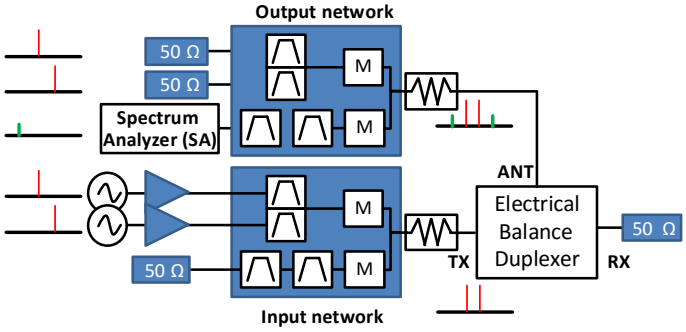

Fig. 23. TX-to-antenna path IIP3 measurement setup.

TABLE AI. COMPONENTS AND EQUIPMENT USED IN THE TESTS.

Component	*Manufacturer/Product*
Dielectric duplexer (Band 1)	Murata DFYH71G95HDNAC
Dielectric filter (2x)	Murata DFCH31G84HDJAA
Power amplifier	Mini-Circuits ZVE-8G+
Generator (2x)	Rohde & Schwarz SMA100A
Spectrum analyzer	Rohde & Schwarz FSW26

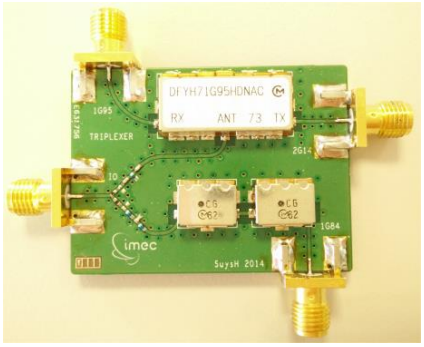

Fig. 24. Manufactured triplexer PCB photo used for the linearity tests.

through phase-matching, in which each network M rotates the phase of the filter/duplexer path to have a very high impedance at the center frequency of the other paths. Finally, a 3 dB attenuator between the triplexer and DUT improves matching in the case that the DUT itself is poorly matched.

The output network connects the triplexer in an inverse way, terminating the duplexer ports with 50 Ω to absorb the

2-tone and using a spectrum analyzer at the IM3 port to measure the DUT's output IM3. The components and equipment used and a picture of a mounted triplexer on a FR4-PCB are shown in Table AI and Fig. 24.

Fig. 25 shows the calibration procedure before measuring the DUT: IM1 level calibration of the input network (Fig. 25a), and the characterization of IM1 and IM3 loss in the output network (Fig. 25b). Then, the input and output networks are connected back-to-back (Fig. 25c), to observe the system's calibrated performance: a -110 dBm IM3 product is measured at +21.5 dBm two-tone level, indicating a +87 dBm IIP3 as previously calculated in Equation (A1).

A more complex measurement setup is required for testing with external jammers. In such cases, a triplexer network must be used on the antenna side to inject a jammer, a second network to inject the TX signal, and finally an output triplexer network to observe the distortion.

Fig. 26 and Fig. 27 show the setup for the full-duplex-spaced jammer and co-channel jammer tests, respectively. In both cases, the TX power is set to +27 dBm at the TX input, and a -15 dBm / -43 dBm jammer is applied at the antenna.

In the full-duplex-spaced test case, the jammer is injected at the lower frequency (1.84 GHz), the TX is injected in the middle frequency (1.98 GHz) so that the IM3 generated is observed at 2.12 GHz.

For the co-channel jammer test case, a 2-tone with a narrow tone-spacing is generated from a single generator (1.84 GHz) and a jammer is injected within the RX band (2.12 GHz). In this case, there is no concern about the IM3 generated near the two-tone. Instead, the XMD near the jammer can be observed in-band at the RX/jammer frequency, at 2.12 GHz.

Note that all of these test cases are only possible at the specific combination of frequencies that the dielectric filters allow. Testing for such high linearity across frequency either requires tunable, highly linear filters, or various combinations of triplexers.

ACKNOWLEDGMENT

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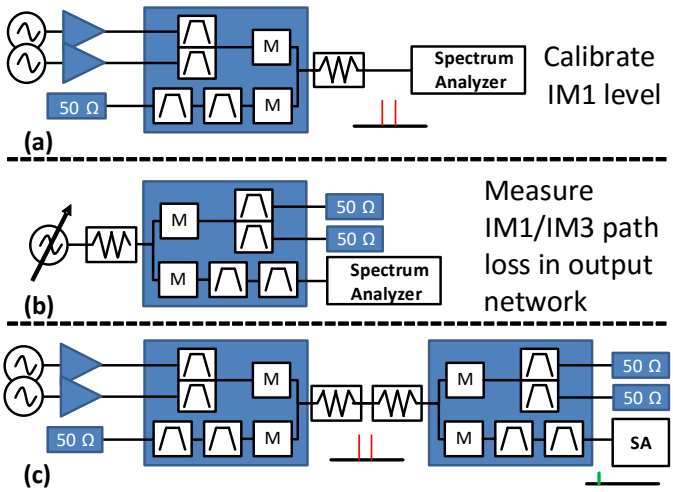

Fig. 25. Calibration of the triplexer filter bank: (a) DUT input level calibration, (b) IM1/IM3 output loss characterization, (c) back-to-back connection of in- and output networks to evaluate the setup IIP3 limit.

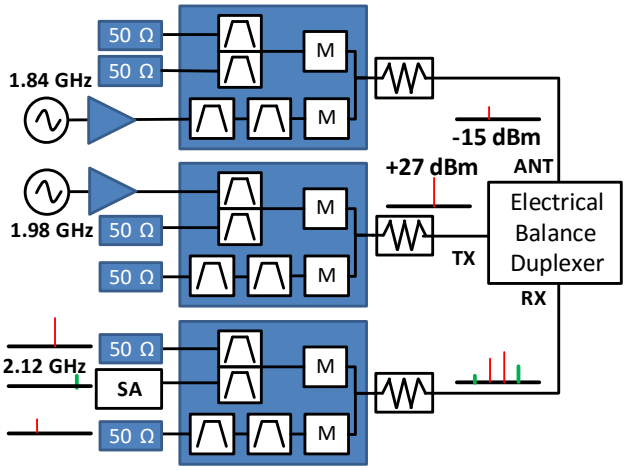

Fig. 26. Full-duplex-spaced jammer intermodulation measurement setup.

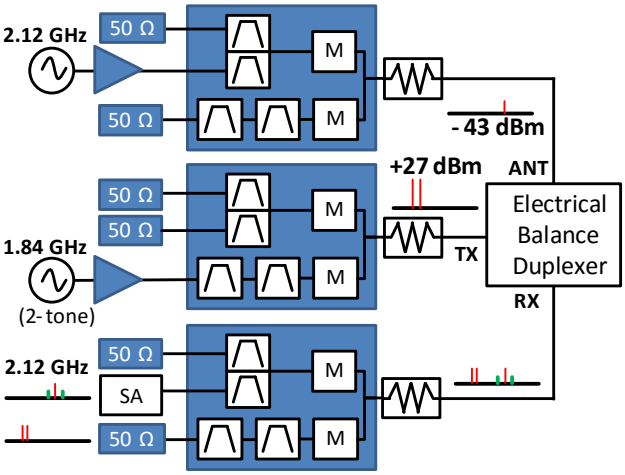

Fig. 27. Triple-beat test (co-channel jammer) measurement setup.

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