

 Open access • Journal Article • DOI:10.1109/4.482155

A 70-MS/s 110-mW 8-b CMOS folding and interpolating A/D converter

— [Source link](#) 

Bram Nauta, A.G.W. Venes





Institutions: Philips

Published on: 01 Dec 1995 - IEEE Journal of Solid-state Circuits (IEEE)

Topics: Time-to-digital converter, CMOS, Mixed-signal integrated circuit, Comparator and Amplifier

Related papers:

- [An 80-MHz, 80-mW, 8-b CMOS folding A/D converter with distributed track-and-hold preprocessing](#)
- [An embedded 240-mW 10-b 50-MS/s CMOS ADC in 1- \$\mu\text{m}\$ /sup 2/](#)
- [A 12 b 50 M sample/s cascaded folding and interpolating ADC](#)
- [An 8-bit video ADC incorporating folding and interpolation techniques](#)
- [A 10 b, 20 Msample/s, 35 mW pipeline A/D converter](#)

Share this paper:    

View more about this paper here: <https://typeset.io/papers/a-70-ms-s-110-mw-8-b-cmos-folding-and-interpolating-a-d-o5yyhgab3b>

A 70 Ms/s 110 mW 8-b CMOS folding and interpolating A/D converter

Citation for published version (APA):

Nauta, B., & Venes, A. G. W. (1995). A 70 Ms/s 110 mW 8-b CMOS folding and interpolating A/D converter. *IEEE Journal of Solid-State Circuits*, 30(12), 1302-1309. <https://doi.org/10.1109/4.482155>

DOI:

[10.1109/4.482155](https://doi.org/10.1109/4.482155)

Document status and date:

Published: 01/01/1995

Document Version:

Publisher's PDF, also known as Version of Record (includes final page, issue and volume numbers)

Please check the document version of this publication:

- A submitted manuscript is the version of the article upon submission and before peer-review. There can be important differences between the submitted version and the official published version of record. People interested in the research are advised to contact the author for the final version of the publication, or visit the DOI to the publisher's website.
- The final author version and the galley proof are versions of the publication after peer review.
- The final published version features the final layout of the paper including the volume, issue and page numbers.

[Link to publication](#)

General rights

Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

- Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
- You may not further distribute the material or use it for any profit-making activity or commercial gain
- You may freely distribute the URL identifying the publication in the public portal.

If the publication is distributed under the terms of Article 25fa of the Dutch Copyright Act, indicated by the "Taverne" license above, please follow below link for the End User Agreement:

www.tue.nl/taverne

Take down policy

If you believe that this document breaches copyright please contact us at:

openaccess@tue.nl

providing details and we will investigate your claim.

Special Issue Papers

A 70-MS/s 110-mW 8-b CMOS Folding and Interpolating A/D Converter

Bram Nauta, *Member, IEEE*, and Ardie G. W. Venes, *Member, IEEE*

Abstract—A CMOS analog to digital converter based on the folding and interpolating technique is presented. This technique is successfully applied in bipolar A/D converters and now also becomes available in CMOS technology. The analog bandwidth of the A/D converter is increased by using a transresistance amplifier at the outputs of the folding amplifiers and, due to careful circuit design, the comparators need no offset compensation. The result is a small area (0.7 mm^2 in $0.8 \mu\text{m}$ CMOS), high speed (70 MS/s), and low-power (110 mW at 5 V supply, including reference ladder) A/D converter. A 3.3 V supply version of the circuit runs at 45 MS/s and dissipates 45 mW.

I. INTRODUCTION

TODAY, the folding and interpolating technique is well established for use in high-speed bipolar analog to digital converters [1]–[3]. The advantage of a folding A/D converter is the reduced number of comparators compared to a full-flash converter while a sample-and-hold is not required, as in a multi-step architecture. The result is a high-speed, low-power data converter with small die area. This paper describes a folding and interpolating A/D converter in CMOS technology.

CMOS A/D converters with sample rates beyond 50 MS/s can be found in the literature [4], [5]. The design of [4] achieves a sample rate of 85 MS/s thanks to a parallel pipeline architecture. Another approach by Steyaert *et al.* is given in [5], where a current interpolation technique allows a sample rate of 100 MS/s. Both designs however have a power dissipation of more than 1 W, which is too much for embedded applications. Recently, folding and interpolating A/D converters in CMOS technology have also been reported [6], [7], which require significantly lower power. This paper describes the approach presented previously by the authors [7] and achieves a sample rate of 70 MS/s while dissipating only 110 mW. A 3.3 V supply version of this circuit runs at 45 MS/s and dissipates 45 mW.

Applications of CMOS folding and interpolating A/D converters can be found in high-speed signal processing, such as (oversampled) digitalization of video signals. The advantage of CMOS technology over bipolar is that the A/D converter can

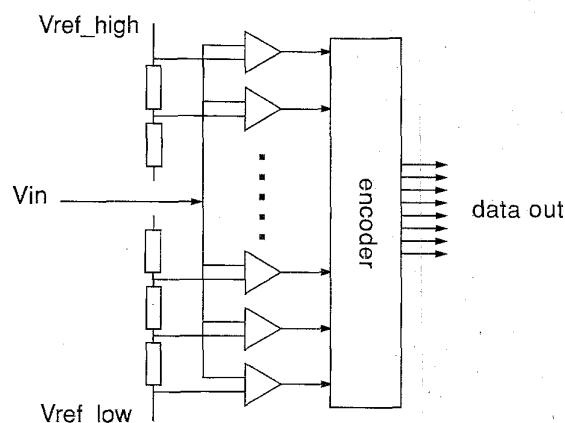


Fig. 1. Block diagram of a full-flash A/D converter.

be integrated on the same die as the digital signal processing part, resulting in a compact and cheap integrated system.

This paper starts with a description of the more general folding principle. After that more specific CMOS matters are described in the section “folding in CMOS.” The actual circuit is described and experimental results are given. The results are summarized in the conclusions.

II. FOLDING PRINCIPLE

A simple way to make a high-speed A/D converter is to use a full-flash structure as shown in Fig. 1. This type of converter consists of an array of $2^n - 1$ comparators with n being the number of bits. Each comparator is connected with one input to the input voltage and with the other input to a reference voltage. This reference voltage is generally generated by a resistor ladder. The outputs of the comparators are fed into encoding logic that generate the databits. The advantage of this full-flash converter is its ease of design and its inherently good high frequency behavior. For resolutions larger than 7 b, offset compensation is required in order to avoid using large transistors in the comparators for matching reasons. In Pelgrom *et al.* [8], an 8-b full-flash converter with offset compensation is described. The disadvantage of full-flash converters is clear; if for example 8 b are needed, 255 comparators are required resulting in large chip area and power consumption, while

Manuscript received May 10, 1995; revised August 27, 1995.

The authors are with the Philips Research Laboratories, Eindhoven, The Netherlands.

IEEE Log Number 9415833.

0018-9200/95\$04.00 © 1995 IEEE

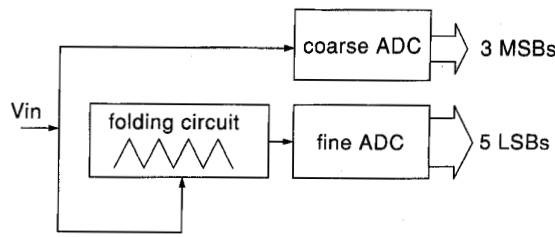


Fig. 2. Block diagram of a folding A/D converter.

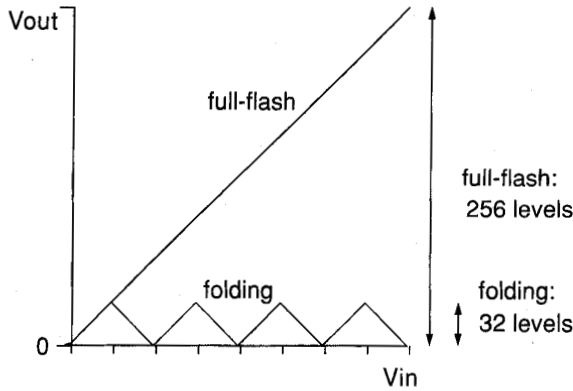


Fig. 3. Transfer curve of folding circuit (zig-zag) in comparison with transfer curve that would belong to a full-flash A/D converter (straight line).

offset compensation results in loss of conversion speed because the comparator offsets have to be compensated during each clock cycle.

The most popular technique nowadays in CMOS technology to deal with power and area is the two- or multi-step approach [9]. This topology requires a sample-and-hold operation and has the advantage that the number of comparators can be significantly lower than that of the full flash resulting in a saving of power and area. A disadvantage is that offset compensation is still required, and thus, the sample rate cannot be too high for an acceptable power consumption.

The folding technique has also a lower comparator count than a full-flash, and thus, low power and small area potentials. If well implemented, the folding type converter operates without offset compensation and therefore allows higher sample rates. Fig. 2 shows the block diagram of a folding A/D converter. The input voltage is applied to a preprocessing circuit depicted as the "folding circuit," and the output of this folding circuit is connected to a 5-b fine A/D converter. The input signal is also directly connected to a 3-b coarse A/D converter. The operation of the folding circuit is illustrated in Fig. 3, where the transfer function of the folding circuit is given. The "zig-zag" shaped transfer curve covers the whole V_{in} range, and the output voltage of the folding circuit needs to be converted to only 32 levels corresponding to the five least significant bits (LSB's) of the A/D converter output code. In order to distinguish the eight possible input voltages that correspond to the same folding signal output, the 3-b coarse A/D converter is required, which generates the three most significant bits (MSB's) of the A/D converter. The total comparator count for

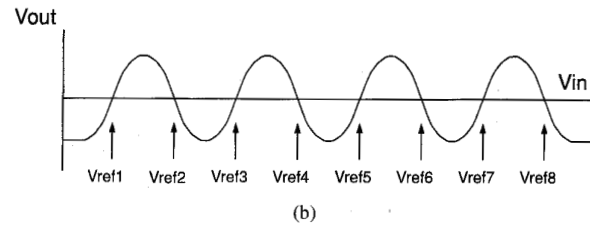
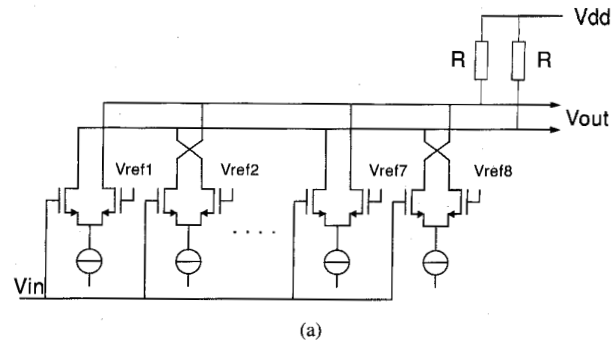


Fig. 4. (a) Basic principle of implementing a folding amplifier in CMOS technology. (b) The transfer curve of the circuit of figure (a).

this folding converter is 32 (fine) + 8 (coarse) = 40, which is much less than the 255 required for a full-flash. Note that the three most significant bits and the five least significant bits are generated synchronously, and thus, a sample-and-hold function is basically not required. The throughput of a folding A/D converter is equal to that of a full-flash, while a two or multi-step converter requires several clock cycles to convert the data. The transfer of the folding circuit in Fig. 3 is called "8-times-folding" because for each folding output there are eight possible input voltages. Other folding factors are possible; lower folding factors require more fine comparators while higher folding factors result in, amongst other things, more preprocessing hardware. Eight-times-folding for an 8-b A/D converter appears to be a good choice.

III. FOLDING IN CMOS

In order to generate the folding signal, a circuit used in bipolar folding converters [1] is converted to CMOS. This circuit is shown in Fig. 4(a). The circuit consists of eight differential pairs with the outputs of the odd- and even-numbered differential pairs cross coupled. The inputs of the differential pairs are connected to the converter input voltage and reference voltages ($V_{ref1} \dots V_{ref8}$) generated by a resistor ladder. The currents are summed at the output nodes through resistors. The differential output voltage versus input voltage is plotted in Fig. 4(b). The tops of this folding signal are somewhat rounded compared to the transfer of Fig. 3; this will be discussed later. A typical range of V_{in} is $1 \dots 2V_{pp}$, and since the eight input windows of the differential pairs have to fit within this voltage, the transistors have small $V_{gs} - V_t$ values and thus operate in moderate inversion. The consequence of this is a large W/L ratio (100/1) for the input devices and small tail currents (40 μA) of the differential pairs. The resulting parasitic capacitances at the output nodes are large (2 pF).

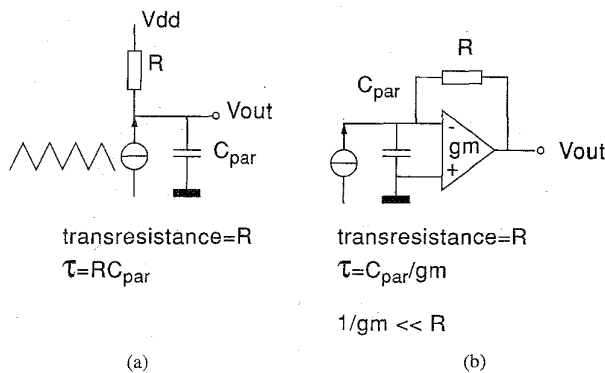


Fig. 5. (a) Illustration of the bandwidth problem encountered at the outputs of the folding amplifier of Fig. 4(a). (b) The bandwidth of the folding amplifier can be increased a factor $gm \cdot R$ by adding an OTA acting as a transresistance amplifier.

On the other hand, the values of the resistors R in Fig. 4(a) have to be large ($5 \text{ k}\Omega$) to allow large output voltages. The latter is required to reduce sensitivity to offsets in the rest of the converter. Note that the eight times folded signal has a bandwidth of 4π of the full swing input signal bandwidth due to the nonlinear folding operation. The large R and C_{par} therefore give rise to serious analog bandwidth limitations, as reported in [6]. Fig. 5 illustrates this problem.

To avoid this problem, a transresistance amplifier is used as shown in Fig. 5(b). The OTA with transconductance gm has a feedback resistor R ($5 \text{ k}\Omega$). The folding current is fed into this resistor and can generate a large output voltage. The input and output impedance of the transresistance stage are both $1/gm$ and can be made low (250Ω), and thus, the analog bandwidth is increased by a factor $gm \cdot R$ (20 times). An additional advantage of the circuit of Fig. 5(b) is its low output impedance; this facilitates driving the next stage.

It was noted already that the tops of the folding signals of Fig. 4(b) are rounded. This need not to be a problem if we consider Fig. 6. Here, two folding signals are plotted with different offsets w.r.t. the input voltage. If one folding signal is in its nonlinear region, the other is in its linear region and vice versa. Thus, instead of needing one good folding signal with the detection of 32 levels, we also can take two folding signals with the detection of 16 levels for each folding signal. This reasoning can be expanded up to 32 folding signals with the detection of only one level per signal [1]. The problem is now that the generation of 32 folding signals with $32 \cdot 8$ differential pairs is as much hardware as a full-flash converter. Interpolation can be used to circumvent this dilemma [1].

Fig. 7 shows the principle of interpolation. Four folding amplifiers generate four folding signals with a mutual offset equal to $1/32$ nd of the full scale input. In the configuration of Fig. 7, four additional folding signals are generated by a resistor ladder from the existing four, resulting in a total of eight folding signals. The interpolation can be repeated until 32 folding signals are generated. The resistive interpolation technique is a power-efficient method to generate additional signals. In a differential circuit, the signal currents through the resistors are forced to flow in a circle, and no current is wasted. The low output impedance of the circuit of Fig. 5(b) can drive

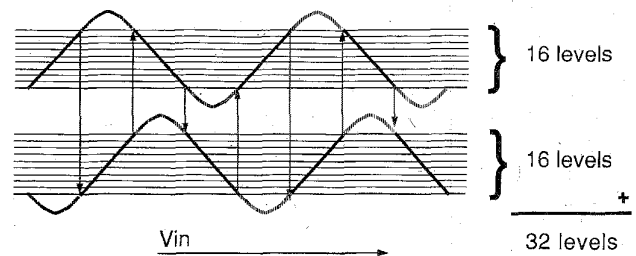


Fig. 6. One folding signal will have rounded tops. If two folding signals are used, with offset w.r.t. the input voltage, always one of the two folding signals is in its linear region. In this case, each folding signal needs detection of 16 levels, compared to the detection of 32 levels for the case of only one folding signal.

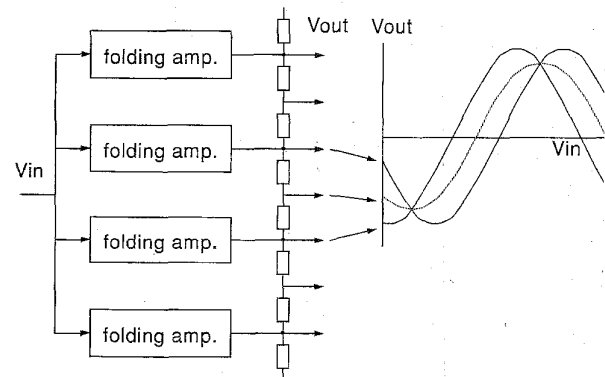


Fig. 7. Illustration of the resistive interpolation principle; the resistor ladder doubles the number of folding signals with little hardware.

the resistors directly. Note that the tops of the interpolated folding signals are not fully correct. This is not important since only the zero-crossings are of importance.

IV. CIRCUIT DESCRIPTION

Fig. 8 shows the block diagram of the CMOS folding A/D converter. The system consists of four folding amplifiers that generate four folding signals (voltages). These folding signals are fed into a first resistive interpolation network, and the resulting eight folding signals are fed into eight amplifiers for eight-times signal amplification. The eight amplified folding signals are fed into a second resistive interpolation network for additional interpolation. The resulting 32 folding signals are fed into comparators. The whole signal path, apart from the input voltage, is fully differential.

The folding amplifiers are shown in Fig. 9(a). The circuit consists of eleven differential pairs with tailcurrents I_s and a dummy structure. This large number can be explained as follows. Eight differential pairs are needed for a folding signal as was explained in Fig. 4. Two additional differential pairs are needed for the extension of the folding signals for the low and high side of the input range to allow interpolation in that region. The circuit is fully differential, and therefore, one additional differential pair is needed for proper dc balance, resulting in a total number of differential pairs of eleven. The circuit has relatively large parasitic capacitances due to the moderate inversion operation of the differential pairs. Since the

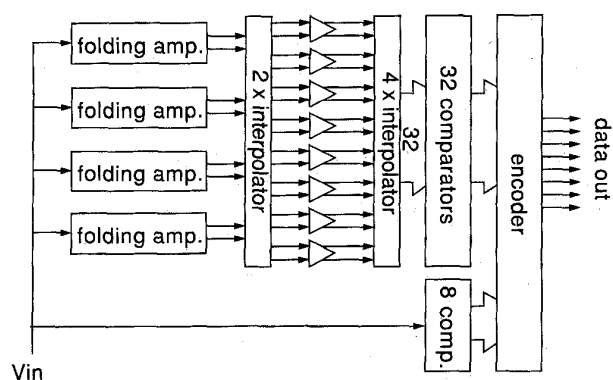


Fig. 8. Block diagram of the folding and interpolating A/D converter.

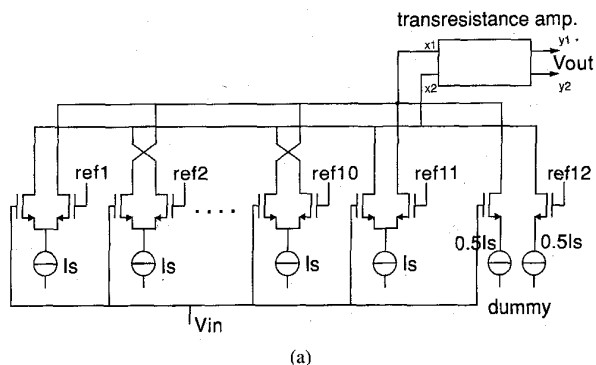
differential pairs are connected cross-coupled, it can be shown that the parasitic currents, due to the parasitic capacitances, are mainly of common-mode. Two neighboring differential pairs have almost equal parasitic currents however with opposite sign connected to the summation points $x1$ and $x2$. Differential pairs 1 and 2 compensate, 3 and 4 compensate, and so on. Since the total number of differential pairs is eleven and thus odd, a dummy structure, in the form of a differential pair without coupled sources, is added to compensate the parasitic currents of differential pair 11. From Fig. 9(a), it can be seen that a transresistance amplifier performs the current-to-voltage conversion.

Fig. 9(b) shows the most straightforward implementation of this transresistance amplifier based on the OTA-R circuit of Fig. 5(b). The current sources $I1$ and $I2$ deliver the dc bias current for the eleven differential pairs and dummy structure and have each a value $6I_s$. The directions of these currents are illustrated with bold lines in Fig. 9(b). This circuit functions well as long as the current sources $I1$ and $I2$ are perfectly matched. However, the matching demands of these current sources are very strong; the signal current into the transresistance amplifier is small ($<I_s$) compared to the bias sources $I1$ and $I2$. A small percentage of mismatch of $I1$ and $I2$ results in an absolute offset current that is large w.r.t. the signal current. The result is a large INL (integral nonlinearity) error for the A/D converter.

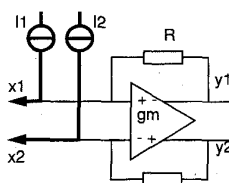
This problem of mismatch in $I1$ and $I2$ can be solved by moving the current sources $I1$ and $I2$ to the back-end of the OTA as shown in Fig. 9(c). The bias currents $I1$ and $I2$, still valued $6I_s$, now flow through the resistors R into the differential pair structure of Fig. 9(a). Mismatch in $I1$ and $I2$ now results in an offset voltage between nodes $x1$ and $x2$. The value of the offset voltage is

$$v_{\text{off}} = \frac{I1 - I2}{gm} \quad (1)$$

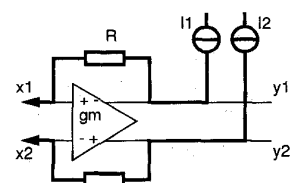
with gm being the transconductance of the OTA. This offset voltage with a σ value of 1 mV is present at a current input and has therefore no effect, since the transresistance amplifier only sees an input current. The offset voltage of (1) is also present at the output nodes $y1$ and $y2$ of the transresistance amplifier, however, the signal voltage is large (200 mVpp) and causes no serious problems.



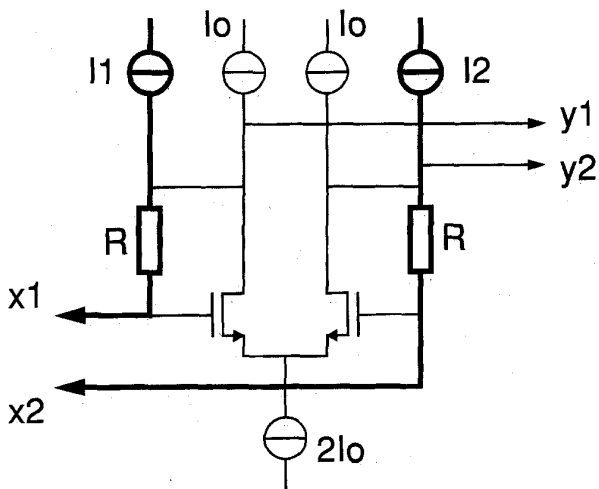
(a)



(b)



(c)



(d)

Fig. 9. (a) Realization of the folding amplifier as used in Fig. 8. (b) Implementation of the transresistance amplifier as used in the circuit of Fig. 9(a). Extreme matching demands are put upon the bias current sources $I1$ and $I2$. (c) By moving the current sources $I1$ and $I2$ to the outputs of the transresistance amplifier, the matching demands on these sources are relaxed. The bias currents flow through the resistors R . (d) Practical implementation of the transresistance amplifier as used in Fig. 9(a).

The actual circuit implementation of the transresistance amplifier is shown in Fig. 9(d) where the OTA is simply implemented with a differential pair. Diffusion resistors are used in the circuit for matching reasons, while linearity is of no importance. A simple common mode feedback loop controls the common mode voltage of nodes $x1$ and $x2$, and thus $y1$ and $y2$. The common mode voltage is sensed at the common source node of the OTA and controls the tailcurrents I_s of the differential pairs of Fig. 9(a).

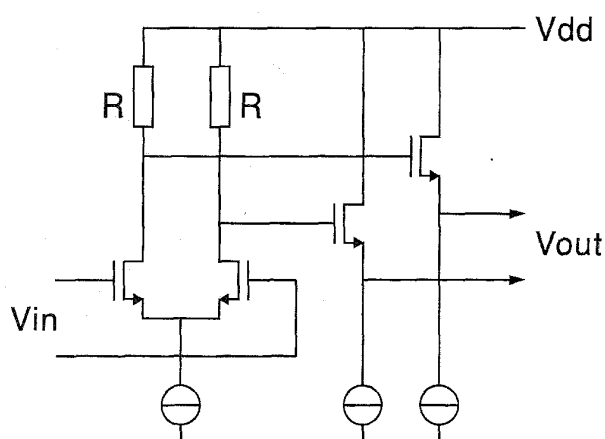


Fig. 10. Implementation of the amplifier as used in the block diagram of Fig. 8.

The low-ohmic outputs y_1 and y_2 of the folding amplifier are connected to the first interpolation ladder, and the eight differential folding signals are fed into eight amplifiers as shown in Fig. 10. The amplifier is straightforwardly designed as an eight times gain stage loaded with source followers to drive the second interpolation ladder. The exact value of the gain is not critical.

After the second interpolator, the 32 differential folding signals are fed into 32 comparators for detection of the zero-crossings. The comparator schematic is given in Fig. 11 and consists of a folded cascode structure (M1–M4) loaded with a latch structure (M5–M7). The reset signal of the latch is connected to the gate of M7. The network M8 and M9 limits the voltage swing at the nodes $d1$ and $d2$, which are connected to a digital slave flip-flop. The comparator of Fig. 11 needs no offset compensation because the input signal is relatively large due to signal amplification in the folding circuits; 1 LSB equals 30 mV while σ_{offset} of the comparator is equal to 2.5 mV. The offset of the comparator can be calculated using matching theory [10]. As a result of the absence of offset compensation, the clock frequency can be very high.

Eight comparators as in Fig. 11 are used in the coarse A/D converter of the folding A/D converter. Six comparators are required for the MSB and MSB-1 generation [2] while two additional comparators are used for overflow and underflow detection. The noninverting inputs of these comparators are connected to the input signal of the A/D converter, and the inverting inputs are connected to taps of the same reference ladder as the four folding amplifiers. Similarly, as in the fine A/D converter, the comparators in the coarse A/D converter may also have significant offset voltages. The zero-crossings of one of the folding signals represent the MSB-2 b transitions and the output signals of the eight coarse comparators are digitally synchronized with these zero-crossings. The coarse comparators now may have an offset voltage of 1/16 of the input voltage range of the A/D converter.

The preprocessing of the input voltage to 32 folding signals takes about 4 ns. For this reason, the clock signals of the fine A/D converter have to be delayed w.r.t. the coarse A/D converter. For a maximal input frequency of 10 MHz, this delay

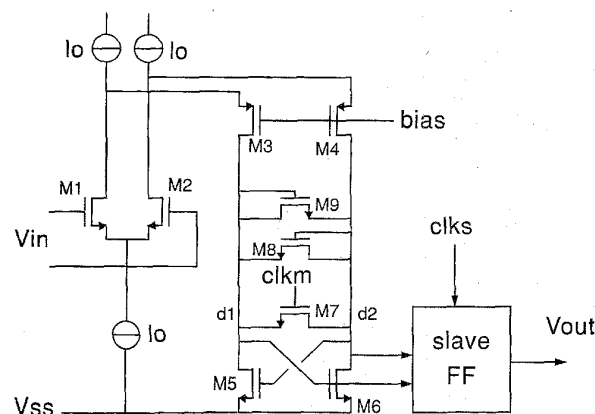


Fig. 11. Implementation of the comparators as used in the block diagram of Fig. 8.

must be larger than 2 ns and smaller than 6 ns. If this is the case, then the digital correction can correct the timing errors. The delay of the clock signals is implemented with a dummy circuit that delay tracks the delay of the preprocessing circuitry over temperature and process variations.

The thermometer code coming from the comparators in the fine A/D converter is first fed through a digital error correction network. This network removes the so-called “bubbles” from the thermometer code. The bits are encoded via logic gates. All digital hardware in this converter is standard CMOS. Current steering logic, as used in [6], produces less substrate noise. However, current steering logic requires more power if the logic activity is low. More important, a CMOS A/D converter must be applicable in fully integrated digital VLSI systems that will contain substrate noise anyway. This A/D converter is designed in such a way that substrate noise has minimal effect, e.g., by differential design.

An important feature of this A/D converter is the absence of offset compensation in the comparators. This allows a factor 2–3 higher sample rate than in designs with offset compensation. Several measures have been taken in this design in order to avoid offset compensation.

- 1) The input transistors of the folding amplifiers are large ($W/L = 100/1$), and therefore, offsets are small.
- 2) The biasing of the folding amplifiers at the outputs instead of the inputs of the transresistance amplifiers causes the offset in the bias current sources I1 and I2 to have hardly any effect.
- 3) Signal gain in the preprocessing circuit results in large comparator input voltages (30 mV/LSB), so that comparator offsets ($\sigma_{\text{offset}} = 2.5$ mV) are acceptable.
- 4) Resistive interpolation helps in reducing offsets. The interpolated signals are always in between the signals driving the interpolation ladder, and thus, smooth A/D converter transfer function is the result. This has positive impact on the DNL (differential nonlinearity) of the converter. Furthermore, the signals driving the interpolation ladder influence each other a little due to the nonzero source impedance driving the ladder. This results in an even smoother transfer of the A/D converter [11].

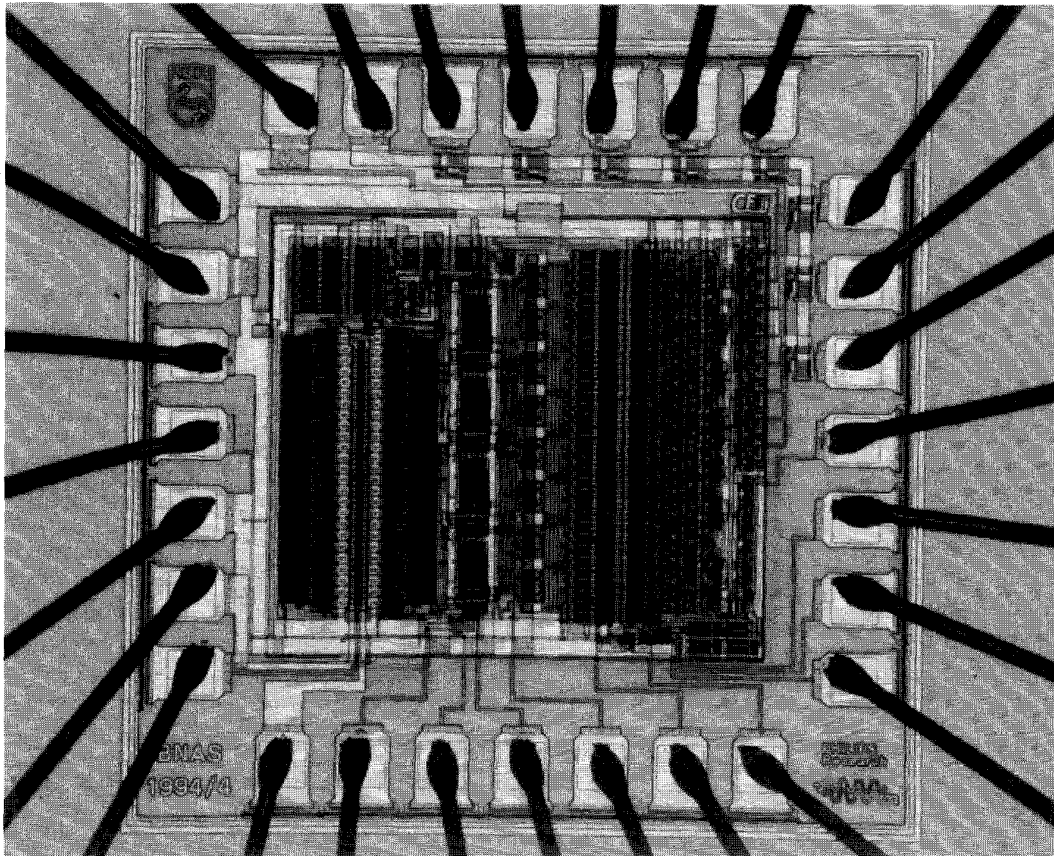


Fig. 12. Chip photograph. The circuit is fabricated in a 0.8 μm CMOS process and the active area is 0.7 mm^2 .

V. EXPERIMENTAL RESULTS

Two versions of the A/D converter have been realized in standard 0.8 μm CMOS technology. One circuit operates on 5 V and the other at 3.3 V supply. Differences are found in dimensioning of circuit parameters such as current and resistor values.

Fig. 12 shows the chip photograph. The area of the converter is 0.7 mm^2 .

Fig. 13(a) shows the measured differential nonlinearity (DNL) for the 5 and the 3.3 V version of the circuit. Fig. 13(b) shows the measured integral nonlinearity (INL) for both circuits. These DNL and INL curves were measured for low frequency (100 kHz) input signals while the clock frequency was 25 MHz for the 3.3 V circuit and 40 MHz for the 5 V circuit. The low DNL values proof that offset compensation of the comparators is indeed not necessary.

The dynamic performance of the converters is plotted in Fig. 14. The signal to noise and distortion ratio is expressed in Effective Number Of Bits (ENOB)

$$\text{ENOB} = \frac{20 \log \left(\frac{\text{signal}}{\text{noise} + \text{distortion}} \right) - 1.76}{6.02}. \quad (2)$$

An ideal 8-b A/D converter has no distortion, and the only noise is quantization noise of -50 dB, and has, according to

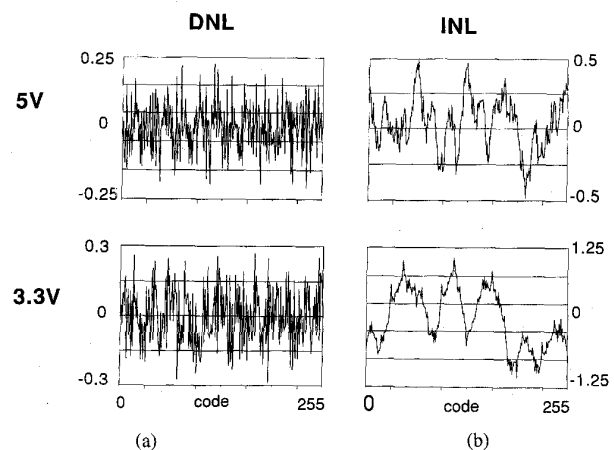


Fig. 13. (a) Measured differential nonlinearity (DNL) and (b) integral nonlinearity (INL) errors of the 5 and 3.3 V supply circuits.

(2), 8.0 effective bits. For each 6 dB loss in signal-to-noise-and-distortion, the ENOB is reduced by 1.

The 5 V design achieves 7.7 effective bits for low analog input frequencies and a sample rate of 40 MS/s. The ENOB decreases with increasing analog input frequencies, which is due to the finite bandwidth of the circuit together with the

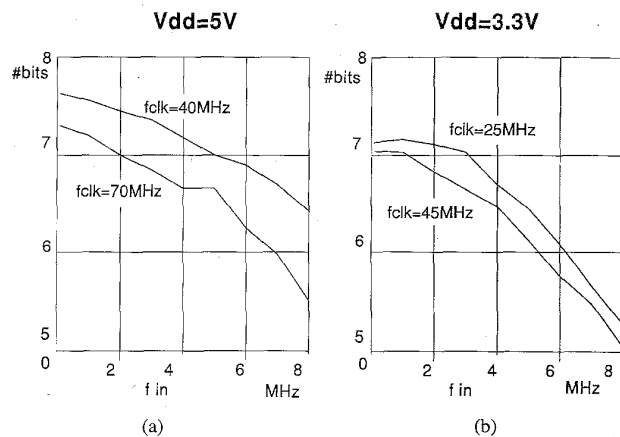


Fig. 14. (a) Measured effective number of bits for the 5 V supply circuit and (b) for the 3.3 V circuit.

TABLE I

parameter		
resolution	8bit	
input capacitance	4.8 pF	
reference ladder resistance	720 Ω	
active area	0.7 mm ²	
technology	0.8 μ m, 1 poly, 2 metal, CMOS	
supply voltage	$V_{dd}=5V$	$V_{dd}=3.3V$
analog input	2Vpp	1.4Vpp
Integral nonlinearity	$\pm 0.5LSB$	$\pm 1.0LSB$
Differential nonlinearity	$\pm 0.2LSB$	$\pm 0.3LSB$
max. clock frequency	70MHz	45MHz
power dissipation	110mW	45mW

much higher (factor 4π) internal frequencies of the folding circuitry. If the clock frequency is increased to about 65 MHz, the performance does not change much. At 70 MS/s, the ENOB drops to a lower value while at 75 MS/s the circuit produces large bit errors. The 3.3 V design shows similar behavior; 7.2 effective bits for low input frequencies and 25 MS/s sample rate. The sample rate could be increased to 45 MS/s. Although basically not needed, a sample-and-hold circuit can be used if larger analog bandwidths are required.

All the measurements were carried out on a HP82000 mixed mode test system.

The experimental results are summarized in Table I.

VI. CONCLUSIONS

The folding and interpolating technique has successfully been demonstrated in CMOS technology. The analog bandwidth has been increased a factor 20 compared to a straight-forward implementation due to the use of a transresistance amplifier at the outputs of the folding circuits. The circuit

requires no offset compensation, which is accomplished with several measures throughout the A/D converter. The result is a small (0.7 mm², in 0.8 μ m CMOS technology), low power (110 mW at 5 V supply, including reference ladder) and high sample rate (70 MS/s) A/D converter. A 3.3 V supply version of the circuit achieves a sample rate of 45 MS/s while dissipating 45 mW. The A/D converter circuit is designed for applications in digital VLSI systems.

REFERENCES

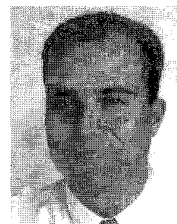
- [1] R. E. J. van de Grift, I. W. J. Rutten, and M. van de Veen, "An 8-b video ADC incorporating folding and interpolation techniques" *IEEE J. Solid-State Circuits*, vol. 22, no. 6, pp. 944-953, Dec. 1987.
- [2] R. J. van de Plassche and P. Baltus, "An 8-b 100 MHz full-Nyquist analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 23, no. 6, pp. 1334-1344, Dec. 1988.
- [3] C. J. van Valburg and R. J. van de Plassche, "An 8 b 650 MHz folding ADC," *IEEE J. Solid-State Circuits*, vol. 27, pp. 1662-1666, Dec. 1992.
- [4] C. S. Conroy, D. W. Cline, and P. R. Gray, "An 8-b 85-MS/s parallel pipeline A/D converter in 1 μ m CMOS," *IEEE J. Solid-State Circuits*, vol. 28, pp. 447-454, Apr. 1993.
- [5] M. Steyaert, R. Roovers, and J. Craninckx, "A 100 MHz 8 b CMOS interpolating ADC," in *Proc. CICC'93*.
- [6] M. Flynn and D. Allstot, "CMOS folding ADC's with current-mode interpolation," in *Proc. ISSCC'95*.
- [7] B. Nauta and A. Venes, "A 70 MS/s 110 mW 8-b CMOS folding and interpolation A/D converter," in *Proc. ISSCC'95*.
- [8] M. Pelgrom, A. van Rens, M. Vertregt, and M. Dijkstra, "A 25 MS/s 8-b CMOS A/D converter for embedded application" *IEEE J. Solid State Circuits*, vol. 29, pp. 879-886, Aug. 1994.
- [9] N. Fukushima, T. Yamada, N. Kumazawa, Y. Hasegawa, and M. Soneda, "A CMOS 40 MHz 8 b 105 mW two-step ADC," in *Proc. ISSCC '89*, pp. 14-15.
- [10] M. Pelgrom, A. Duinmaier, and A. Welbers, "Matching properties of MOS transistors," *IEEE J. Solid State Circuits*, vol. 24, no. 5, pp. 1433-1440, Oct. 1989.
- [11] K. Kattmann and J. Barrow, "A technique for reducing differential nonlinearity errors in flash A/D converters," in *Proc. ISSCC '91*, pp. 170-171.



Bram Nauta (S'89-M'91) was born in Hengelo, The Netherlands, in 1964. He received the M.S. degree (cum laude) in electrical engineering from the University of Twente, Enschede, The Netherlands, in 1987 on the subject of BIMO amplifier design. In 1991, he received the Ph.D. degree from the same university on the subject of analog CMOS filters for very high frequencies.

In 1990, he cofounded Chiptronix Consultancy and gave several courses on analog CMOS design in the industry. In 1991, he joined the Analog Integrated Electronics Group of Philips Research Laboratories, Eindhoven, The Netherlands, where he is engaged in analog signal processing.

For his Ph.D. work, Dr. Nauta received the "Shell study tour award" and his Ph.D. thesis is published as a book, *Analog CMOS Filters for Very High Frequencies* (Norwell, MA: Kluwer, 1993).



Ardie G. W. Venes (M'94) was born in Doetinchem, The Netherlands, in 1970. He received the M.S. degree in electrical engineering from the University of Technology, Eindhoven, The Netherlands in 1993 on the subject of CMOS folding A/D conversion.

In the same year, he joined Philips Research Laboratories, Eindhoven. In the Integrated Transceivers Group, he is involved in embedded analog front-end design for signal processing applications.