A 77-GHz Phased-Array Transceiver With On-Chip Antennas in Silicon: Transmitter and Local LO-Path Phase Shifting

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***Abstract*—Integration of mm-wave multiple-antenna systems on silicon-based processes enables complex, low-cost systems for high-frequency communication and sensing applications. In this paper, the transmitter and LO-path phase-shifting sections of the first fully integrated 77-GHz phased-array transceiver are presented. The SiGe transceiver utilizes a local LO-path phase-shifting architecture to achieve beam steering and includes four transmit and receive elements, along with the LO frequency generation and distribution circuitry. The local LO-path phase-shifting scheme enables a robust distribution network that scales well with increasing frequency and/or number of elements while providing high-resolution phase shifts. Each element of the heterodyne transmitter generates +12.5 dBm of output power at 77 GHz with a bandwidth of 2.5 GHz leading to a 4-element effective isotropic radiated power (EIRP) of 24.5 dBm. Each on-chip PA has a maximum saturated power of +17.5 dBm at 77 GHz. The phased-array performance is measured using an internal test option and achieves 12-dB peak-to-null ratio with two transmit and receive elements active.**

***Index Terms*—Integrated circuits, LO-path, mm-wave, multiple antenna, phase interpolation, phase rotator, phase shifters, phased array, power amplifier, radar, SiGe, transceiver, transmitter.**

I. Introduction

INTEGRATED mm-wave systems are the next step in the continuous effort to extend the advantages of silicon-based integration to yet higher frequencies. This move towards mm-wave frequencies is spurred by two forces—first, the need to lower system cost and improve system performance for potentially widespread sensing applications like 24-GHz and 77-GHz vehicular radar [1]–[5] and second, the desire to achieve high data rates by leveraging the larger bandwidths available at higher frequencies such as 24 GHz and 60 GHz [6], [7], [9]. Silicon integration at these frequencies brings several benefits with it such as minimal incremental cost of devices, and short on-chip interconnects which enable the realization of complex architectures that are tailored for particular mm-wave sensing and communication applications. As expected, a major challenge with such integration is efficient high-power generation in silicon at mm-wave frequencies as the device scaling that makes devices faster also leads to a reduction in breakdown voltages [10]. One possible method of addressing this challenge is to combine output power from several devices through various combining methods [11], [12]. In the case of wireless applications, one of the more efficient and cost-effective ways to achieve this power combining is to perform it in air, i.e, through spatial beamforming methods using multiple antennas. However, in order for this spatial power combining to be flexible enough for radar and communication applications, the beam needs to be steerable in space.

Phased arrays are a special class of multiple antenna systems that provide a well-known solution to the requirement of electronic beam steering. In addition to providing beamforming and beam steering capabilities, phased-arrays provide higher effective isotropic radiated power (EIRP) in the transmitter and lower noise figure in the receiver [7], [13]. While phased arrays increase transmit EIRP and improve system SNR, they present a new challenge, namely, the need for integrated electronic phase shifting to achieve coherent signal combining in the desired direction.

The above-mentioned benefits of phased arrays have led to increasing interest in integrated phase shifters [14]–[16], as well as demonstrations of integrated phased-array transmitters and receivers [8], [17], [18]. Though LO-path phase-shifting was presented as a viable candidate for integrated phased-arrays in [8], a direct attempt to extend the centralized architecture employed in [8] to a system that integrates an entire transceiver at a higher frequency becomes extremely difficult due to the need for extensive buffering and large silicon area. Therefore, in this work, we utilize a local LO-path phase-shifting scheme to realize the first fully integrated 77-GHz phased-array transceiver implemented in a SiGe process. In this paper, we focus on the transmitter and the phase-shift architecture while the receiver and the on-chip dipole antennas are discussed in greater depth in the companion paper [33]. To the authors' best knowledge, the complete integration of four transmit and receive elements, along with the frequency generation and phase-shifting circuitry, in this transceiver represents the highest levels of silicon integration achieved at mm-wave frequencies [19], [20], [33].

In the following sections, the design and architecture of the transmitter and LO-path phase-shifting sections of the phased-array transceiver will be discussed in greater detail. Section II provides a brief overview of the spectrum around 77 GHz. Section III focuses on the transmitter and the local LO-path phase-shifting architecture, while the circuits in the signal and LO-path are discussed in Section IV. The measurement results are presented in Section V.

Manuscript received May 1, 2006; revised September 1, 2006.

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Digital Object Identifier 10.1109/JSSC.2006.884817

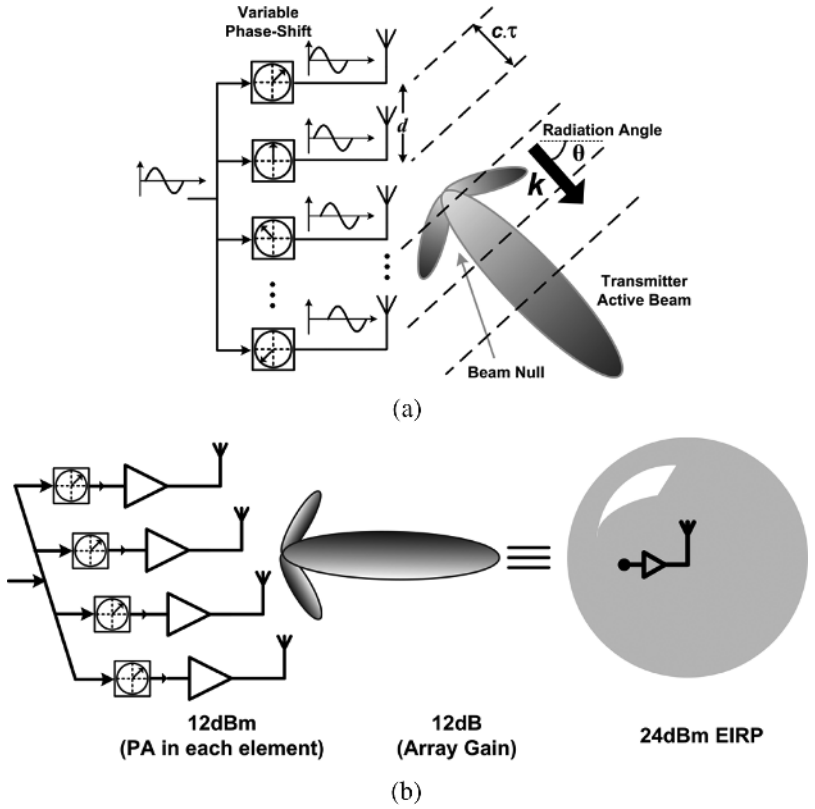

Fig. 1. Phased-array transmitter. (a) Operating principle of phased-array transmitter. (b) Improvement in EIRP in phased-array transmitter.

II. The Spectrum at 77 GHz

Collision-avoidance radar systems on vehicles are expected to play a major role in reducing accidents and improving automotive safety. The uses of mm-wave sensors are, however, not restricted to automobiles as there are numerous military and commercial sensing applications that require high-frequency sensors [22].

In the case of automotive radar, efforts are underway to utilize these systems for blindspot detection, adaptive cruise control and collision-warning applications [21]. Though vehicular radar systems in the near future are permitted to operate at 24 GHz, these systems will have to transition to 77 GHz due to concern over frequency bands near 24 GHz that are used for sensitive measurements in astronomy [23]–[25]. While adaptive cruise control (ACC) systems require beams to have 3° beamwidths and a scanning range of 8° in the azimuth, larger scanning ranges would be necessary for collision-avoidance applications [26], [27]. A beamwidth of 3° in the azimuth and elevation planes calls for 36-dBi system directivity. Splitting this directivity evenly between the transmitter and receiver leads to a 18-dBi directivity requirement in the transmitter. A single transmitter with a highly directive antenna limits the scanning range whereas in a phased array the required directivity can be partitioned between the array gain and the directivity of the antennas, thereby permitting beam scanning. For a phased-array with n elements, the directivity is $10\log(n)$ dBi, which translates to 12-dBi directivity for a 16-element array. Such a phased array, coupled with planar antennas with directivity 6 dB, leads to sufficient system directivity. If each element in this system can transmit 12 dBm, the EIRP for the entire array with the antenna is 42 dBm. The EIRP can be further increased by increasing the antenna gain in the elevation plane, as the gain in the elevation plane does not affect the scanning in the azimuthal plane.

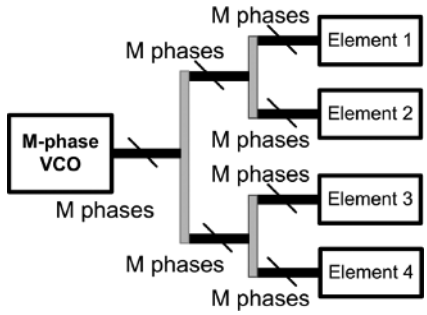

Fig. 2. Centralized LO-path phase-shifting architecture.

III. System Architecture

This section provides a brief introduction to phased-array transmitters followed by a description of the transmitter and the local LO-path phase-shifting architecture employed in the transceiver.

A. Phased-Array Transmitter Overview

A phased array is a multiple-antenna system in which beamforming is achieved by varying the relative phase shifts in each element. As shown in Fig. 1(a), for a certain phase shift setting in each element of an n-element phased-array transmitter, the

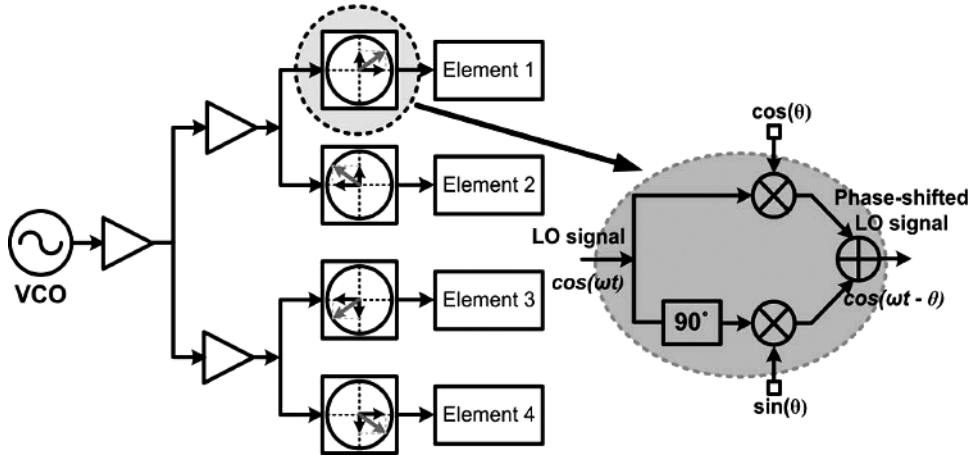

Fig. 3. Local LO-path phase-shifting architecture.

signals from all elements add up coherently in one direction and incoherently in other directions leading to formation of a beam. Electronic phase-shifting enables beam steering, eliminating the need for any moving mechanical components. An important advantage arising from the coherent combining of signals in an n-element phased-array transmitter is the improvement in EIRP by $20\log(n)$ dB, as shown in the example in Fig. 1(b).

B. Local LO-Path Phase Shifting Architecture

The phase-shifting capability required in each element of a phased-array transmitter can be implemented in myriad ways. The tradeoffs of implementing the phase-shift at different points in the transmit or receive chain have been discussed in [8]. Phase-shifting in the LO-path is considered advantageous since the circuits in the LO-path operate in saturation and therefore it is relatively simple to ensure that the gain of each element does not vary with the phase shift setting. Additionally, the requirements on phase-shifter linearity, noise figure and bandwidth are substantially reduced when LO-path phase shifting is adopted.

Earlier integrated phased-array receiver and transmitter designs [7], [17] introduced a centralized LO-path phase-shifting scheme in which an m-phase voltage-controlled oscillator (VCO) generates multiple phases of the LO, as shown in Fig. 2. These multiple phases are then distributed to the phase selector in each element which selects the appropriate phase of the LO for the desired beam direction. One limitation with this approach stems from the fact that the phase resolution is limited by the number of phases generated by the VCO. Another limitation, more important at mm-wave frequencies, arises from the necessity to distribute all the LO phases to each element since the distribution of a large number of LO phases precludes a power-matched, buffered LO-phase distribution network with transmission-line (t-line) interconnects and matched LO buffers. As a result, the centralized scheme is unsuitable for an array operating at high frequencies and/or having a large number of elements as such arrays would require a larger distribution network with intermediate buffering.

The above-mentioned limitations of the centralized phase-shifting scheme dictated the move to the *local* LO-path phase-shifting architecture adopted in this system. In this architecture (shown in Fig. 3), the output of a single-phase VCO is distributed to the phase rotator in each element through a buffered binary-tree distribution network. The use of power-matched buffers ensures an LO signal with sufficient amplitude at the phase rotator input. The phase rotator in each element generates the LO quadrature phase locally and then interpolates between the in-phase (I) and quadrature-phase (Q) LO signals to generate the desired phase shift in each element. From the detailed description of the phase rotator circuitry, presented in Section IV, it can be seen the phase shift resolution in this approach depends primarily upon the resolution of interpolator weights which can be generated with high-resolution by DACs. This increased resolution can also be used to improve phase matching between different elements through calibration procedures.

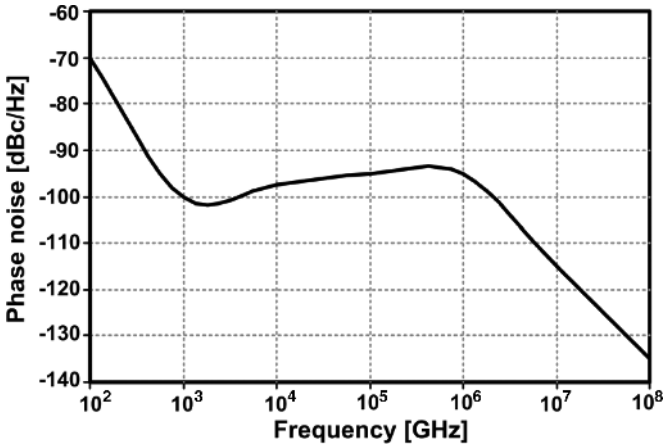

Fig. 4. Simulated closed-loop phase noise of 50-GHz frequency synthesizer.

In addition to the resolution of the weights, the resolution of an LO-path phase-shifting architecture is also limited by the phase noise of the LO signal as the phase setting in each element is affected by LO phase noise which translates to jitter in the beam direction. An estimate of this degradation can be obtained from a sample 50-GHz synthesizer phase noise plot shown in Fig. 4. The output of the phase rotator is a weighted combination of the LO signal and a delayed version of the LO signal.

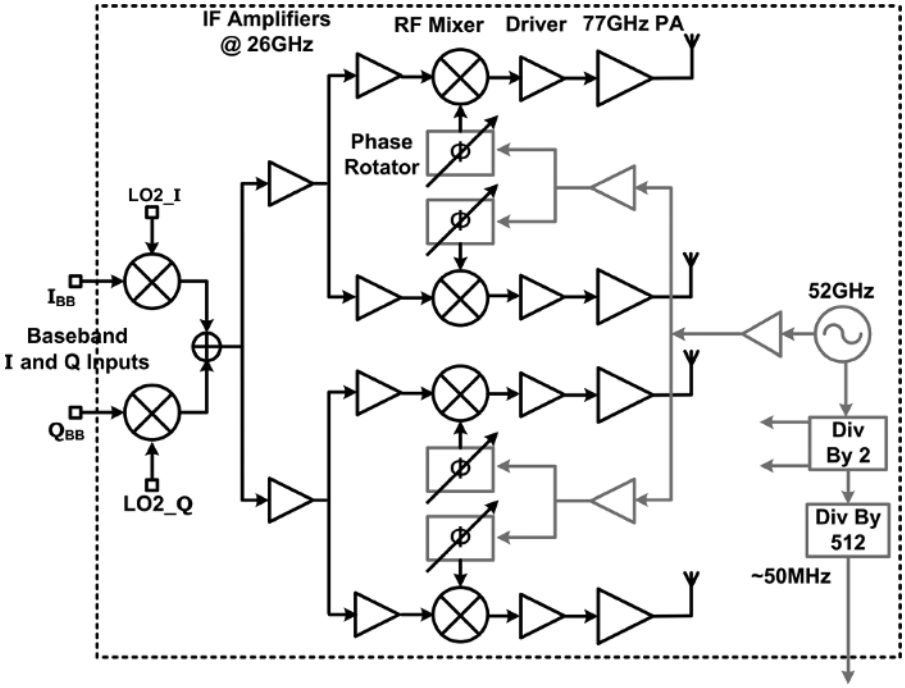

Fig. 5. 77-GHz phased-array transmitter architecture.

Ignoring the effect on phase noise of the correlation induced by this weighted combination, the rms jitter in the phase setting is given in radians by

$$\left\langle \theta^2(t) \right\rangle = 2 \int_{fmin}^{\infty} 10^{L(f)/10} df \tag{1}$$

where L(f) is the phase noise of the closed loop synthesizer in dBc/Hz. For the sample synthesizer plot in Fig. 4, with $fmin = 100$ Hz, the rms jitter in the phase setting in each element is 2.1°.

C. Transmitter Architecture

The 77-GHz phased-array transmitter has four elements and is a part of a fully integrated 77-GHz four-element phased-array transceiver. The LO frequency generation circuits are shared between the receiver (RX) and the transmitter (TX). It is important to note that each transmit and receive element includes an independent phase rotator that applies the desired phase of the LO to the upconversion or downconversion mixer in that element.

The architecture of the transmitter is shown in Fig. 5. The transmitter utilizes a two-step upconversion scheme with an IF frequency of 26 GHz. The on-chip VCO generates the 52-GHz LO signal necessary for the second upconversion in the TX (and for the first downconversion in RX) while the quadrature 26-GHz signal required for the first upconversion (and second downconversion in RX) is provided by a quadrature injection-locked divide-by-two following the VCO.

In the transmit signal path, the baseband signals are upconverted to 26 GHz by a pair of quadrature upconversion mixers. The signal distribution to all the elements is done at IF through a network of distribution amplifiers. The RF mixer in each element upconverts the 26-GHz input signal to 77 GHz, providing the input for a driver that feeds on-chip 77-GHz power amplifiers. The adopted frequency plan leads to the undesired product of the second upconversion falling at 26 GHz while the RF is at 77 GHz. The tuned mixer, driver, and power amplifier (PA) stages provide sufficient attenuation at 26 GHz, therefore the second upconversion does not employ quadrature upconversion.

In the LO-path, the output of the differential, crosscoupled 52-GHz VCO is distributed to the phase rotators in each element through a symmetric network of distribution buffers that ensures that the phase of the LO signal is the same at the input of the phase rotator in all transmit elements. A cascade of divide-by-two frequency divider blocks following the VCO generate the 50-MHz signal that is used by an off-chip PFD to lock the VCO.

IV. Circuits in Transmit and LO Paths

A. IF Stage

The baseband to IF upconversion is achieved using Gilbert-type quadrature upconversion mixers with a shorted t-line as load (Fig. 6). As the mixers drive a pair of IF distribution buffers that are input-matched to 100-Ω differential, the output impedance of the mixers is designed to be 50-Ω differential to provide maximum power into the distribution network. The mixers and the buffers draw 46 mA from a 2.5-V supply.

The multiple elements present on the same die in an integrated phased array result in on-chip interconnects that are up to 1.5 mm in length. At the LO frequency of 52 GHz, this represents 0.52λ. Therefore, interconnect modelling is critical, and adoption of t-line based interconnects that are easily and reliably modeled dramatically simplifies the design effort.The t-line structure adopted in this system is shown in Fig. 6. The presence of the ground shield improves the isolation between adjacent

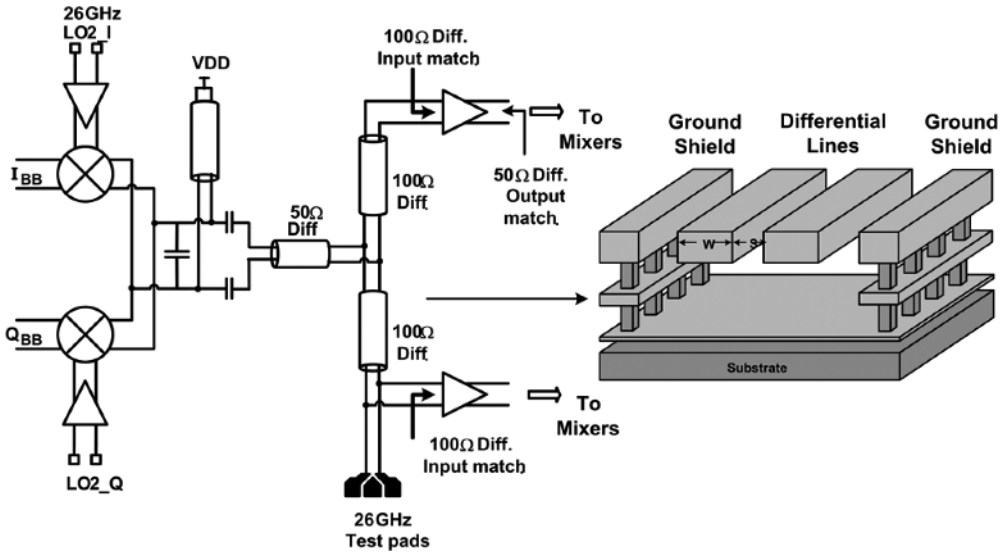

Fig. 6. IF stage.

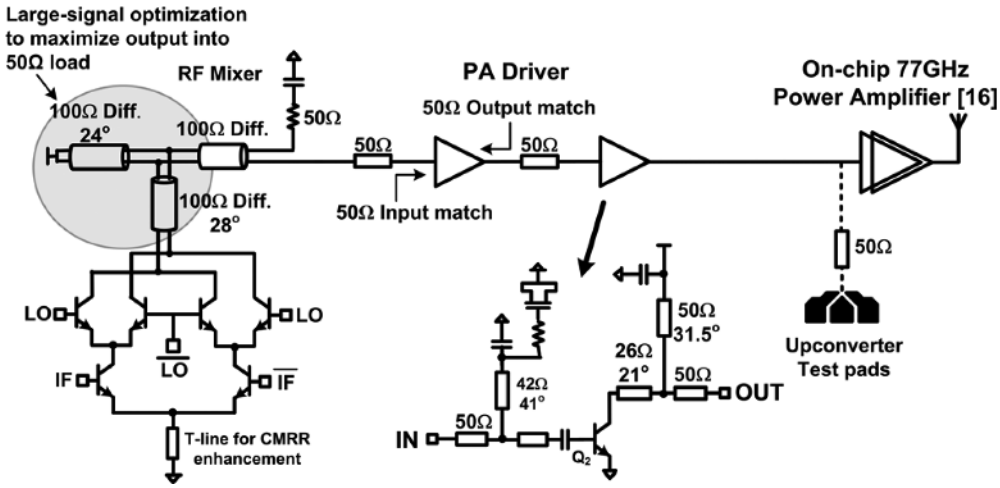

Fig. 7. RF stage.

t-lines by 20 dB, which is important given the number of signal t-lines in the integrated transceiver.

While t-lines simplify modelling, the design is still heavily floorplan dependent as the load impedances are a strong function of interconnect length. This dependency can be eliminated by conjugate-matching each circuit block at the input and output to the t-line interconnects, thereby ensuring that the load impedances are independent of the floorplanning. However, it must be noted that this separation of design and floorplanning is achieved at the cost of bandwidth. For a simple shunt-series t-line matching network, the bandwidth depends upon the transformation ratio which can be high, as the range of impedances achievable with on-chip t-lines for reasonable layout parameters and acceptable loss is limited to 65 Ω. While this reduction in bandwidth can be desirable for some applications, it can pose a problems for broadband applications. This challenge can be overcome by reducing the quality factor (Q) of the tuned loads or by using higher order matching networks [28]. In the transmitter, the Q of the tuned loads was chosen such that the system had a bandwidth of 2.5 GHz. Furthermore, the characteristic impedance of t-line interconnects was generally chosen to be 50 Ω to allow for probe-based measurements at internal test points.

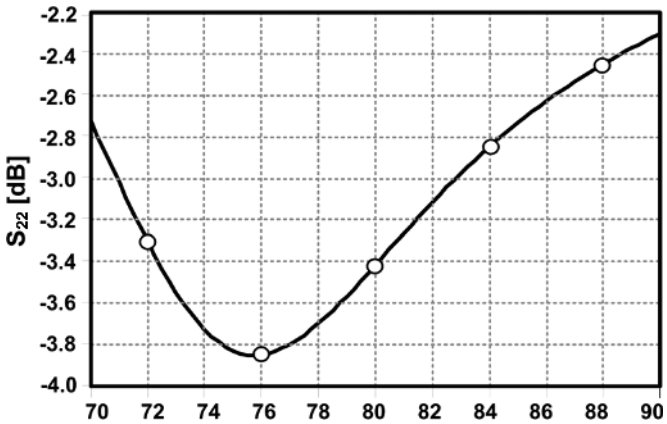

Fig. 8. Simulated power-match at RF mixer output under small-signal conditions.

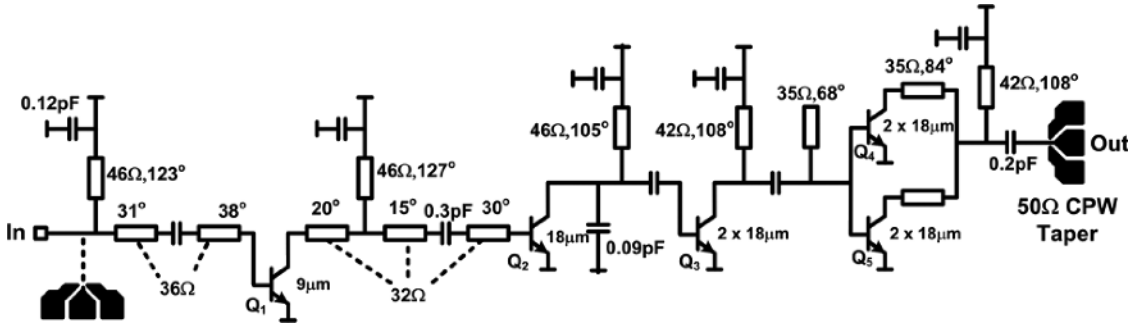

Fig. 9. On-chip 77-GHz power amplifier.

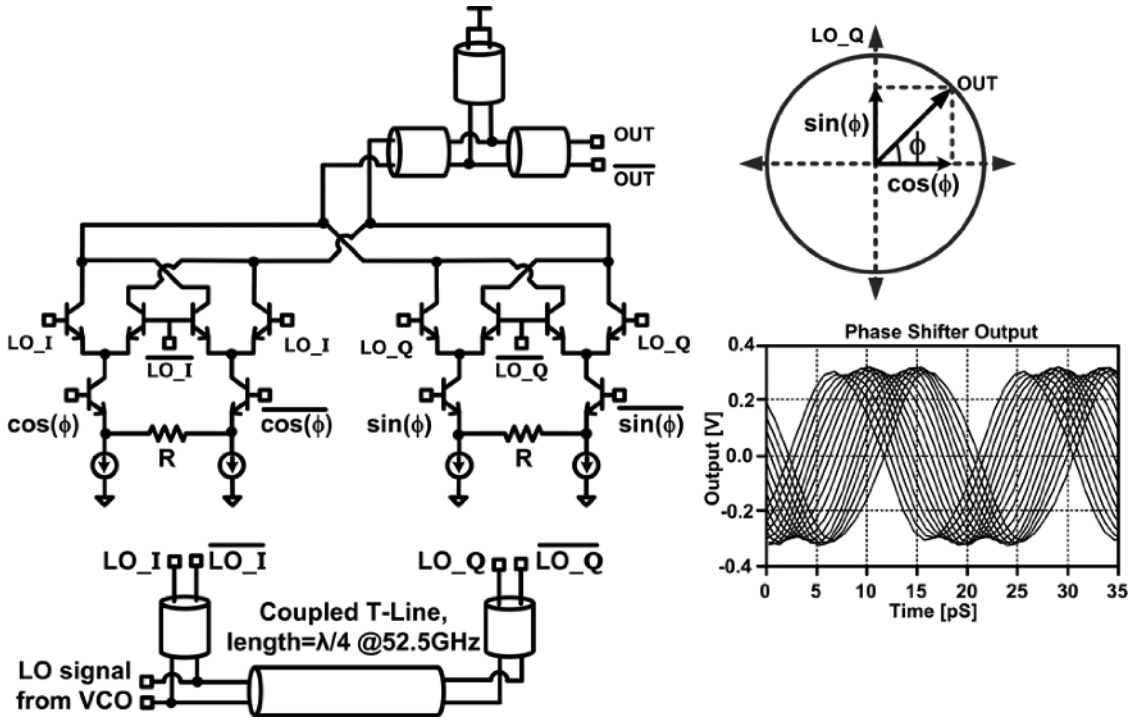

Fig. 10. 52-GHz phase rotator.

B. RF Stage

The 26-GHz IF signal is upconverted to 77 GHz by a Gilbert-type upconversion mixer in each element (Fig. 7). All the circuits in the transmitter up to and including the mixer are differential whereas the PA driver and the PA are single-ended in order to facilitate measurements. While an on-chip mm-wave balun can be implemented, similar to [30], area limitations did not permit that option. Therefore, one of the differential outputs of the mixer is terminated to 50 Ω through a capacitor. The other output of the mixer is fed to the PA driver that is input matched to 50 Ω. A large LO amplitude is desirable at the LO port to improve conversion gain and provide high output power. Since the mixer sees large signals at both its LO and output ports, the mixer output should not be power-matched under small-signal conditions. Therefore, the lengths of the stub and series t-lines used in the mixer output-matching network are optimized, using a methodology similar to the load-pull methodology used in PA design, to maximize the output power into a 50 Ω load under large signal conditions. Fig. 8 plots the simulated[1] small-signal output-match for the optimized network. The poor power-match at 77 GHz at the mixer output with the optimized load shows that small-signal matching is not a good metric to maximize output power.

C. Power Amplifier

The four transmitter outputs are generated by on-chip PAs in each element [27]. As shown in Fig. 9, the PA is a four-stage design with the transistor size doubled in each stage to ensure that the output-stage saturates first provided each stage has at least 3-dB gain. While the first three stages of each PA are designed for maximum gain, the output stage is designed for maximum efficiency. The outputs from two transistors are combined at the output stage, and the combined output is matched to 50 Ω with a t-line network. Each of the PAs is connected to an on-chip dipole antenna that can be trimmed out using a laser for direct

[1]For the small-signal simulations, the LO transistors in the mixer are assumed to be completely switched.

electrical measurements via pads. The design and measurement of the PA has been discussed in depth in [27].

D. 52-GHz Phase Rotator

The input from the LO distribution network to the phase rotator is divided into two paths as shown in Fig. 10. An extra $\lambda/4$ t-line in one of the paths generates the quadrature LO signal locally which are then provided to an analog phase rotator. The emitter-degenerated differential pairs at the bottom in each half of the phase rotator control the relative weights of the I and Q signals that are combined at the output. The emitter degeneration increases the voltage range of the weights in the rotator, thereby relaxing the DAC requirements. As described in the previous section, this local phase-generation scheme minimizes the number of t-lines carrying the 52-GHz signal over long distances and enables the use of well-defined t-lines and power matched LO-path buffers without excessive area and power penalties. Unlike the multi-phase distribution approach in [8], [17], the local phase-shifting scheme presented here does not suffer from additional coupling-induced phase errors and signal loss in the distribution path. As shown in Fig. 10, the simulated amplitude variation in the phase rotator for different phase shift settings is around 1.5 dB. This variation is further reduced in the entire system as the mixer is not very sensitive to the LO amplitude provided it is large enough.

The output of the phase-rotator, V_{out}, can be expressed as

$$V_{\text{out}}(t) = k_1.A\cos(\omega_0 t) + k_2.A\sin(\omega_0 t) = A\sin(\omega_0 t + \theta) \tag{2}$$

where $\tan\theta = k_1/k_2$.

It is evident that the resolution of weight voltages k_1 and k_2 does not translate to the same resolution of phase-shifts due to the nonlinear nature of the cosine and sine functions. In the absence of this nonlinearity, if k_1 and k_2 are generated with n-bit resolution, a phase-shift resolution of $n+1$ bits, or $360/2^{n+1}$ degrees can be expected. Therefore, ideally phase-shifts from 0° to 360° can be generated with steps of $360/2^{n+1}$ degrees. However, because of the nonlinearity, if k_1 and k_2 are generated with uniform steps, there is an error in the phase-shift for some settings as the phase-shifts are not generated with uniform steps. Fig. 11(a) plots the rms and maximum error in the phase-shift against the number of bits in the DAC that generates the weight voltages. It can be seen that that for the same number of bits in the DAC, the error in the phase-shift can be reduced if larger amplitude variations are acceptable.

E. 52-GHz Voltage-Controlled Oscillator

The 52-GHz VCO, the schematic of which is shown in Fig. 12, employs a differential cross-coupled design. A shorted differential t-line that provides approximately 95 pH @ 52 GHz is used as the inductor in the tank. The proximity of the return-path in the chosen t-line reduces the inductance-per-unit-length and increases current-crowding which leads to an inductor Q of 24 @ 53 GHz. However, the well-defined path for return current ensures accurate modeling of the t-line which, when accompanied by careful extraction of interconnect parasitics, ensures that the VCO operates at the desired frequency of 52.5 GHz with a tuning range of 10%. The

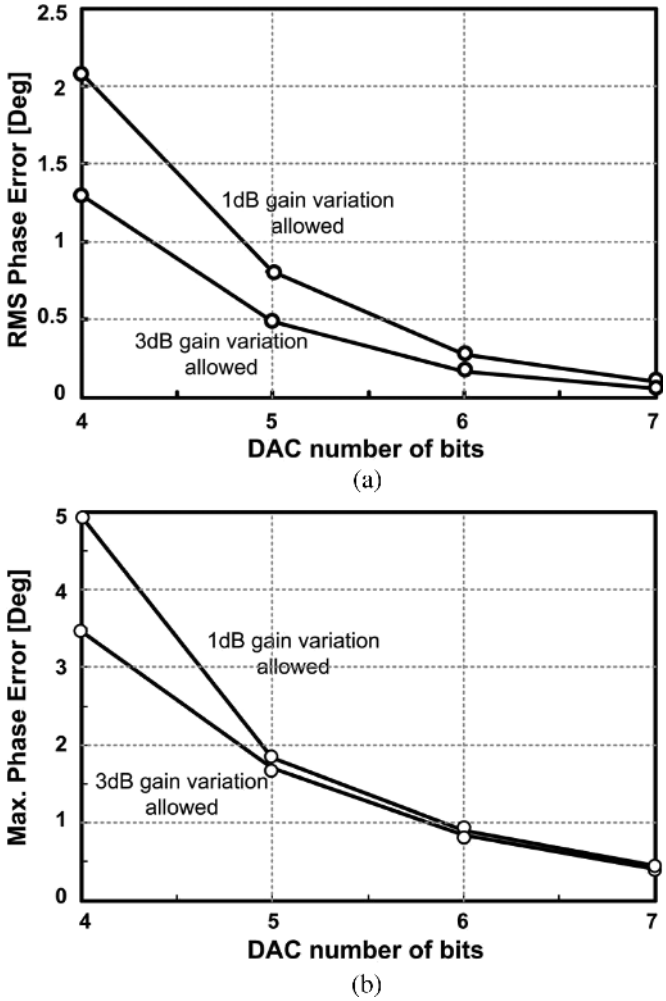

Fig. 11. Phase-shift error versus DAC resolution. (a) RMS phase-shift error. (b) Maximum phase-shift error.

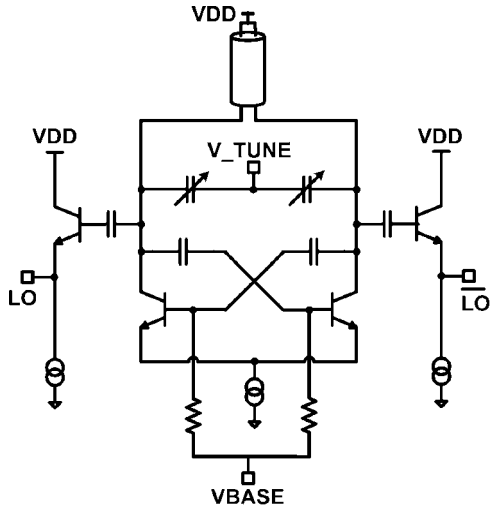

Fig. 12. 52-GHz voltage-controlled oscillator.

VCO tuning is achieved through varactors that have a simulated Q of 40 at 52.5 GHz. The output of the VCO can be measured by probing test pads that are placed after the first stage of the two-stage VCO buffer that follows the VCO.

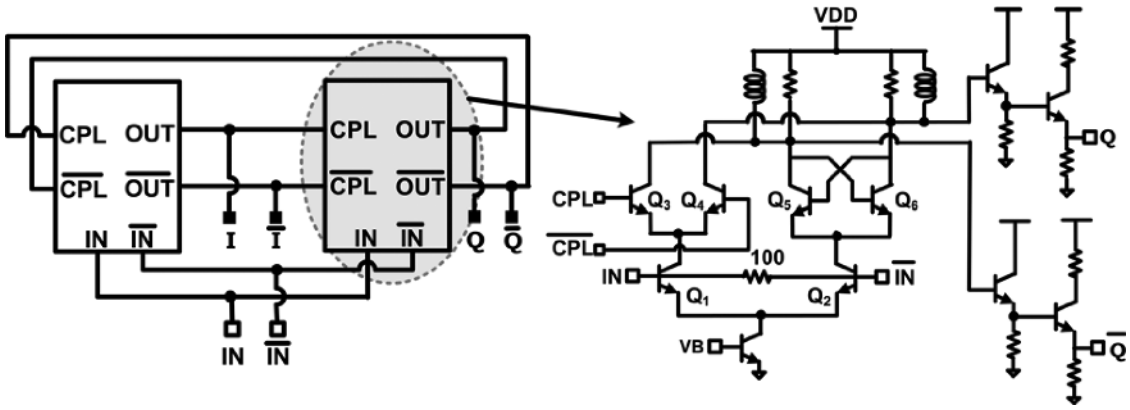

Fig. 13. 52-GHz quadrature injection-locked frequency divider.

F. 52-GHz Injection-Locked Divider

The 26-GHz LO signal necessary in the heterodyne transceiver is generated by a divide-by-two that follows the 52-GHz VCO. Although a digital divider with ECL-based D-flip flops operates over a broad frequency range and generates quadrature-phases, the digital divider power consumption increases at high frequencies, making it unsuitable for low-power designs. In order to reduce the power consumption, an injection-locked frequency divider was used for the the first divide-by-two in this system [34]. While an injection-locked frequency divider consumes much lower power, it operates over a narrow frequency range and therefore the parasitics have to be carefully modelled to ensure operation at the frequencies of interest. Fig. 13 shows the schematic of the injection-locked divider with the VCO input being provided at the tail current. The quadrature phases of the divided signal are generated by the cross-coupling of two-injection locked dividers as shown in Fig. 13. The divider core draws 3.1 mA from a 2.5-V supply.

In addition to the generation of quadrature phases, the cross-coupling of the two dividers increases the sensitivity of the injection-locked divider as will be shown in the following equations. Assuming that VCO output is a single tone, the input to the differential pair Q_1 and Q_2 in the frequency divider can be represented by

$$V_i(t) = V\cos\left(\omega_i(t) + \psi\right) \tag{3}$$

and the differential in-phase output $V_{oI}(t)$ and quadrature output $V_{oQ}(t)$ can be represented by

$$V_{oI}(t) = V_0\cos(\omega_0 t) \tag{4}$$

$$V_{oQ}(t) = V_0\sin(\omega_0 t). \tag{5}$$

The AC current in the collector of Q3, $i_{Q3}(t)$, is given by

$$\begin{aligned} i_{Q3}(t) &= f\left(V_i(t), V_{oI}(t)\right) \\ &= \sum_{m=0}^{\infty}\sum_{n=0}^{\infty} K_{m,n}\cos(m\omega_i t + m\psi)\cos(n\omega_0 t) \end{aligned} \tag{6}$$

where $K_{m,n}$ is the intermodulation coefficient of the mth order harmonic of $V_i(t)$ and the nth order harmonic of $V_{oI}(t)$ [31].

Assuming the identical transistors are used for $Q_3 \sim Q_6$, the collector current of Q_5, $i_{Q5}(t)$, is

$$\begin{aligned} i_{Q5}(t) &= f\left(-V_i(t), V_{oQ}(t)\right) \\ &= \sum_{m=0}^{\infty}\sum_{n=0}^{\infty}(-1)^m K_{m,n} \\ &\qquad \times \cos(m\omega_i t + m\psi)\sin(n\omega_0 t) \end{aligned} \tag{7}$$

For the divide-by-two, $\omega_i = 2\omega_0$. Also, due to the tuned load, only the intermodulation components around ω_0 matter. Ignoring the intermod components beyond fourth order in (6) and (7)

$$\begin{aligned} i_{Q3}(t) &= K_{0,1}\cos(\omega_0 t) + \frac{1}{2}K_{1,1}\cos(\omega_0 t + \psi) \\ &\quad + \frac{1}{2}K_{1,3}\cos(\omega_0 t - \psi) \end{aligned} \tag{8}$$

$$\begin{aligned} i_{Q5}(t) &= K_{0,1}\sin(\omega_0 t) - \frac{1}{2}K_{1,1}\sin(\omega_0 t + \psi) \\ &\quad - \frac{1}{2}K_{1,3}\sin(\omega_0 t - \psi). \end{aligned} \tag{9}$$

From (8) and (9), it can be seen that when i_{Q3} and i_{Q5} are added, the amplitude of each intermod product is increased by $\sqrt{2}$ as the products are in quadrature. Thus, in addition to generating the I and Q phases at the divider output, the quadrature coupling of the dividers increases the locking range of the dividers making them more robust to process variations and modeling errors at high frequencies.

V. Measurements

The four-element transceiver was implemented in a SiGe BiCMOS process that had SiGe Bipolar transistors with an f_t of 200 GHz [29]. The process offered seven metal layers. The top two thick metal layers were 4 μm and 1.25 μm and were used for signal distribution to minimize losses. Fig. 14 shows a die micrograph of the entire transceiver, which occupies 6.8 mm $\times$ 3.8 mm of die area. The transmitter and the LO circuits occupy 17 mm^2. As the transmitter measurements have to be performed at mm-wave frequencies, a waveguide-based measurement setup was utilized for characterizing the transmitter (Fig. 15). In the case of single-element measurements,

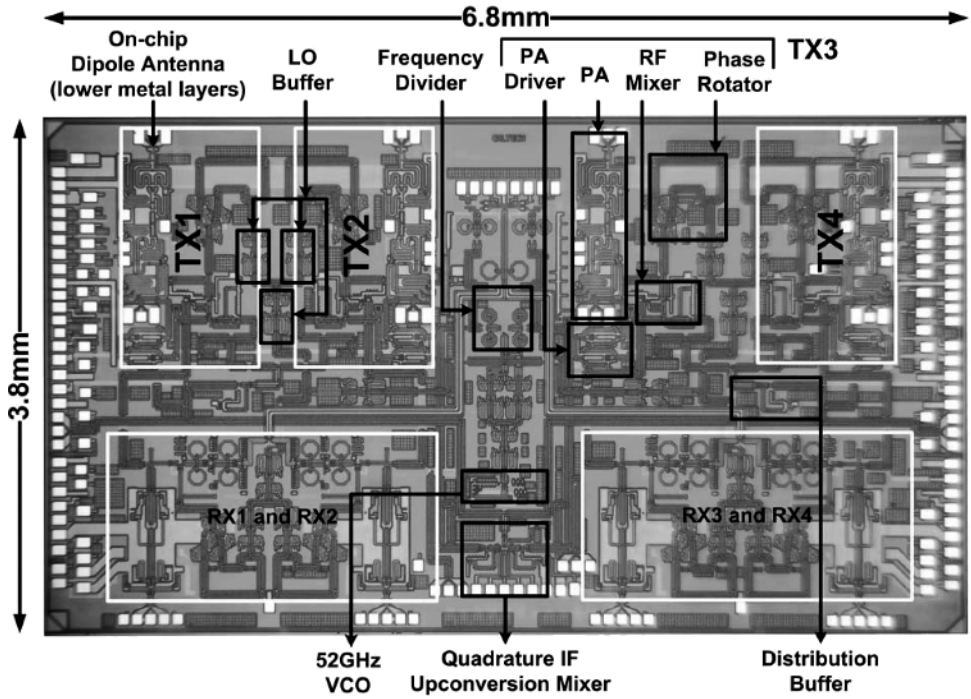

Fig. 14. Die photograph of 77-GHz phased-array transceiver.

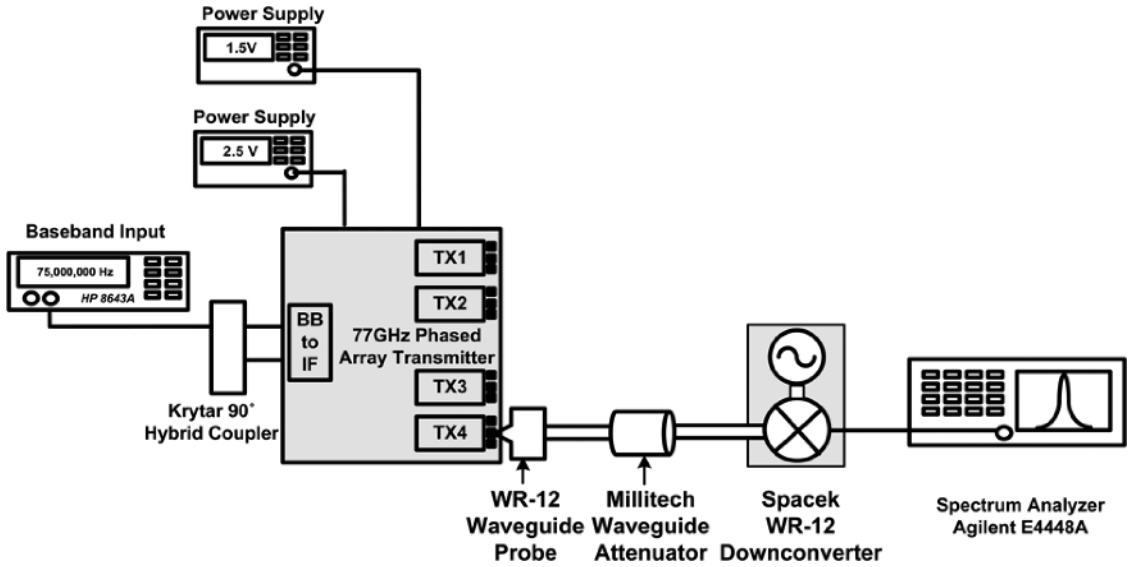

Fig. 15. 77-GHz transmitter measurement setup.

the output of the transmitter is probed using WR-12 probes. The output is then connected to an external downconverter which mixes the 77-GHz output down to 18 GHz, making it possible to view the output on a spectrum analyzer. As mentioned, the chip requires a 1.5-V supply for the PA and the PA driver and a 2.5-V supply for the rest of the circuitry.

The 52-GHz VCO and frequency divider were measured using internal test points. Fig. 16 shows that the VCO can be tuned from 50.35 GHz to 55.49 GHz which is a tuning range of 9.7%. Fig. 16 also shows that the injection-locked divider locks to the VCO input from 51.4 GHz to 54.5 GHz. The VCO phase-noise was measured using a waveguide-based external mixer that downconverted the 52-GHz LO to 8 GHz using an external 60-GHz signal. The VCO measurements show a phase noise of -95 dBc/Hz at 1-MHz offset at 54 GHz (Fig. 17). The divider's input sensitivity, which is the input power necessary for the divider to achieve locking, is plotted in Fig. 18. As can be seen from Fig. 16 and Fig. 18, the VCO tuning range and the divider locking range are sufficient for the applications of interest.

Fig. 19 plots the output power of the transmitter at 77 GHz. Each element in the transmitter generates up to 12.5 dBm with a 1-dB compression point of 10.2 dBm. The transmitter has a bandwidth of 2.5 GHz. Stand-alone measurements on the PA indicate a maximum power of 17.5 dBm with a power-added efficiency (PAE) of 12.8%.

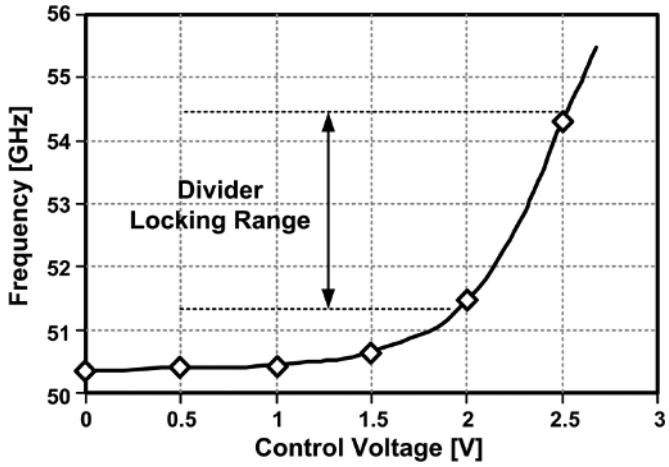

Fig. 16. Measured VCO tuning range.

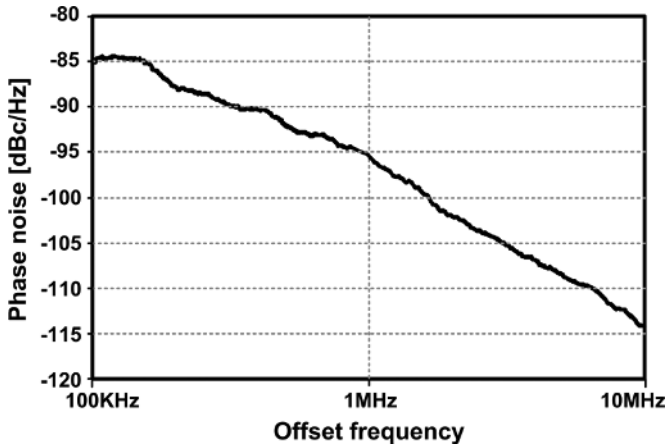

Fig. 17. Stand-alone VCO phase noise @ 54 GHz.

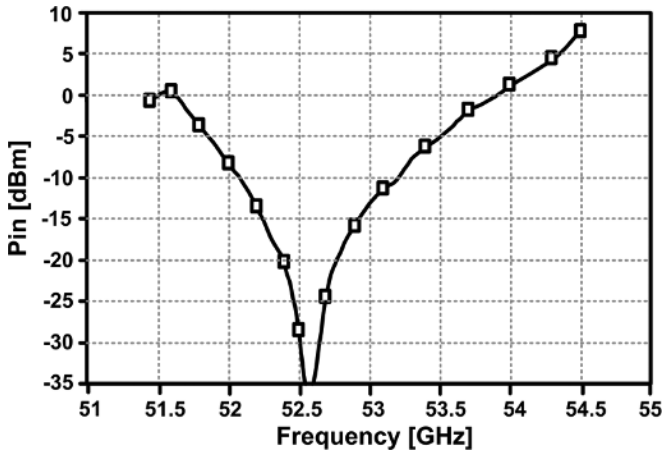

Fig. 18. 52-GHz injection-locked frequency divider sensitivity.

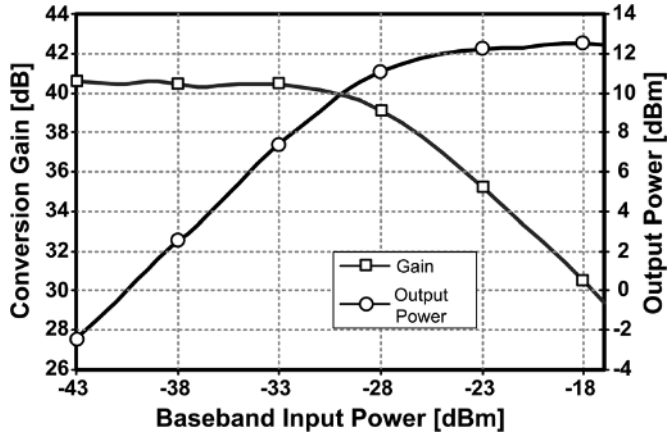

Fig. 19. Single element Tx conversion gain and output power at 77 GHz.

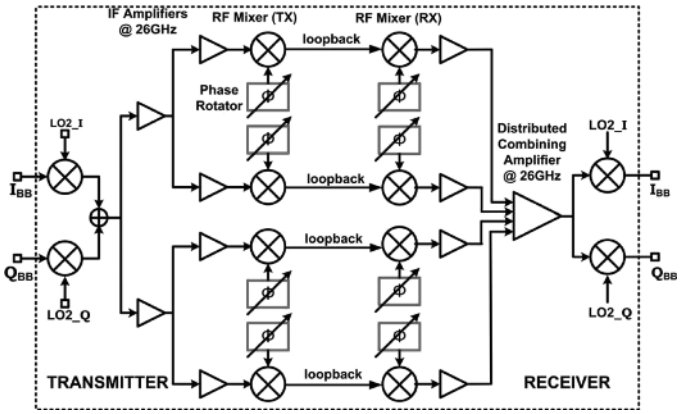

Fig. 20. Internal loopback measurement.

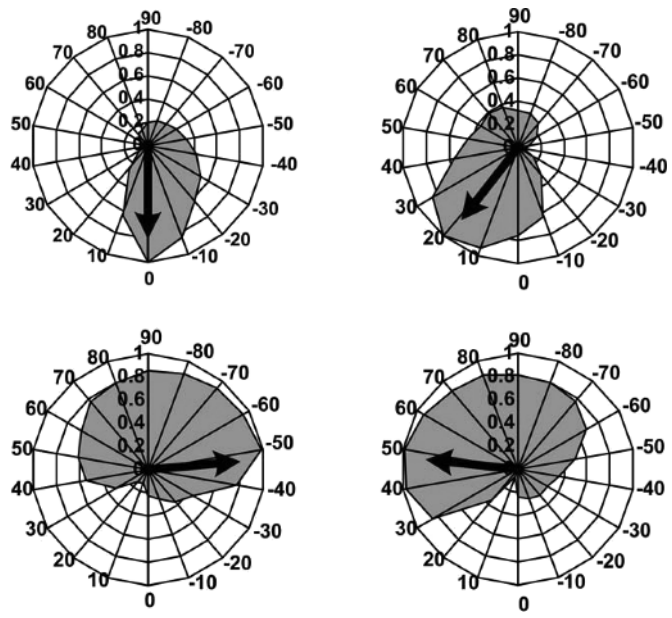

Fig. 21. Loopback array pattern with two Tx and Rx elements active.

The phased-array transmitter is a part of the 77-GHz phased-array transceiver [20], which allows for testing via an internal 77-GHz loopback option that utilizes laser trimming. To implement the loopback option, the output of the RF up-conversion mixer in the transmit element is connected to the input of the RF downconversion mixer in the receive element. During stand-alone receiver and transmitter characterization, the internal loopback connections between the transmit and receive elements are laser trimmed. However, for testing in the loopback mode, the PA in the transmitter element and the LNA in the receiver element are bypassed using laser trimming and

TABLE I
TRANSMITTER PERFORMANCE

Transmitter performance	
Maximum output power	+12.5dBm
4-element EIRP	+24.5dBm
Transmit 3dB-bandwidth	2.5GHz
Gain	40.6dB (single element)
Output referred 1dB compression point	+10.2dBm
Image signal attenuation	> 20dBc (for first upconversion step) > 30dBc (for second upconversion step)
LO leakage power	<-19dBc
Transmitter power consumption	
Signal path @ 77GHz	
PA and PA Driver (@1.5V)	200mA (per element)
RF mixer and buffer (@2.5V)	18mA (per element)
Distribution buffers and baseband mixers (@2.5V)	46mA
Phased array performance	
Peak-to-null ratio (2-element *loopback*)	> 12dB
Beam-steering resolution	Continuous (limited by DAC resolution in practice)
VCO tuning range	50.35GHz to 55.49GHz (9.6%)
Divider locking range	51.4GHz to 54.5GHz (5.9%)
LO-path power consumption	
VCO and buffers (@2.5V)	10mA
Analog divider core (@2.5V)	3.1mA
Divider buffers	28mA
LO path distribution buffers (@2.5V)	12mA (each distribution buffer)
Phase rotators (@2.5V)	14mA (each phase rotator)
Die size	$17mm^2$ (Tx + LO circuits) $25.8mm^2$ (Transceiver)
Device Technology	0.12μm SiGe BiCMOS

the loopback connection between the output of the 77-GHz upconversion mixer in a transmit element and the input of the 77-GHz downconversion mixer in a receive element is preserved as shown in Fig. 20. In order to characterize an array pattern, without using antennas, the outputs of different transmit elements have to be combined with different phase-shifts to emulate signal combining in different directions, as done in [7], [17], and [18]. As mentioned in Section III, the LO-phase in each element of the transceiver can be set independently. Therefore, in the loopback mode, it is possible to measure the transmitter pattern for a particular phase-shift setting by varying the phase-shift settings in the receive elements to emulate signal-combining with different phase-shifts in different directions Thus, the loopback option allows for transmitter and receiver array patterns to be measured using baseband input-output, with no off-chip mm-wave connection. Fig. 21 shows the measured patterns with two transmit-receive pairs active in the loopback mode. The good match between expected and measured beam direction demonstrates the beam-forming capabilities of the transmitter.

Table I summarizes the measured performance of the transmitter.

VI. CONCLUSION

The transmitter and LO-path phase-shifting sections of a fully integrated 77-GHz phased-array transceiver have been presented. The transceiver employs a local LO-path phase-shifting architecture that scales well with an increase in number of on-chip elements. The transmitter with on-chip power amplifiers, achieves 12.5-dBm output power at 77 GHz with a bandwidth of 2.5 GHz. The on-chip VCO tunes from 50.3 GHz and 55.49 GHz and the quadrature injection-locked frequency divider locks to the VCO output from 51.4 GHz to 54.5 GHz. The phased-array achieves 12-dB peak-to-null ratio with two elements active. To the authors' best knowledge, the complete integration of four transmit and receive elements along with the frequency generation and phase-shifting circuitry in this transceiver represent the highest levels of silicon integration achieved at mm-wave frequencies.

ACKNOWLEDGMENT

The authors thank the DARPA trusted foundry program and IBM for chip fabrication, and are grateful to Prof. D. Rutledge, Dr. S. Weinreb, Dr. B. Analui, Prof. Hashemi, and, T. Yu for

their valuable assistance and support. The technical support for CAD tools from Agilent Technologies and Zeland Software Inc. is also appreciated.

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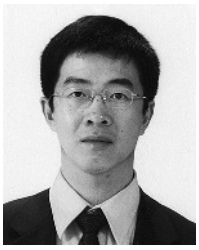

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