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12.5 A 9.4-ENOB 1V 3.8μW 100kS/s SAR ADC with Time-Domain Comparator

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The signal bandwidth used in portable or autonomous sensor systems is often lower than 50kHz with ADC requiring about 8 to 10 bits resolution, but the consumed power must be very low: few μW or a FOM = $P/(2^{ENoB}f_{sampl})$ lower than 0.1pJ/conversion-step. To achieve this target, the successive approximation algorithm is a convenient solution, because it requires only a comparator, a capacitive array and digital logic [1, 2]. In circuits with transistors operated in the sub-threshold region, the ratio between power consumption and unity-gain frequency is almost constant until the leakage current is a negligible fraction of the total. Therefore, it is possible to maintain a low FOM in a reasonably large range of conversion frequencies. However, one additional bit of resolution, when approaching the kT/C noise limit, leads to 4× larger capacitances, with an equivalent increase of power consumption. Therefore, maintaining very-low FOM with increasing ENOB is quite challenging and definitely not straightforward.

This SAR-ADC converter achieves 56fJ/conversion-step FOM with 58dB SNDR. It uses a comparator, named time-domain comparator, that instead of operating in the voltage domain, transforms the input and the reference voltages into pulses and compares their duration. The comparator operates with less than 1μA at 1V supply and provides 1.4M conversions per second with 0.2mV sensitivity. The 12b SAR architecture, shown in Fig. 12.5.1, uses a capacitive split-array consisting of a 6b main array, a 6b sub-array and a unity coupling capacitor. The SAR logic is optimized for minimum power consumption. The conversion requires 14 clock periods of the main clock: the first for the input sampling, 12 periods are for the successive approximation cycles and the last one for end of conversion and data transfer.

Figure 12.5.2 shows the circuit schematic of the time-domain comparator. It is the combination of 2 voltage-to-time converters and a logic circuit. When the signal Φ_C is low, transistors M_1 and M_2 charge the nominally equal capacitors C_1 and C_2 to V_{DD}, while nodes A and B are discharged to cancel out any memory of the previous conversion. When Φ_C rises, transistors M_5 and M_6 become constant current generators, with $I_{M5}=V_1/R_D$ and $I_{M6}=V_2/R_D$, respectively, and discharge capacitors C_1 and C_2 at a constant rate. When the voltages across C_1 and C_2 cross the threshold voltage of M_3 and M_4, the following stages and the chain of inverters switch, producing two pulses with durations T_1 and T_2. The flip-flop reveals the pulse that ends first and provides the comparator output. A possible mismatch between the two circuits causes an input-referred offset.

The kT/C noise, the latch time margin ΔT (the minimum delay between set and clock to ensure a correct latching) and the input-referred noise of M_3 (or M_4) determine the accuracy of the comparator. For the latter, the used technology requires ΔT=130ps, which corresponds to a difference between V_B and V_{in} equal to:

$$\Delta V_{in} = \frac{\Delta T \cdot V_2^2}{R_D C_1 \cdot \Delta V_{out}} \quad (1)$$

where ΔV_{out} is the voltage drop across the capacitor. In the proposed circuit R_DC_1=0.1μs, ΔV_{out}=0.4V and V_2=0.15V. Therefore, ΔV_{in}=73μV. The charging and discharging of capacitances cause the noise voltages $\sqrt{2kT/C_1}$ and $\sqrt{2kT/C_2}$. Considering C_1=C_2=0.8pF, the above two terms are equal to 101μV. Moreover, the equivalent noise generator of M_3, $V_{n,3}$, is referred to the input multiplied by $\Delta V_{out}/V_2 \cdot V_{n,3}$ is estimated to be 150μV. Summing up, all the quadratic combination of the 3 contributions on the 2 channels gives our accuracy that is equal to 194μV. Moreover, since R_D is 125kΩ, the discharge current in the reference branch is 1.2μA, which flows with 50% duty cycle.

The time required to discharge 0.8pF by 0.4V with a 1.2μA constant current is 0.267μs. Since T_2 must be less than half of the clock period, the maximum usable clock is 1.87MHz. However, to have a margin to possible errors, this design uses f_{CK}=1.4MHz.

The power consumed to charge and discharge C_1 depends on the successive-approximation sequence at the gate of M_5. If that voltage is much higher than V_B, then C_1 is fully discharged; if the gate of M_5 is much lower than V_B, the capacitance C_1 remains charged to V_{DD}. Therefore, the consumed energy is $C_1V_{DD}^2$ or zero. Assuming that the ones equal in average to the zeros, the energy per conversion is $NC_1V_{DD}^2/2$. With N=12, V_{DD}=1V and f_s=100kS/s, the current draw is 0.48μA.

The binary-weighted split-capacitive arrays used in the architecture (Fig. 12.5.3) are 2 equal sets of binary-weighted elements of 120fF each. Notice that the LSB array does not include the unity capacitance normally connected to V_{REF-} and counts the same number of elements of the MSB array. Moreover, the value of the scaling capacitance between the two arrays is one instead of being fractional [3]. As a result the DAC full scale is $V_{ref}=(V_{REF+}-V_{REF-})$ instead of $V_{ref}(2^N-1)/2^N$. It can be verified that the error is equally distributed between the quantization intervals of the DAC and, instead of causing INL, the error leads to a 1-LSB gain error that can be easily corrected. Complementary n-p pairs with W/L of 1/0.18μm and 2/0.18μm, respectively, and dummy transistors with half width make the switch used for each unity capacitance. The switching array and the charging and discharging of capacitor, with 1V supply and 1.4MHz clock, requires a power of ~0.5μW.

The SAR including the clock generator uses 870 equivalent gates and consumes 1.4μW at 1.4MHz clock and V_{DD}=1V. Therefore, summing up the contributions of comparator, switched array and logic, the estimated power consumption at V_{DD}=1V is about 3μW.

The ADC-SAR is fabricated in a 0.18μm 2P5M CMOS process. Experimental measurements show that the circuit works with a 0.8V to 1.8V supply, V_{DD}, and reference voltages at $0.1V_{DD}$ and $0.9V_{DD}$. The power consumption is 3.8μW at 1V and 11.5μW at 1.8V. The increasing supply voltage improves the SNDR (at V_{DD}=1.8V is 4.8dB more), but the FOM worsens. The FoM, is 56fJ/conversion-step, at V_{DD}=1V. Figure 12.5.4 shows the low-frequency DNL and INL for 10b output obtained by the histogram of 65536 points (V_{DD}=1V). The 3.2mV mismatch in the comparator is corrected by an external trimming of V_B (with V_{bias} at 0.54V). Figure 12.5.5 shows the FFT of the output with $0dB_{FS}$ sine waves at 2.8kHz and 43.8kHz. The main clock is 1.4MHz (100kS/s). The single ended configuration is the source of the second-harmonic distortion that dominates the SFDR: -71.8dB at low frequency and near the Nyquist frequency equal to -64.2dB, as shown in Fig. 12.5.6. The SNDR at Nyquist drops by 1.7dB with a loss of 0.3b. Higher distortion at higher frequency is due to a relatively high non-linear on-resistance of the switches connecting the capacitive arrays to V_{bias} (Fig. 12.5.3). To avoid interferences, a shield of metal 5 almost completely covers the active area. The chip micrograph with annotation and layout on the background is shown in Fig. 12.5.7. The core area is 0.24mm² and the entire die is 0.7mm².

Acknowledgment:
The authors wish to thank National Semiconductor for chip fabrication.

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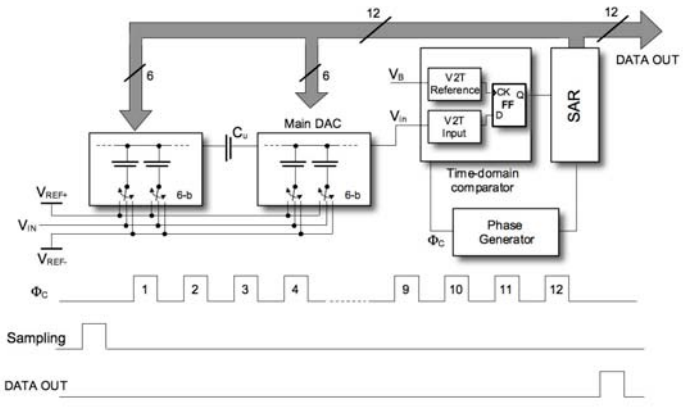

Figure 12.5.1: SAR-ADC architecture.

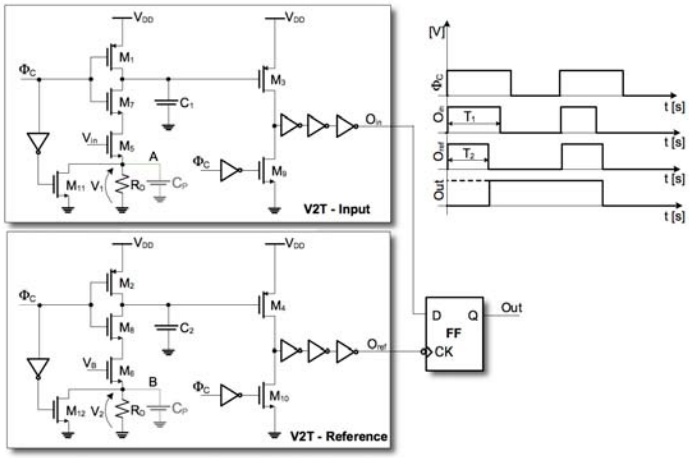

Figure 12.5.2: Time-domain comparator schematic diagram.

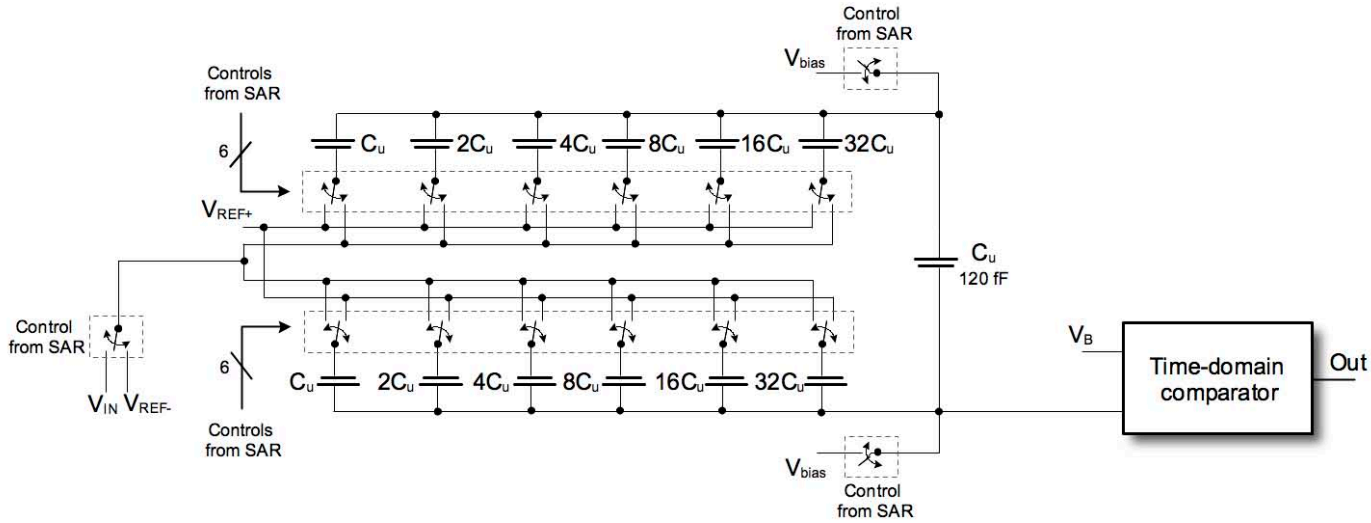

Figure 12.5.3: Binary-weighted split-capacitive arrays.

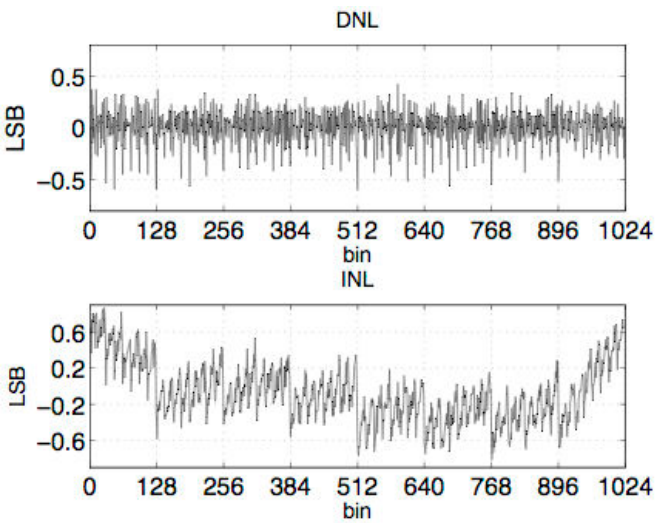

Figure 12.5.4: DNL and INL at 10b resolution.

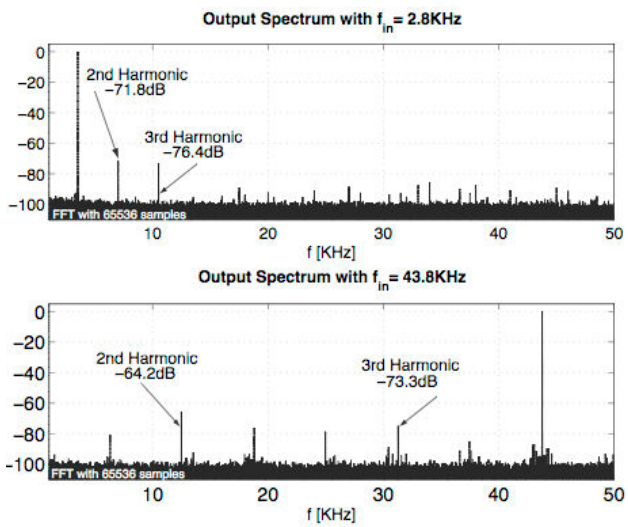

Figure 12.5.5: Output spectrum with f_{IN}=2.8kHz and f_{IN}=43.8kHz.

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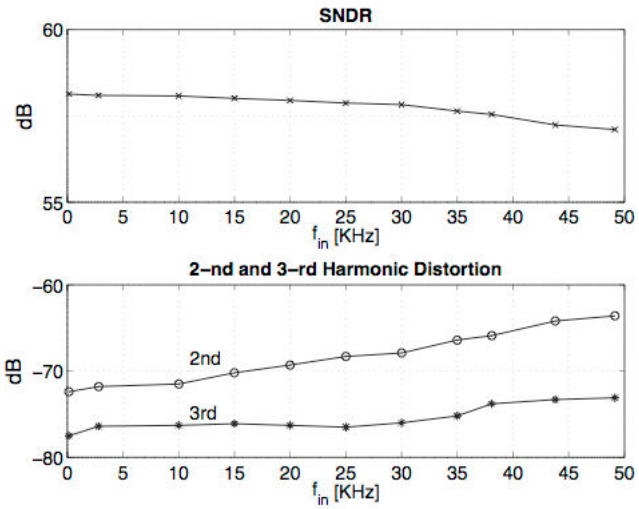

Figure 12.5.6: SNDR, 2nd and 3rd harmonic distortion as a function of f_{IN}.

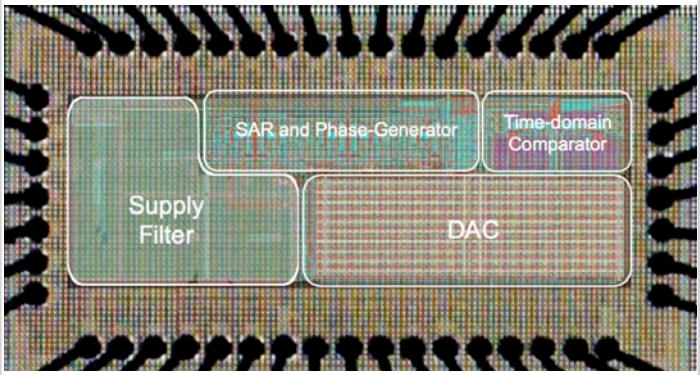

Figure 12.5.7: Chip micrograph.

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