A 9-bit 150-MS/s 1.53-mW Subranged SAR ADC in 90-nm CMOS

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Abstract

This paper reports a subranged SAR ADC consisting of a 3.5-bit flash coarse ADC, a 6-bit SAR fine ADC, and a differential segmented capacitive DAC. The flash ADC controls thermometer MSBs of the DAC and SAR ADC controls the binary LSBs. The segmented DAC improves DNL during MSB transitions. The merged switching of MSB capacitors enhances operation speed. The 9-bit 150-MS/s ADC consumes 1.53 mW from a 1.2-V supply. The ENOB is 8.69 bit and ERBW is 100 MHz. The FOMs at 1.2 V, 150 MS/s and 1 V, 100 MS/s are 24.7 and 17.7 fJ/conversion-step, respectively. At 1.3-V supply voltage, the sampling rate achieves 200 MS/s.

Introduction

In medium to high resolution applications such as video processing, SAR ADCs become more and more important due to their excellent power efficiency. A SAR ADC mainly consists of a comparator, a DAC and SAR logic. The mismatches of the DAC degrade ADC linearity. In general, a binary-weighted DAC has better intrinsic matching than C-2C and split DAC ones. However, the total capacitance of a binary-weighted DAC grows exponentially with resolution. The switching of large MSB capacitors requires long settling time, thus limiting operation speed. The mismatches between MSB and LSB capacitors also degrade DNL [1]. Due to parasitic effect and process variation, the DNL chart possibly shows large steps during MSB transitions, e.g., 128, 256 and 384 in a 9-bit case. This paper proposes a subranged SAR architecture which alleviates these problems.

ADC Architecture and Building Blocks

When a DAC switching happens, a SAR ADC must idle until the DAC voltage settles to required accuracy, and then the next comparison begins. For example, the second comparison must wait for the MSB settling. The switching of first few MSB capacitors is the bottleneck of operation speed. The proposed architecture depicted in Fig. 1 uses a segmented DAC consisting of thermometer MSB capacitors and binary-weighted LSB ones. A flash ADC controls the thermometer capacitors, and a SAR ADC handles the binary ones. The flash ADC performs the first comparison and determines the subrange where input signal locates. Depending on the output of the flash ADC, this ADC pulls down a number of thermometer capacitors. Then, the input range of the subsequent SAR ADC becomes smaller. In a 2-bit coarse ADC case, the input range reduces by a factor of 4.

Fig. 2 depicts the block and timing diagrams of this ADC which contains a 3.5-bit flash ADC, a 6-bit SAR ADC, and a differential segmented capacitive DAC. The capacitance ratio between thermometer and binary capacitors is around 7. The 3.5-bit flash ADC is composed of an S/H circuit, a reference ladder, 14 comparators, and an encoder. The comparators determine 15 subranges. The top and bottom subranges are 1.5 times wider than the others. This architecture tolerates the offset of a coarse comparator up to ±1/32 full scale range.

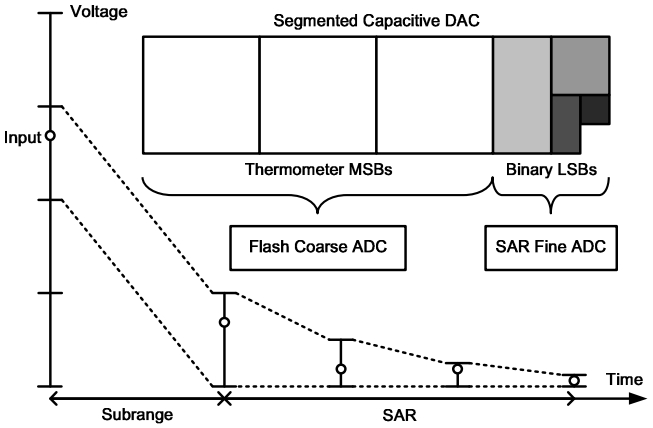

Fig. 1 The concept of a subranged SAR ADC.

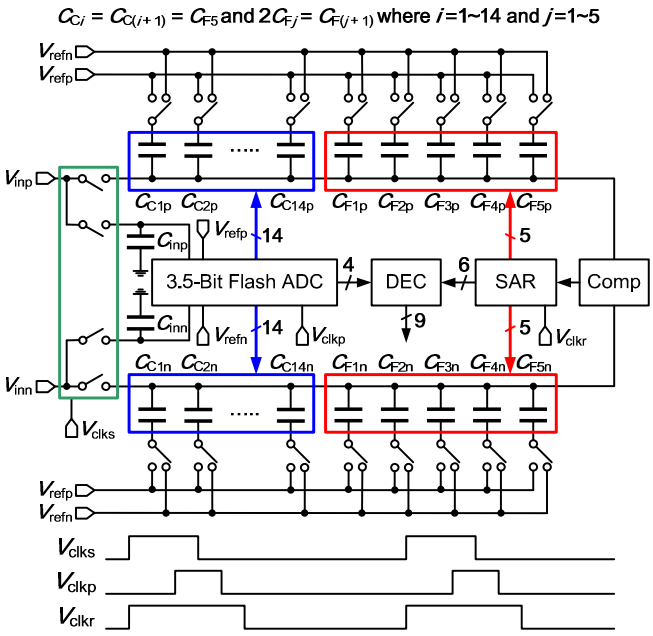

Fig. 2 Block and timing diagrams of the proposed ADC

Hence, the accuracy requirement of the coarse ADC greatly relaxes. The thermometer codes of the flash ADC are the control signals of the thermometer capacitors. This ADC employs the switching scheme in [2] where the comparator input common-mode voltage gradually approaches the negative reference voltage (V_{refn}) during conversions. The offset voltage of a differential pair can be expressed as

$$V_{os} = \Delta V_{th1,2} + 0.5(V_{GS} - V_{th})_{1,2}(\Delta S_{1,2}/S_{1,2} + \Delta R/R) \quad (1)$$

where the first term is a static value due to random mismatch and the second one is a dynamic value related to effective voltage. The static offset is tolerated because a SAR ADC only has one comparator. In [2], the variation of the input common-mode voltage generates a dynamic offset. In this work, after the first DAC switching, the input range is pulled down to 1/8 full scale value. Therefore, the dynamic offset has an insignificant influence on accuracy due to the reduced input range of the fine ADC.

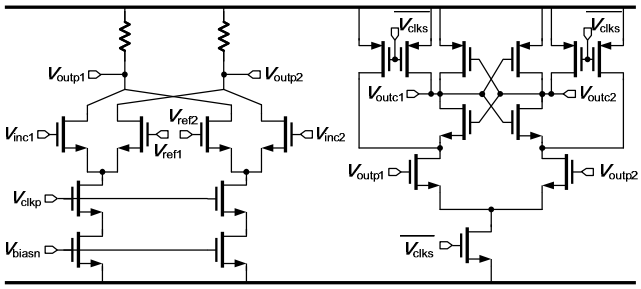

Fig. 3 Preamplifier (left) and comparator (right) of the flash ADC.

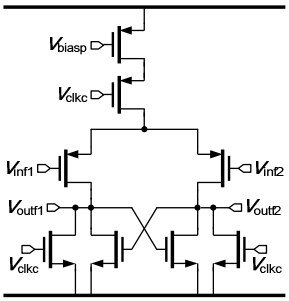

Fig. 4 Comparator of fine ADC.

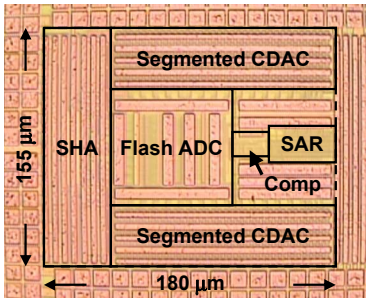

Fig. 5 Chip micrograph.

Fig. 3 shows the preamplifier and comparator of the flash ADC. As V_{clkp} shown in Fig. 2, the preamplifiers turn on before the end of sampling (V_{clks}) and turn off before the beginning of fine conversions (V_{clkr}) to save power consumption. Because the input common-mode voltage gradually approaches V_{refn}, the fine ADC uses a p-type comparator, as depicted in Fig. 4. The fine comparator has a bias transistor to make the gate-source voltage of the input pair stable when its input common-mode voltage varies.

Experimental Results

Fig. 5 shows the prototype fabricated in a 90-nm CMOS process. This ADC occupies a 0.028-mm^2 active area. The capacitive DAC consists of a 2.2-fF fingered sandwich MOM unit capacitor. The peak-to-peak differential input swing of this ADC is 2 V. Fig. 6 shows the peak values of DNL and INL are −0.48/0.35 and −0.48/0.44 LSB, respectively. The static performance shows no large step in MSB transitions. At 150-MS/s, this ADC consumes 1.53 mW from a 1.2-V supply voltage. The sampling time is around 20% of a period. The coarse conversion uses 15% and the fine conversions take the rest. Due to the flash ADC, the first three bits are converted in a short time. Fig. 7 shows a measured spectrum at 50-MHz input. Fig. 8 depicts the SNDR and SFDR versus input frequency. The peak SNDR is 54.07 dB and the peak SFDR is 72.75 dB. The high SFDR demonstrates the excellent linearity of the ADC. At 1.3-V supply, the sampling rate achieves 200 MS/s. At 150-MS/s, the prototype has an FOM of 24.7 fJ/conversion-step. At 1-V 100-MS/s, the FOM is even lower, 17.7 fJ/conversion-step. Table 1 shows the specification summary and comparison to state-of-the-art 9-bit and 10-bit ADCs. Compared to other ADCs, this ADC has the smallest active area and best power efficiency.

Conclusion

A flash ADC is high speed and high power while a SAR ADC is opposite. Traditionally, a subrange ADC consists of two flash ADCs. The complicated reference network of the fine flash ADC limits the achievable resolution. The proposed 9-bit hybrid architecture exploits the high speed of a flash ADC and low power of a SAR ADC. The low complexity, low power flash ADC enhances the overall speed by merging the switching of the first three MSBs. The small input range and low resolution of the SAR ADC enable high accuracy and high speed operation [2]. Without any calibration, the measurement results show this ADC achieves high accuracy, operation speed and power efficiency.

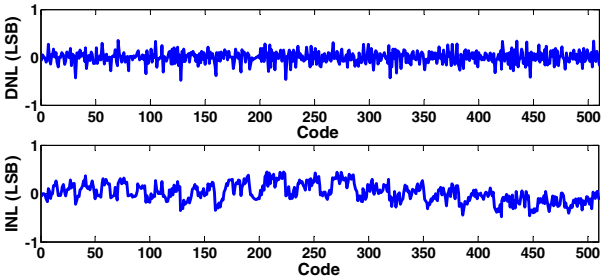

Fig. 6 Measured DNL and INL.

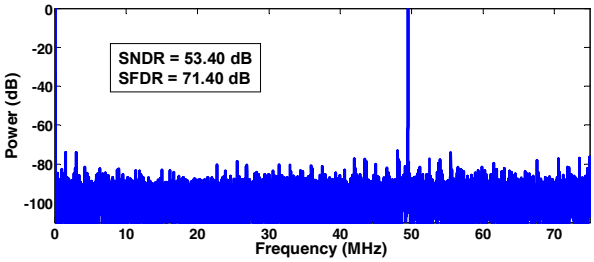

Fig. 7 Measured spectrum at 50-MHz input and 150 MS/s.

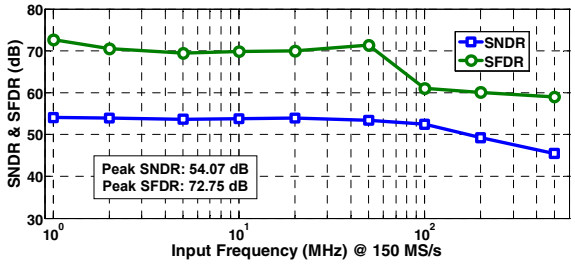

Fig. 8 Measured SNDR and SFDR vs. input frequency.

Table 1 Comparison and Specification Summary

Specification (Unit)	ISSCC'07	ISSCC'08	ISSCC'08	VLSI'09	This Work		
Supply Voltage (V)	1	1	1.2	1.2	1	1.2	1.3
Sampling Rate (MS/s)	50	40	100	50	100	150	200
Power (mW)	0.7	0.82	4.5	0.92	0.75	1.53	2.20
ENOB (bit)	7.8	8.56	9.5	8.48	8.72	8.69	8.66
ERBW (MHz)	10	32	200	100	50	100	100
FOM (fJ/conv.-step)	65	54	62	52	17.7	24.7	27.2
Architecture	SAR	SAR	Pipelined	SAR	Flash + SAR		
Resolution (bit)	9	9	10	10	9		
Active Area (mm^2)	0.08	0.09	0.07	0.075	0.028		
Technology	90 nm	90 nm	65 nm	130 nm	90 nm		

Acknowledgment

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References

[1] C.-H. Lin and K. Bult, "A 10-b, 500-MSample/s CMOS DAC in 0.6 mm^2," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 1948-1958, Dec. 1998.

[2] C.-C. Liu, S.-J. Chang, G.-Y. Huang, and Y.-Z. Lin, "A 0.92mW 10-bit 50-MS/s SAR ADC in 0.13µm CMOS process," *IEEE Symp. on VLSI Circuits*, Jun. 2009, pp. 236-237.