A 90 nm Logic Technology Featuring 50nm Strained Silicon Channel Transistors, 7 layers of Cu Interconnects, Low k ILD, and 1 um^2 SRAM Cell

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Abstract

A leading edge 90 nm technology with 1.2 nm physical gate oxide, 50 nm gate length, strained silicon, NiSi, 7 layers of Cu interconnects, and low k CDO for high performance dense logic is presented. Strained silicon is used to increase saturated NMOS and PMOS drive currents by 10-20% and mobility by > 50%. Aggressive design rules and unlanded contacts offer a 1.0μm^2 6-T SRAM cell using 193nm lithography.

Introduction

The power dissipation of modern microprocessors has been rapidly increasing, driven by increasing transistor count and clock frequencies. The rapidly increasing power has occurred even though the power per gate switching transition has decreased approximately $(0.7)^3$ per technology node due to voltage scaling and device area scaling. Figure 1 shows these trends for Intel's microprocessors and CMOS logic technology generations. In this paper we describe a 90 nm generation technology designed for high speed and low power operation. Strained silicon channel transistors are used to obtain the desired performance at 1.0V to 1.2V operation.

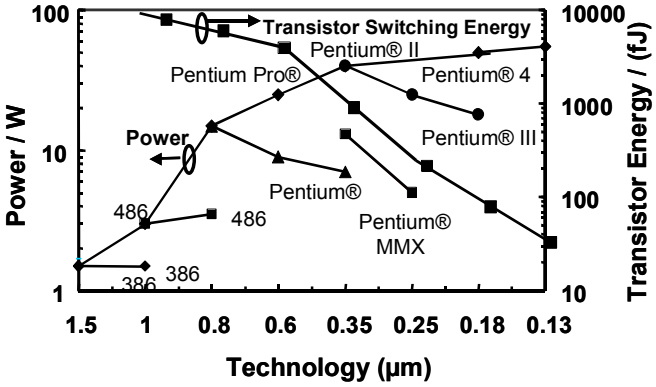

Figure 1: Power and transistor switching energy trends.

Process Flow and Technology Features

Front-end technology features include shallow trench isolation, retrograde wells, shallow abrupt source/drain extensions, halo implants, deep source/drain, and nickel salicidation. N-wells and P-wells are formed with deep phosphorous and shallow arsenic implants, and boron implants respectively. The trench isolation is 400 nm deep to provide robust intra- and inter-well isolation for N+ to P+ spacing below 240 nm while maintaining low junction capacitance. Sidewall spacers are formed with CVD Si_3N_4 deposition, followed by etch-back. Shallow source-drain extension regions are formed with arsenic for NMOS and boron for PMOS. NiSi is formed on poly-silicon gate and source-drain regions to provide low contact resistance.

193 nm lithography is used to pattern the poly-silicon gate layer down to a gate dimension of 50 nm as shown in Figure 2. The minimum pitches and thicknesses for the technology layers are summarized in Table 1. The result is a 1.0μm^2 6-T SRAM cell without the use of a local interconnect layer. Figure 3 shows a top-down SEM image of the polysilicon gate conductor. The interconnect technology uses dual damascene copper to reduce the resistances of the 7 layers of interconnects. Carbon-doped oxide (CDO) is used as inter-level dielectric (ILD) to reduce the dielectric constant. The dielectric constant k is measured to be 2.9.

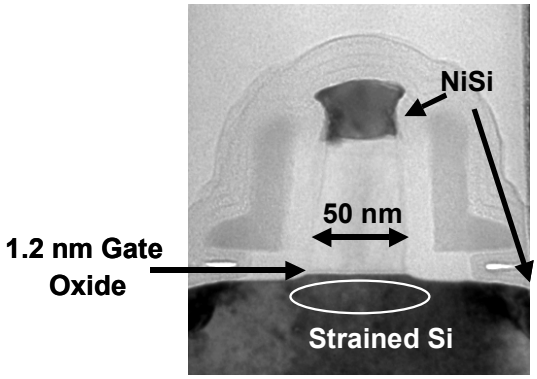

Figure 2: TEM of 50nm transistor.

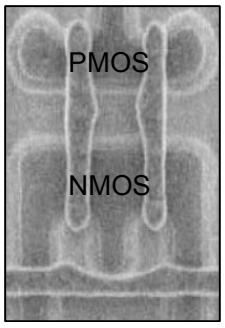

Figure 3: Top-down SEM of poly silicon gate conductor of 1.0μm^2 6-T SRAM bit.

LAYER	PITCH	THICK	AR
Isolation	240	400	-
Poly-Si	260	140	-
Metal 1	220	150	1.4
Metal 2,3	320	256	1.6
Metal 4	400	320	1.6
Metal 5	480	384	1.6
Metal 6	720	576	1.6
Metal 7	1080	972	1.8

Table 1: Layer pitch, thickness (nm) and aspect ratio.

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Transistor

Gate length and gate oxide scaling have been the dominant factors to improve transistor performance [1-3]. In this technology, we continue with gate length and oxide scaling but also use SiGe to strain the silicon channel for improved mobility. To control short channel effects, a thin 1.2 nm physical oxide is used as shown in Figure 4. The thin oxide enables MOSFETs with well-controlled short channel characteristics down to a physical gate of 50 nm, which is a 0.7x scaling of our previous generation on a two-year offset [3] (Figure 5).

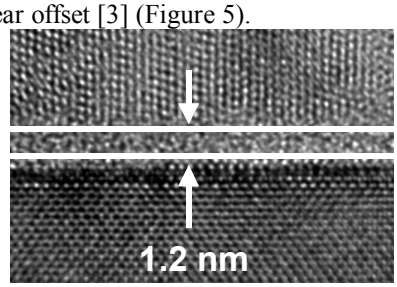

Figure 4: TEM of 1.2nm gate oxide.

Strained silicon channels have been shown experimentally [4] and theoretically [5] to offer large mobility enhancement (greater than 2X), thus, giving strong motivation for incorporation into future CMOS technologies. Yield considerations and CMOS flow integration issues place constraints on the magnitude of silicon strain and hence mobility enhancement. In this work, strained silicon channels with greater than 50% mobility enhancement are inserted into an integrated process flow with equivalent yield. Due to electron and hole velocity saturation, the benefit strained enhanced mobility on short channel device performance has been the subject of some debate. The first confirmation that strain-enhanced mobility improves saturated drive current for short 0.1um devices was shown in 1998 [6] and again recently in 2001 [7]. For the first time we show that for sub-100 nm transistors with gate lengths as small as 50 nm, the enhanced mobility still improves the saturated drive current. Also, we observe that for the same magnitude of electron and hole mobility improvement, a larger saturation current gain is observed for p channel transistors due to velocity saturation being less important for holes than electrons. Figures 6 and 7 show the saturated drive currents for strained silicon surface n and p channel MOSFETs, which are improved 10 – 20 % over our best 50 nm non-strained channel control device (I_{OFF} = 40 nA/µm).

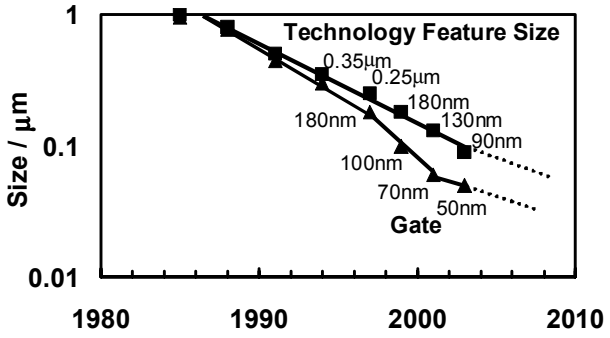

Figure 5: Transistor size and technology trend.

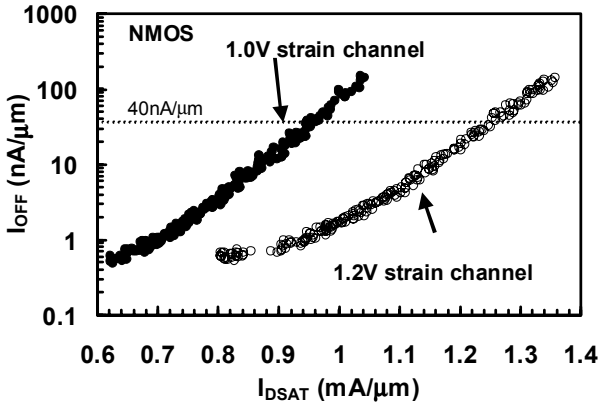

Figure 6: NMOS I_{ON} vs. I_{OFF} at 1.0V and 1.2V.

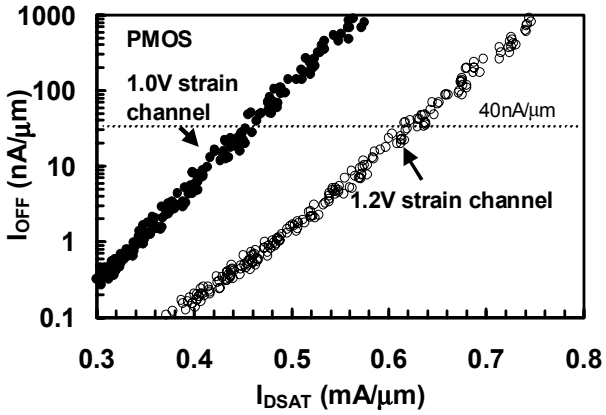

Figure 7: PMOS I_{ON} vs. I_{OFF} at 1.0V and 1.2V.

Three techniques to strain the silicon channel have been previously reported (Figure 8): (a) biaxial in-plane tensile strain using epitaxial SiGe [4-6, 9-12], (b) strain by a tensile film [13,14], and (c) strain by mechanical force [7]. Strained silicon channel CMOS obtained by a tensile film (without implant relaxation) provides small to no net gain since it improves electron mobility but degrades hole mobility [13]. Implant relaxation is also difficult to implement due to close proximity of n and p-channel transistors [14]. It is interesting that large hole mobility enhancement is predicted theoretically [5] but much smaller improvements have been observed experimentally [4]. Many publications have reported on large electron mobility enhancement for biaxial in-plane tensile straining using SiGe; however, the magnitude of enhanced hole mobility has varied [4,9]. Also phonon-limited mobility enhancement is predicted theoretically [8] to be present at both low and high effective vertical fields but experimental data have been inconclusive [4,9], possibly due to increased surface roughness scattering at high effective field in some of the samples.

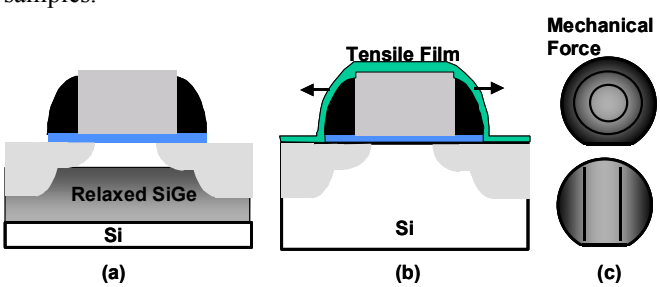

Figure 8: Techniques to strain the silicon channel.

This work, while having some similarities with the above-discussed approaches, is unique and uses epitaxial SiGe to strain the silicon channel. High mobility is achieved by making devices with equivalent fixed oxide charge and surface roughness compared to bulk. In this work, both the electron and hole mobility gains are present at both low and high effective vertical fields. The enhanced hole mobility versus effective field is shown in Figure 9 and compared to other recent publications. By varying the Ge concentration, the strain in the silicon can be increased or decreased. Figure 10 shows the hole mobility enhancement versus strain. In this work with high yield, we target > 50% improved mobility.

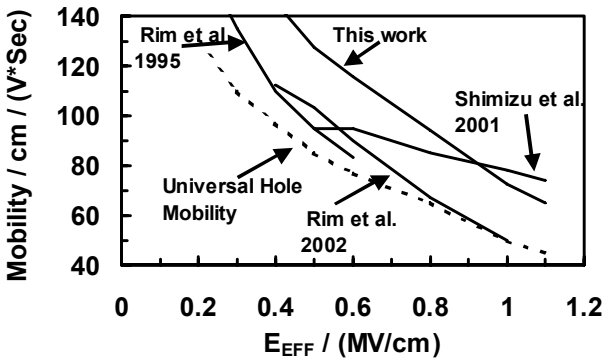

Figure 9: Hole mobility as a function of effective field.

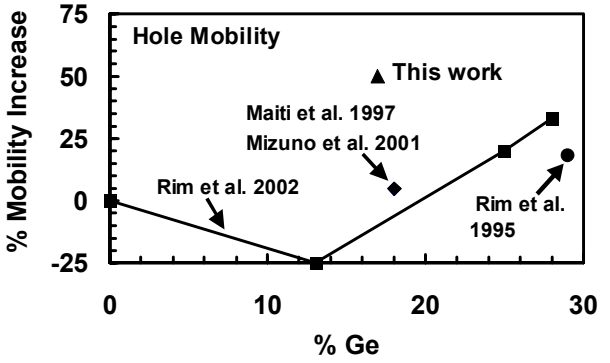

Figure 10: Low field hole mobility vs. Ge concentration.

Saturation drive currents are 1.26 mA/μm for N and 0.63 mA/μm for P-channel high V_T devices with 40 nA/um off-state leakage (Figures 6 and 7). Low threshold devices are also offered with 10X higher leakage and 15% higher drive current. Subthreshold slopes for both N and P-channel high and low V_T devices remain well controlled at less than 85 mV/decade at L_{GATE} = 50 nm. The dielectric time to fail for the 1.2 nm oxide on the strained silicon channel meets the requirements for 1.2 V operation including tolerances (Figure 11).

Since the SiGe in the source/drain regions inhibits cobalt silicide transition to the low resistivity disilicide phase, nickel silicide or cobalt silicide with a silicon buffer layer in the source drains is needed. Both approaches can support low resistance polycide down to < 50 nm as shown in Figure 12. However, nickel silicide is the primarily approach since it provides lower cost, improved interface resistance and better narrow gate polyicide resistance compared to cobalt silicide with raised source/drains.

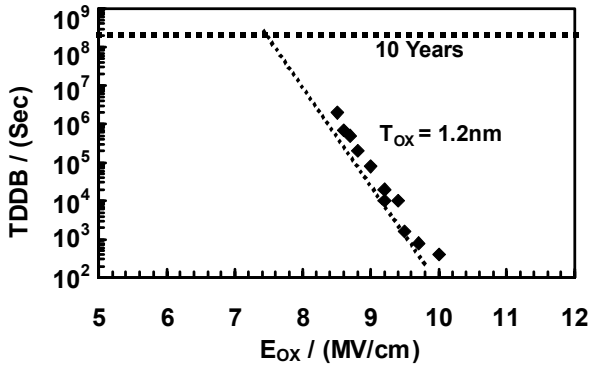

Figure 11: 1.2 nm gate oxide time to fail vs. electric field.

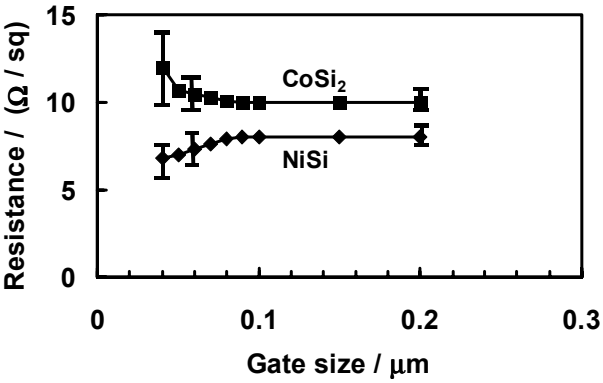

Figure 12: Resistance vs. gate size for NiSi and $CoSi_2$.

Interconnects

This process technology uses dual damascene copper interconnects and CDO (k=2.9) inter-level dielectric to achieve reliable, high performance wiring. Figure 13 is a cross-section SEM image showing the dual damascene interconnects. Metal pitches are 220 nm at the first metal layer and increase to 1080 nm at the top layer. Contacts to the substrate use tungsten plugs. CDO is used for all layers except M1 and M7.

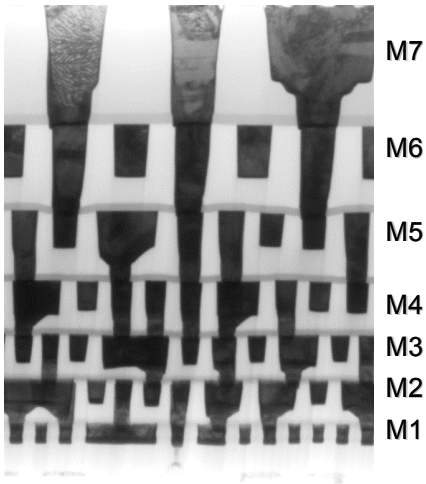

Figure 13: Cross-section SEM image of a processed wafer.

Vias are etched first before the trenches without using two etch-stop layers [15]. The single thin SiN provides 15% lower line to line capacitance over the two etch stop approach. The low K ILD reduces the line-to-line capacitances on average 22% over fluorinated SiO_2 used on the 130 nm technology [2,3] as shown in Figure 14. Metal aspect ratios are optimized for minimum RC delay, and range from 1.6 to 1.8. To benchmark the performance of interconnects, Figure 15 shows the RC delay in picoseconds per millimeter of wire. Data for each metal layer is shown as a function of the minimum pitch at that layer. For a given pitch, a 70% reduction in RC is achieved by using Cu interconnects and CDO ILD over aluminum and fluorinated SiO_2 [1].

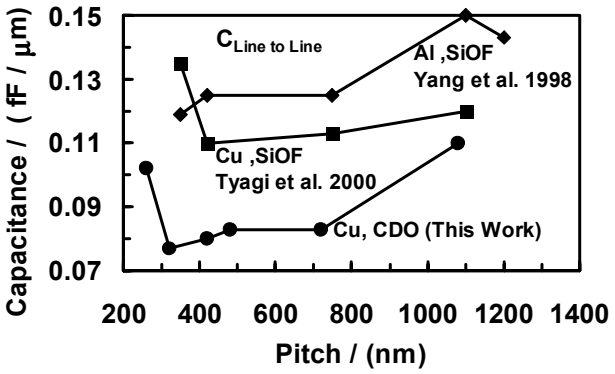

Figure 14: Line-to-line capacitance as a function of layer pitch.

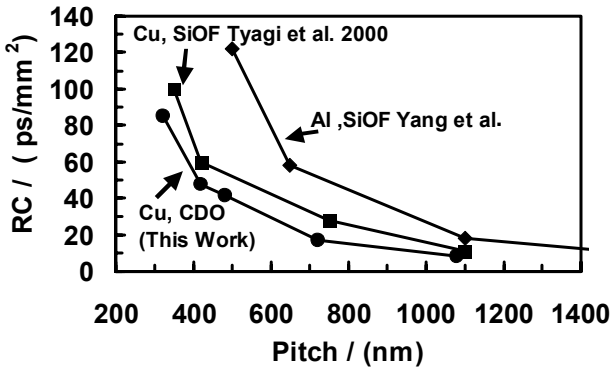

Figure 15: RC delay for a wire length of 1mm as a function of layer pitch.

SRAM Test Vehicle

A yielding 52 Mbit CMOS SRAM has been designed and fabricated on this technology incorporating the strained silicon channel transistors and 7 metal layers with CDO. A die photo of the 52 Mbit SRAM is shown in Figure 16. The 52 Mbit SRAM die size is 109 mm^2 and contains 330 millions transistors. All 330 million transistors have a strained silicon channel and are used as a yield and reliability test vehicle during the process development. Figure 17 shows the schmoo plot for the SRAM, i.e. the Fmax as a function of voltage. The SRAM operates at > 2.0 Ghz at 1.2 V.

Conclusion

A 90 nm generation logic technology has been demonstrated with low power high performance strained silicon channel transistors. Excellent interconnect performance is achieved by using 7 layers of dual damascene Cu with CDO dielectrics. The technology performance capabilities are demonstrated with a strained silicon channel 52 Mbit SRAM operating at 2.0 GHz.

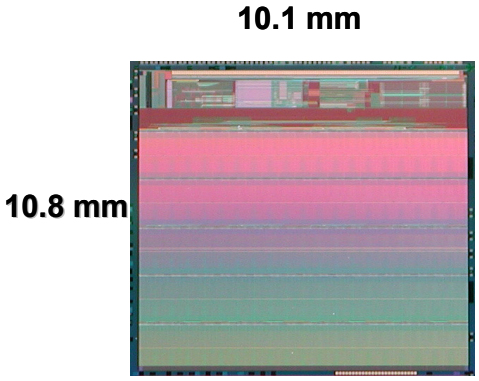

Figure 16: Die photo of 52 Mbit SRAM with 1µm^2 6-T cell.

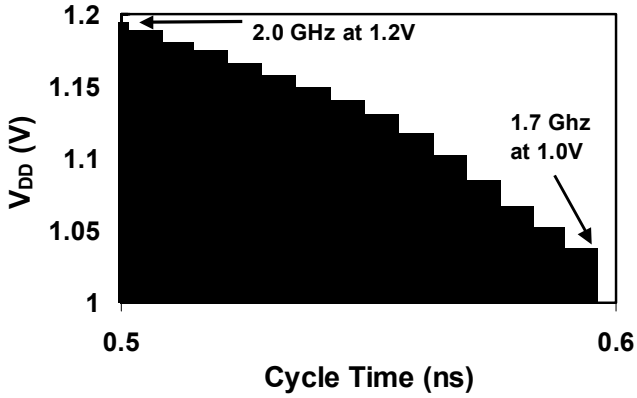

Figure 17: Schmoo plot for the 52 Mbit SRAM.

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