A 90nm Variable Frequency Clock System for a Power-Managed Itanium® Architecture Processor

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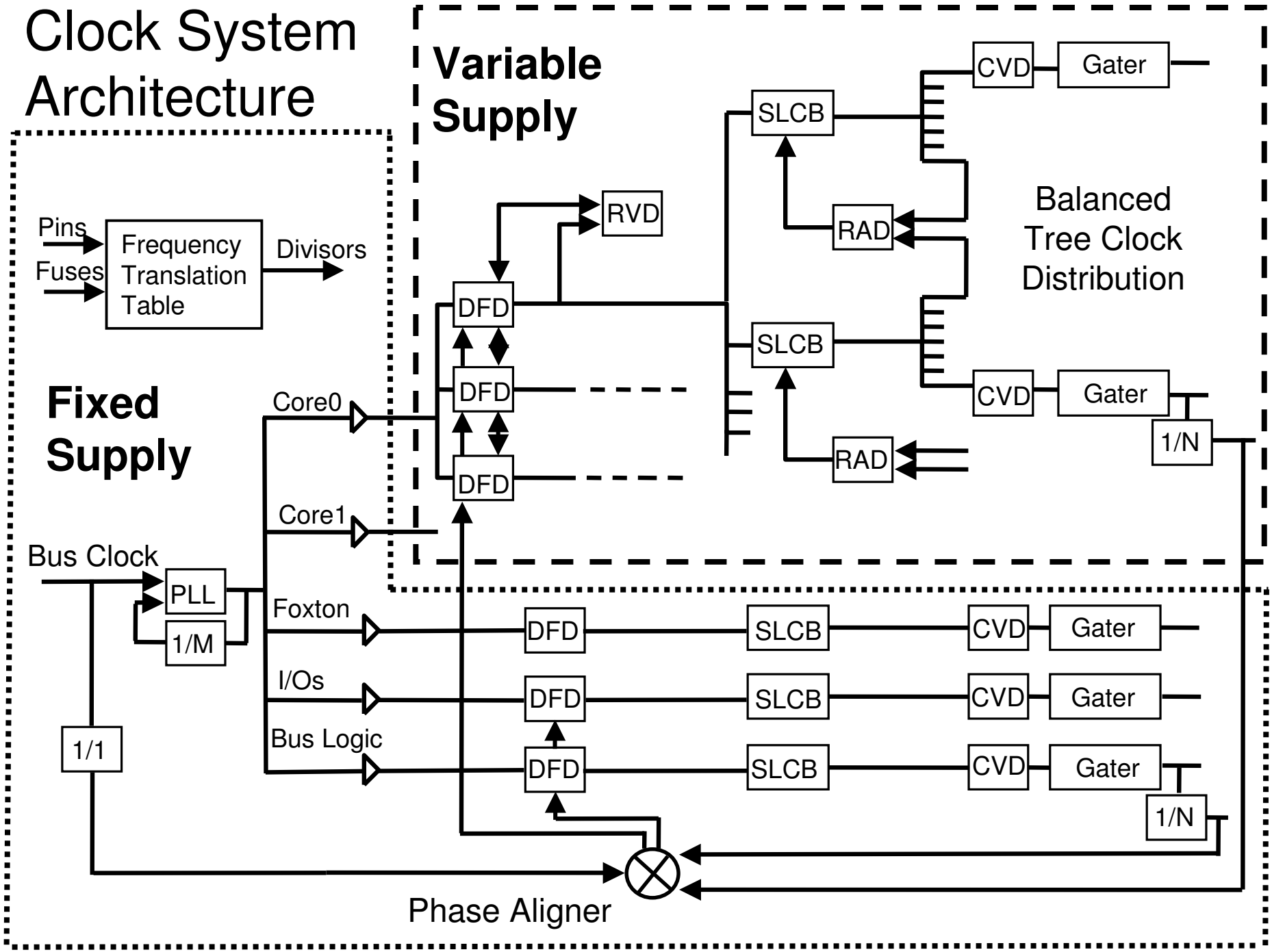
Presentation Overview

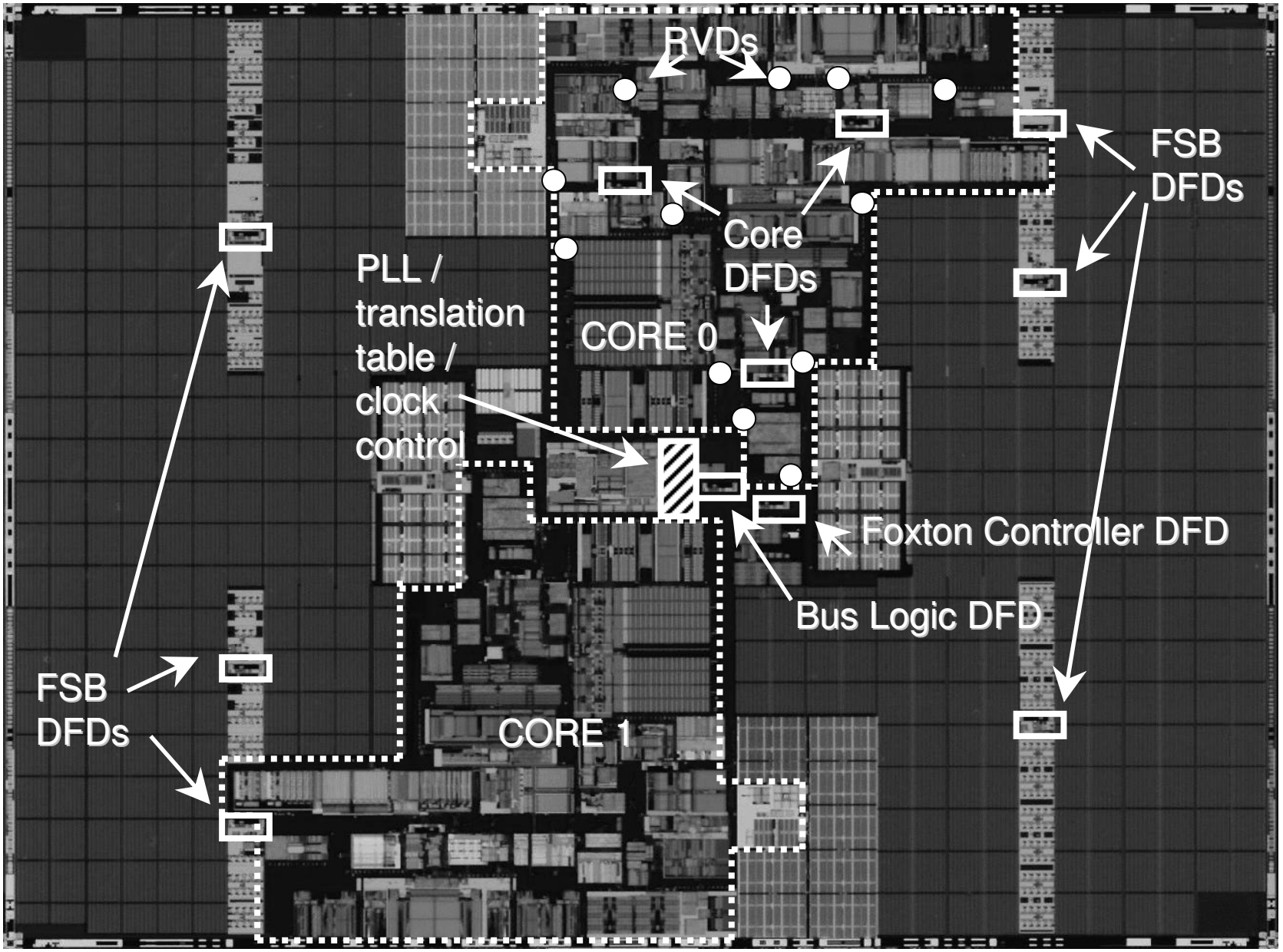
- Montecito Clock System Architecture
- Montecito Voltage to Frequency Converter (VFC) Architecture
  - Digital Frequency Divider (DFD)
  - Regional Voltage Detector (RVD)
- Results
- Summary and Acknowledgements


Clock System Architecture
Variable Supply
Fixed Supply
Pins
Fuses
Frequency Translation Table
Divisors
RVD
DFD
DFD
DFD
SLCB
SLCB
RAD
RAD
CVD
Gater
CVD
Gater
1/N
Balanced Tree Clock Distribution
Core0
Core1
Bus Clock
PLL
1/M
1/1
Foxton
I/Os
Bus Logic
DFD
DFD
DFD
SLCB
SLCB
SLCB
CVD
Gater
CVD
Gater
CVD
Gater
1/N
Phase Aligner

Montecito Clock Generation Overview

- PLL generates master clock: Fmax = M*F_{bus_clock}
- DFDs lock on Fmax using local DLLs
  - Synthesize core / uncore frequencies in 1.6% Fmax steps (*ticks*)
  - DFD range is Fmax*1.0 to Fmax*0.504
  - Translation table sets DFD frequency at startup
- Supply / Clock Domains
  - 2 Cores : variable V, F
  - Uncore (bus logic): fixed V, F = N * bus clock
  - Foxton controller : fixed V, F = 1 GHZ, DSP algorithms
  - Master PLL : fixed V, F, within clock system only

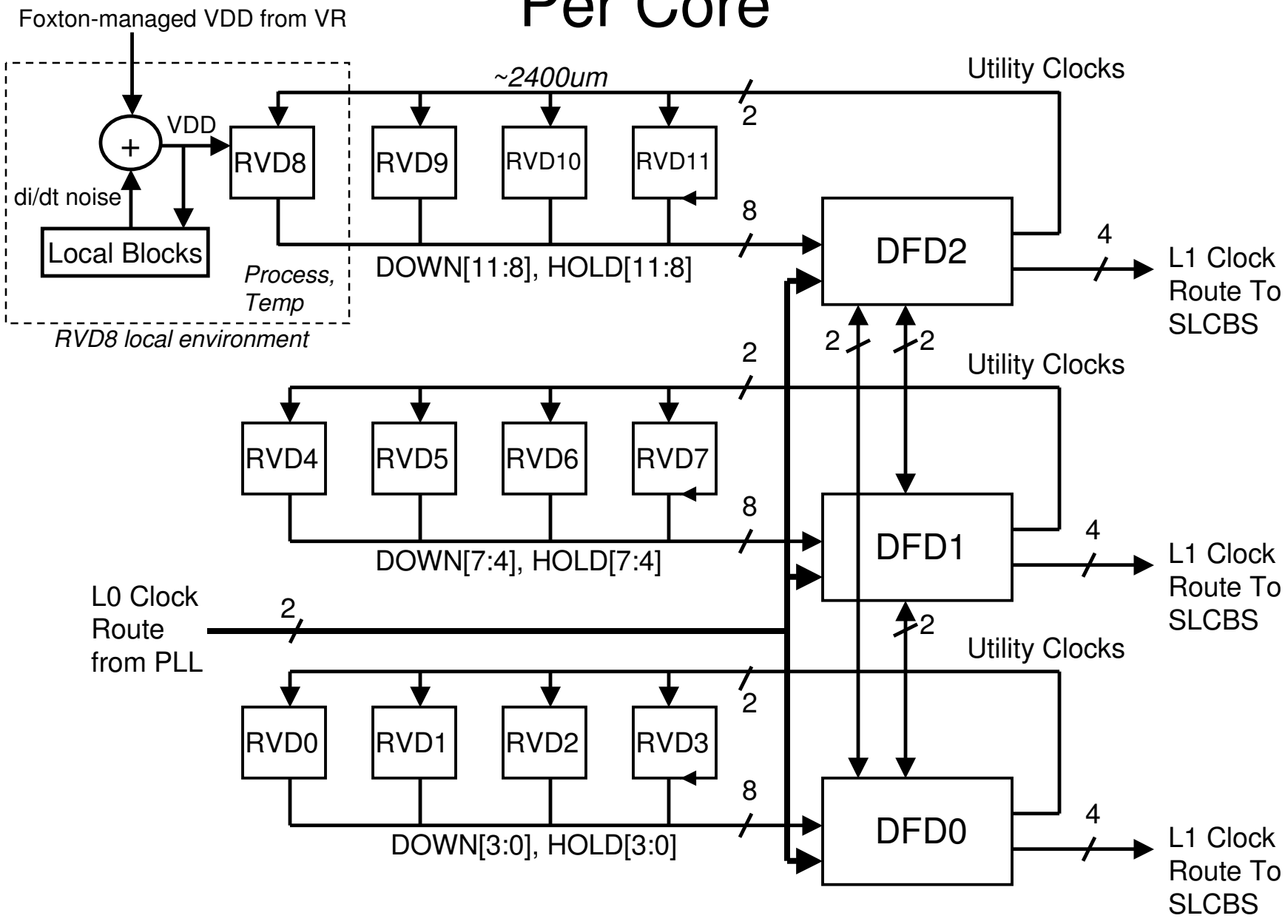
Montecito Clock System Floorplan



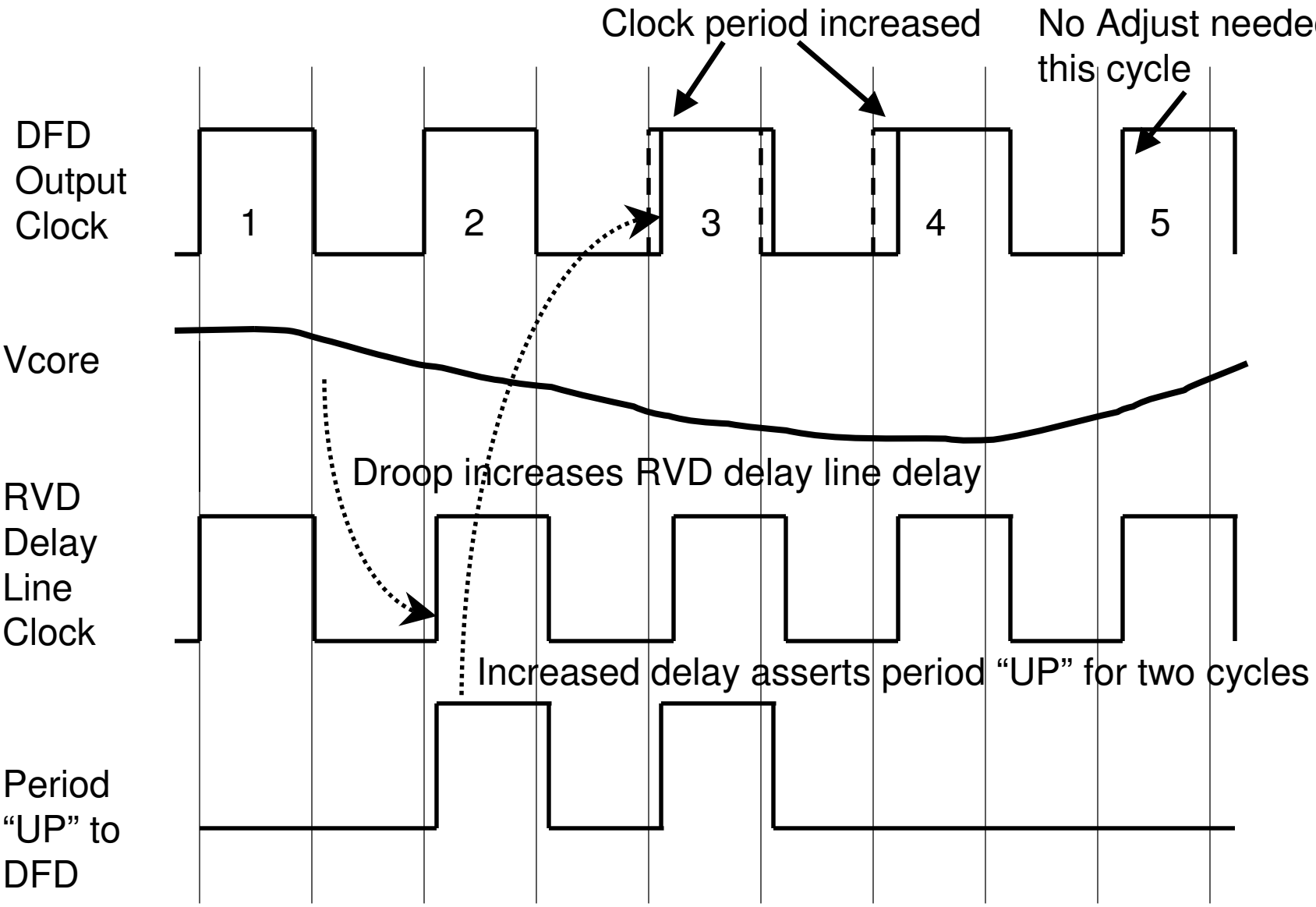
Clock System Modes

- Fixed Frequency (FFM)
  - Cores/Uncore are frequency and phase aligned
  - Cores/Uncore interfaces synchronous
- Variable Frequency (VFM)
  - Core supply modulated by Foxton Controller to manage power envelope
  - Core frequencies track Vcore via Regional Voltage Detector (RVD) V-F curves
    - Respond to Foxton modulation and local transients
    - V-F curves match worst-scaling paths on chip
  - Core/Uncore interfaces asynchronous

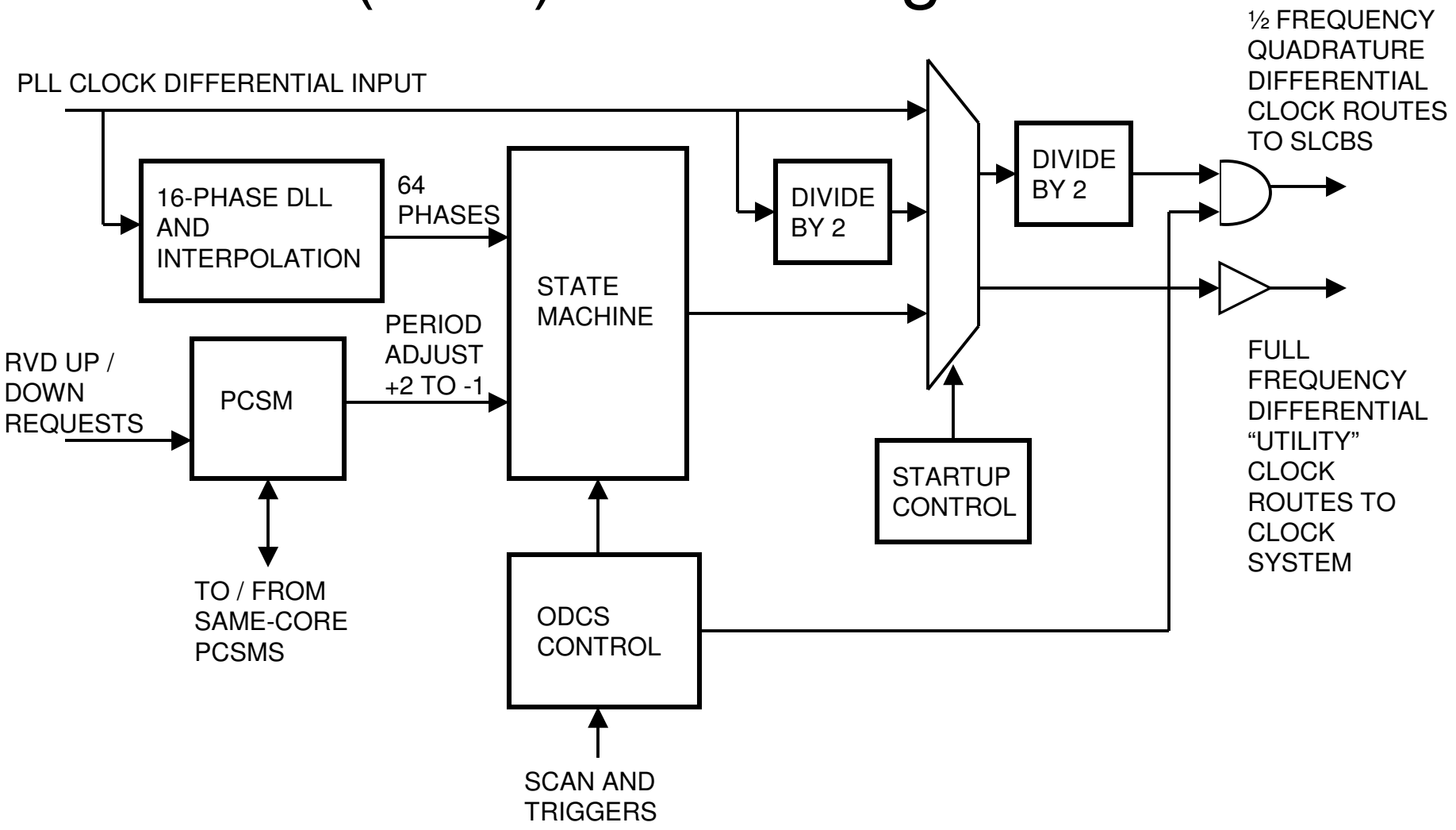
Voltage-to-Frequency Conversion (VFC) Per Core



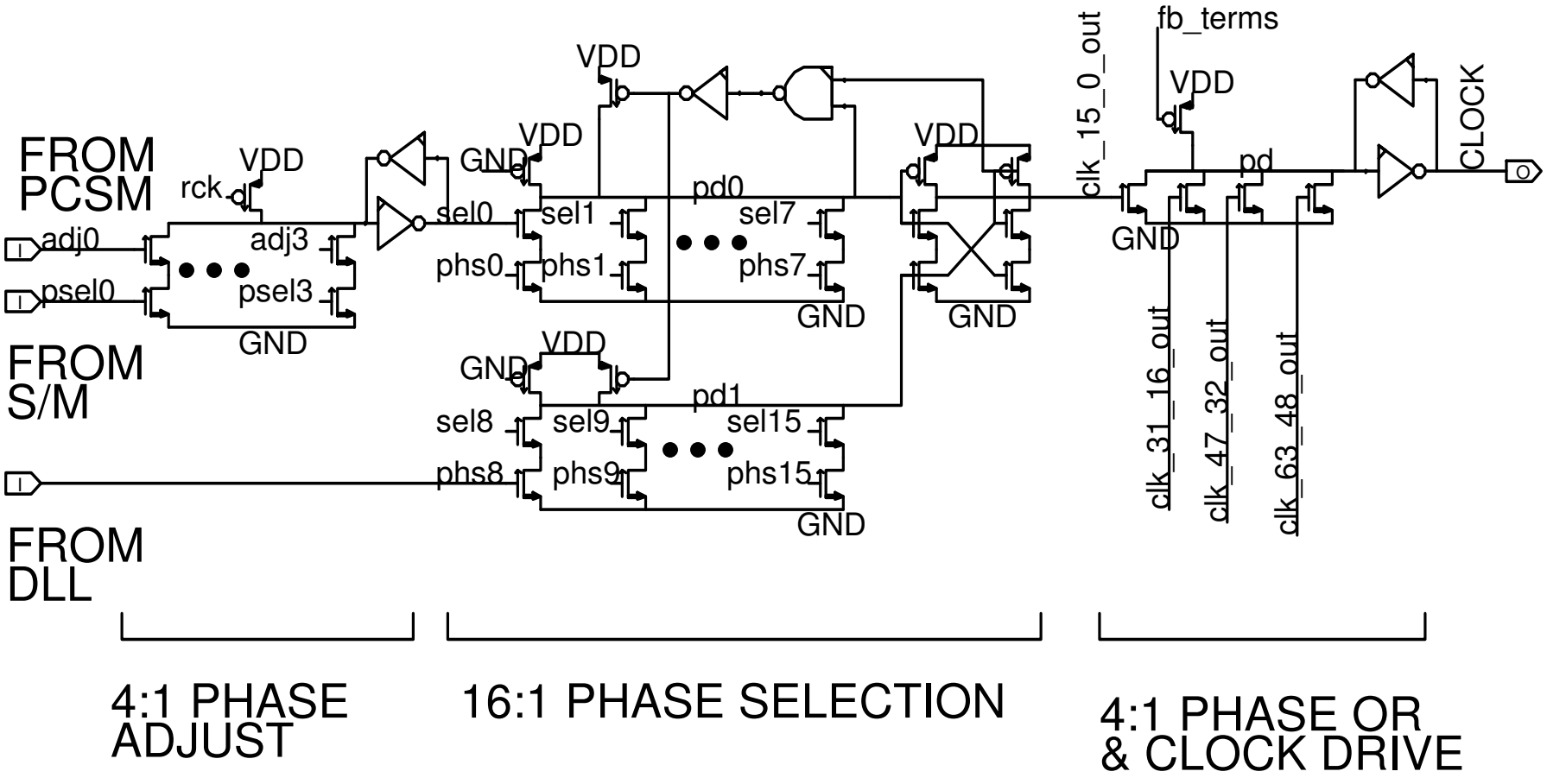
Example VFC Supply Droop Response



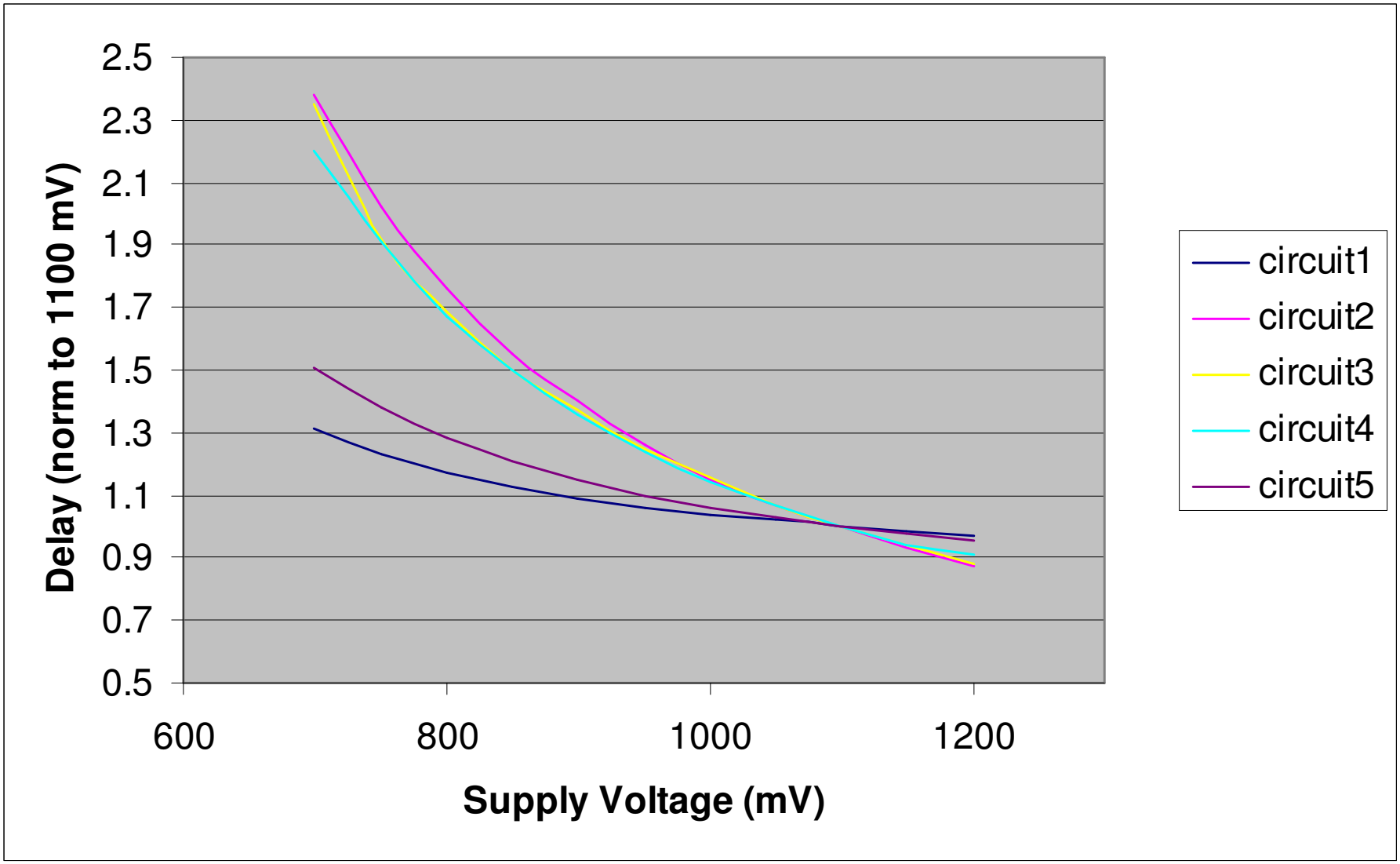
Digital Frequency Divider (DFD) Block Diagram



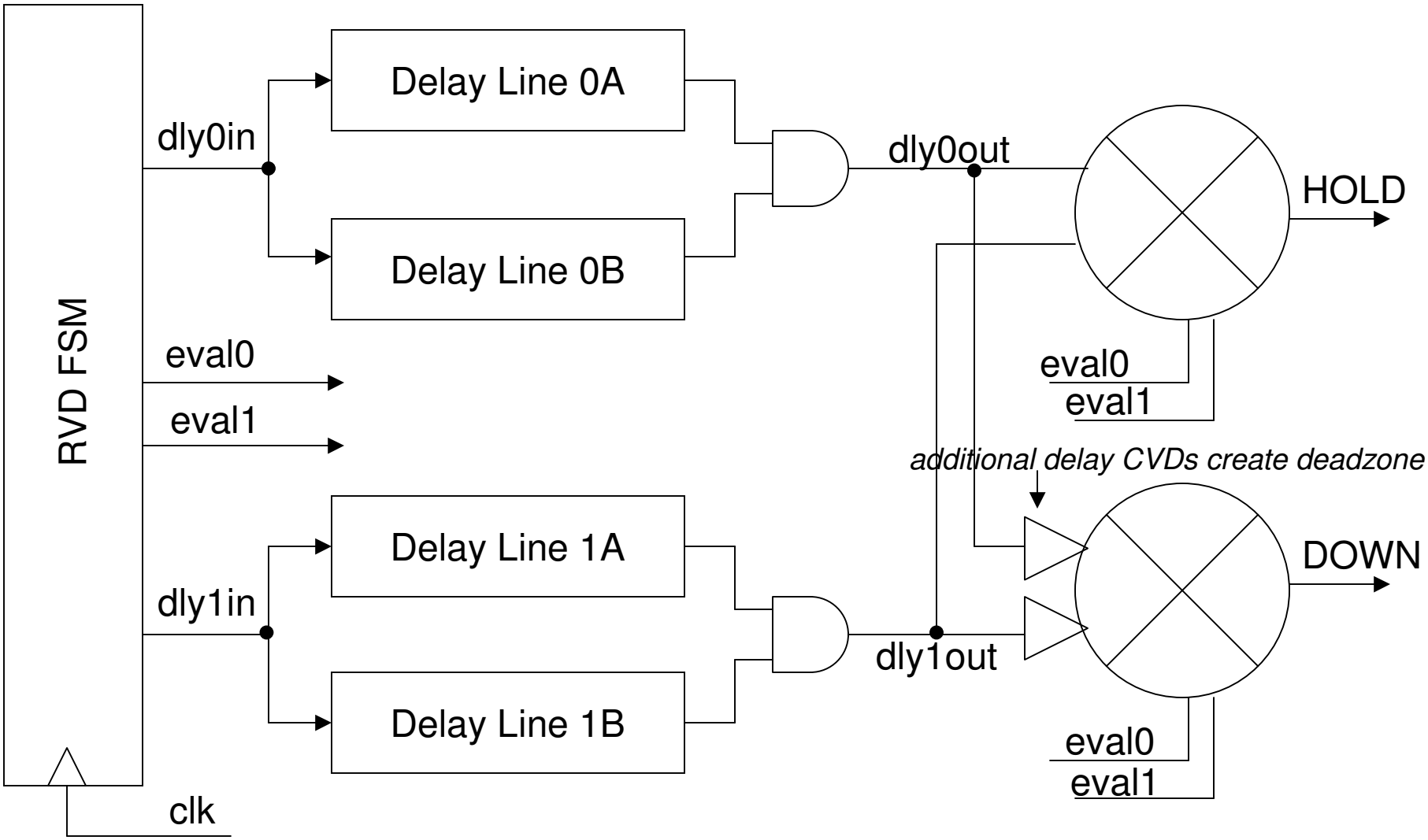
DFD Phase Selection Datapath



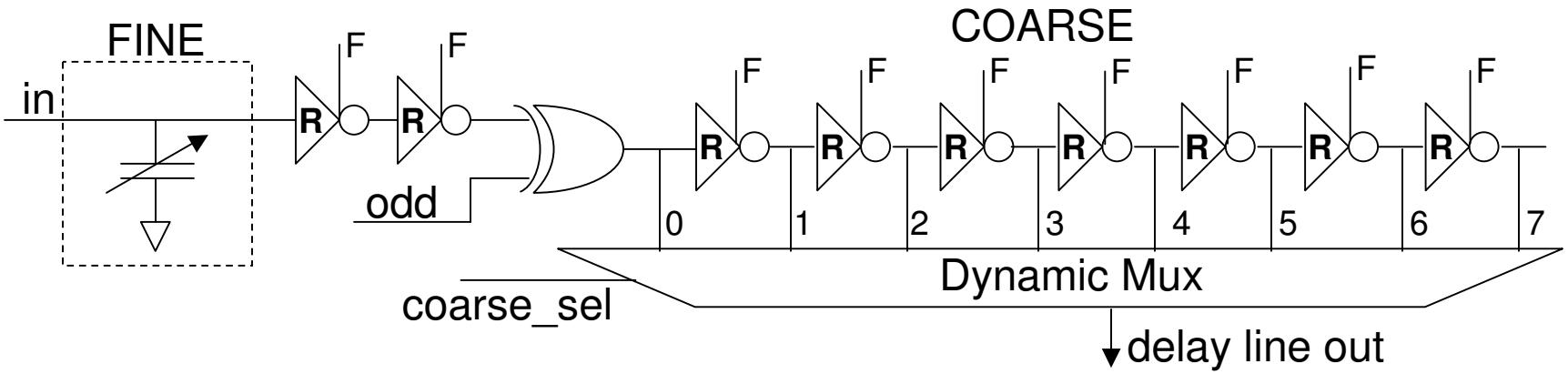
VFC/RVD Voltage Tracking and CMOS Critical Path Scaling



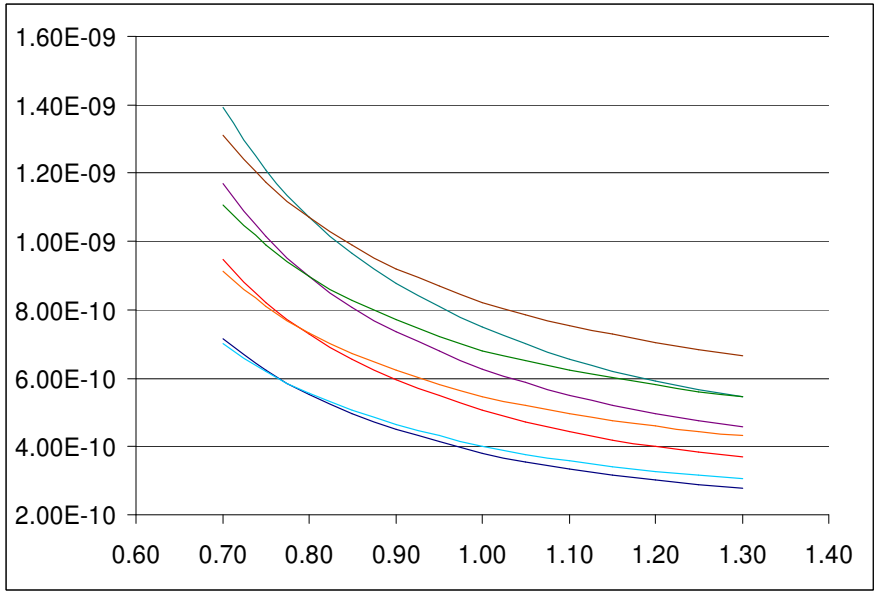
RVD Block Diagram



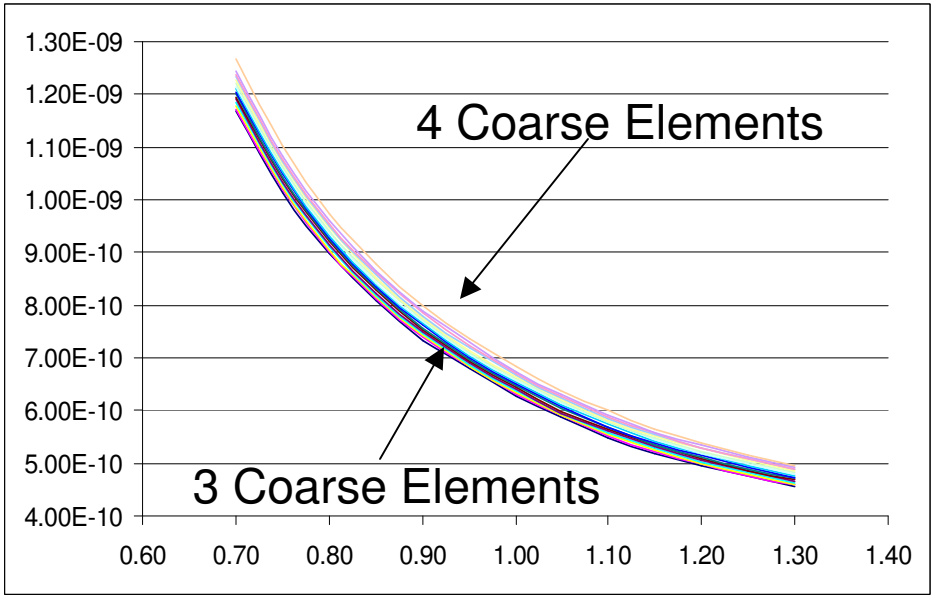
RVD Delay Line



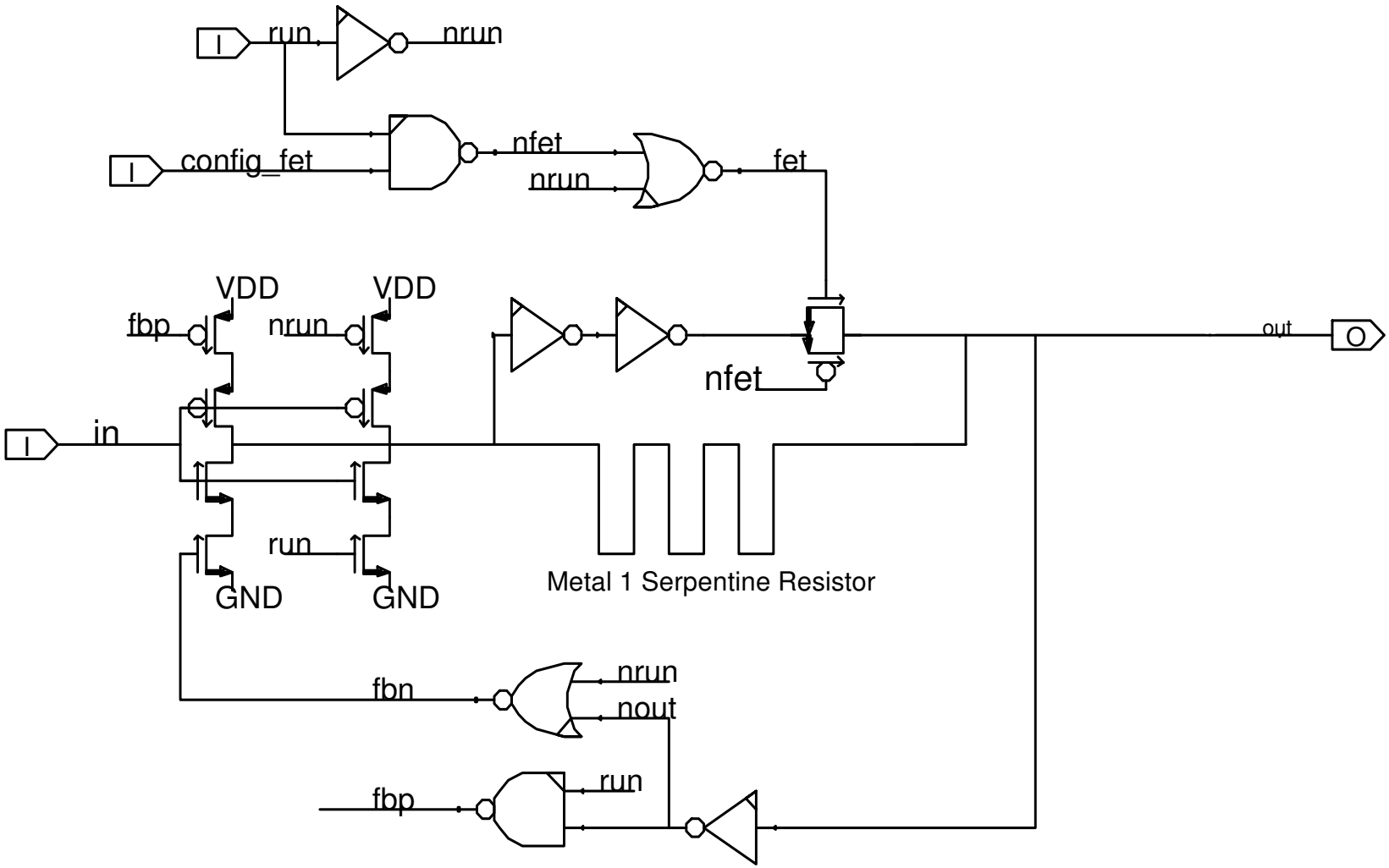
Coarse Delay Incremental Curves



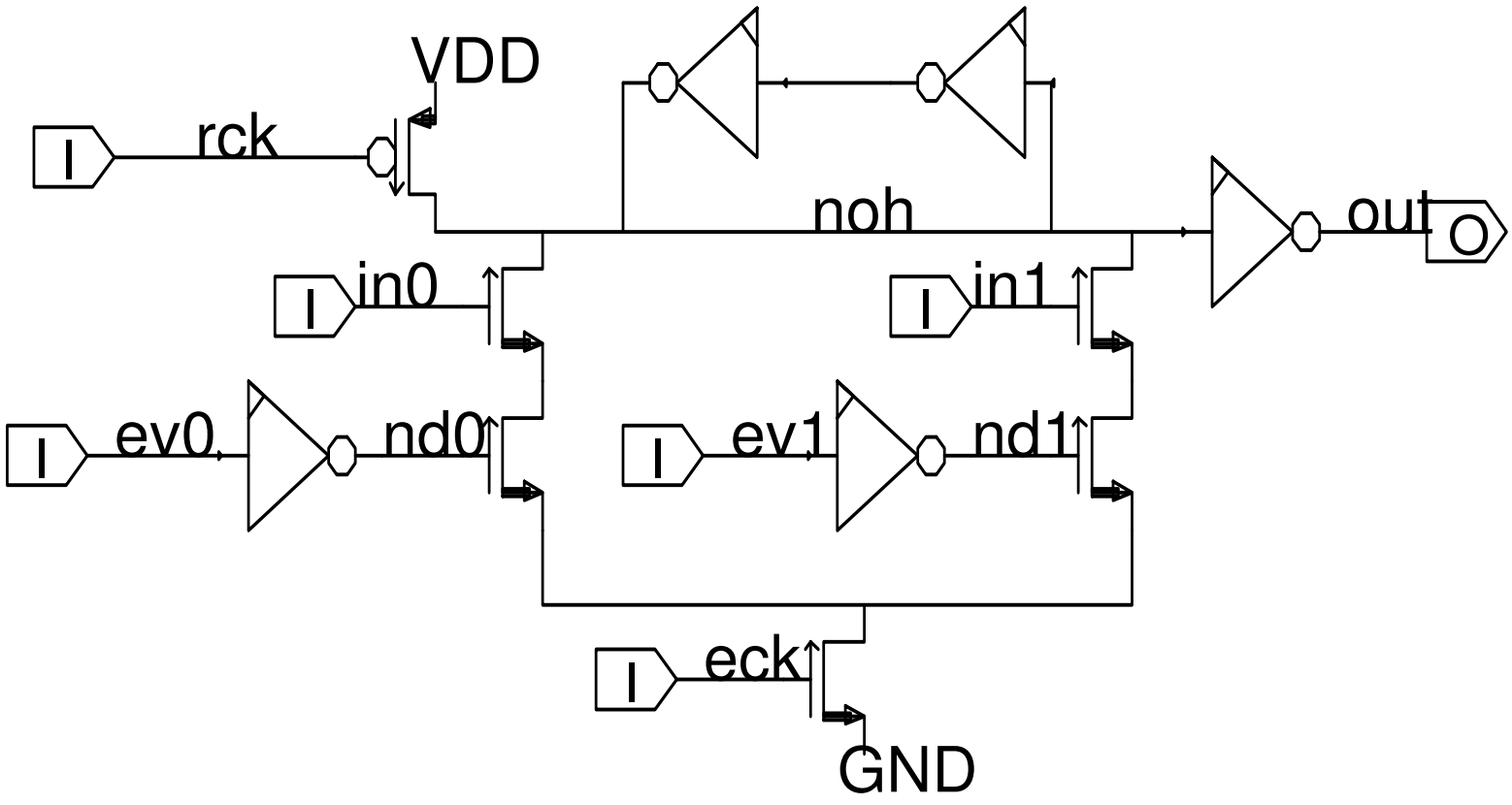
Fine Delay Incremental Curves

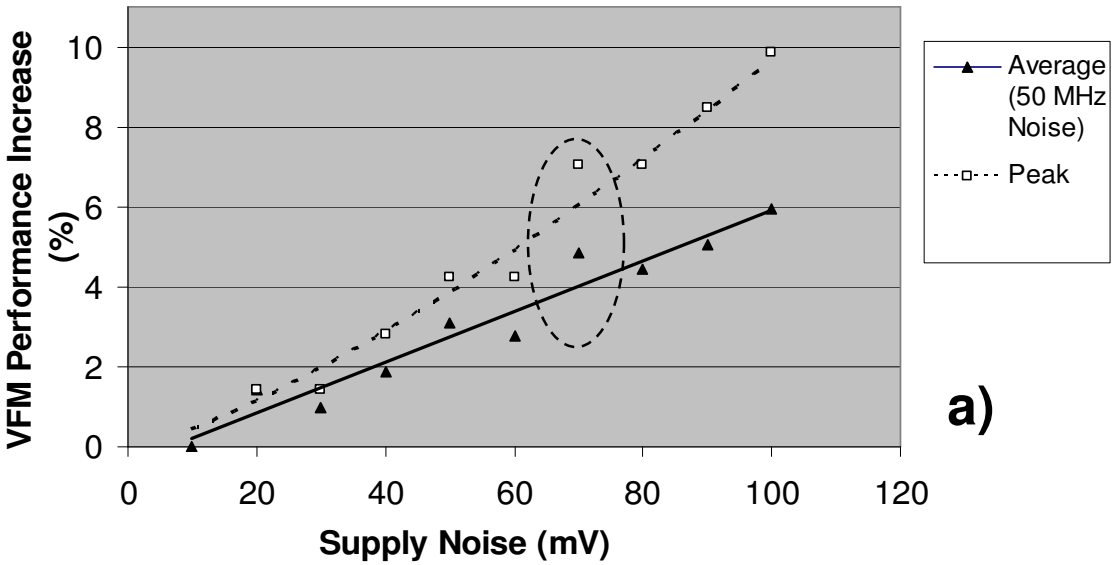


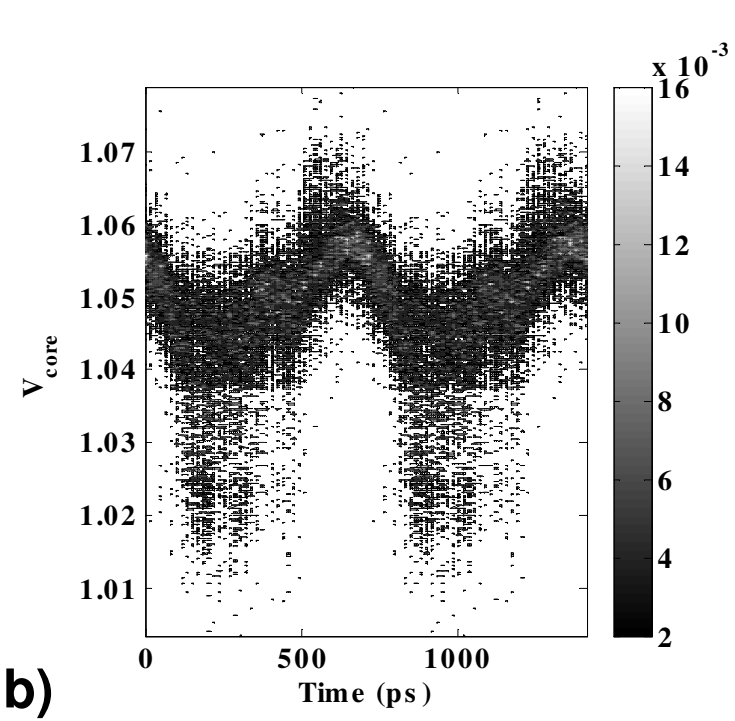
RVD Coarse Delay Element

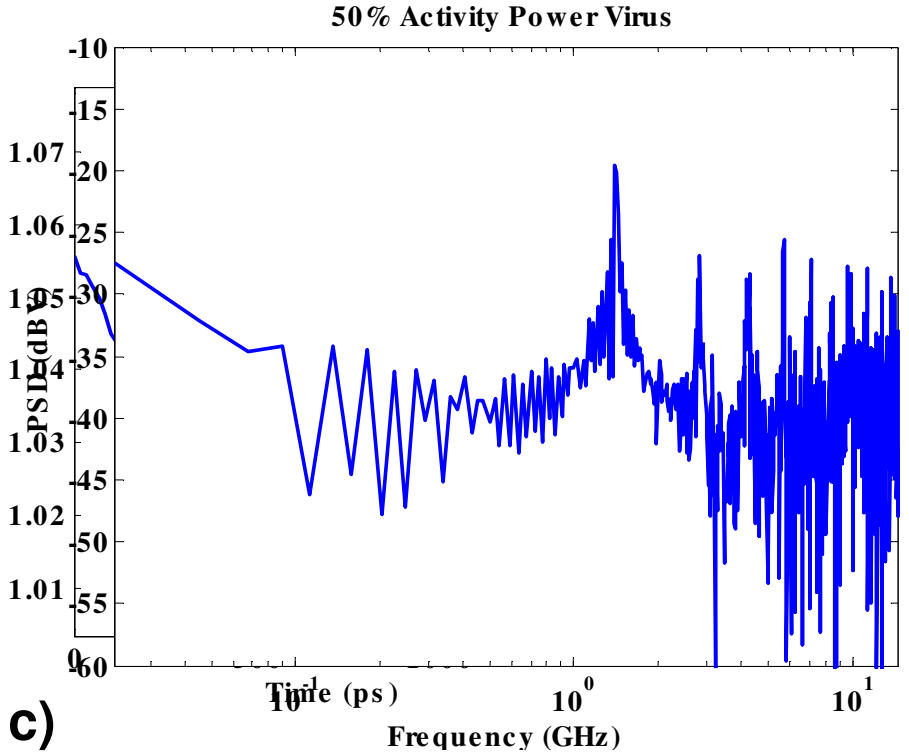


RVD Phase Comparator



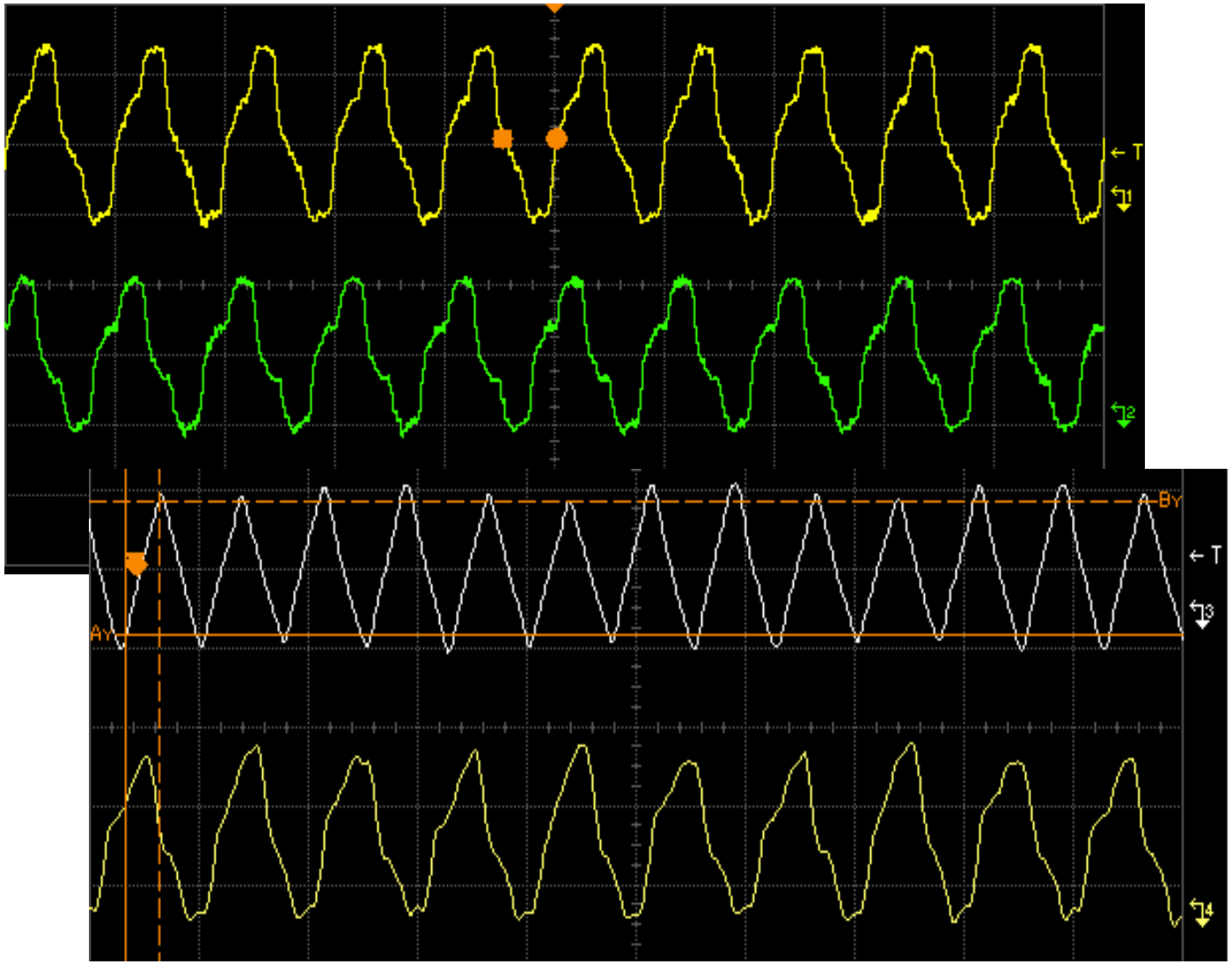






VFM Performance vs. Supply Noise

FFM/VFM Core/Bus Clock Oscilloscope Traces



FFM, 1.2V

Core clock
1.6GHz

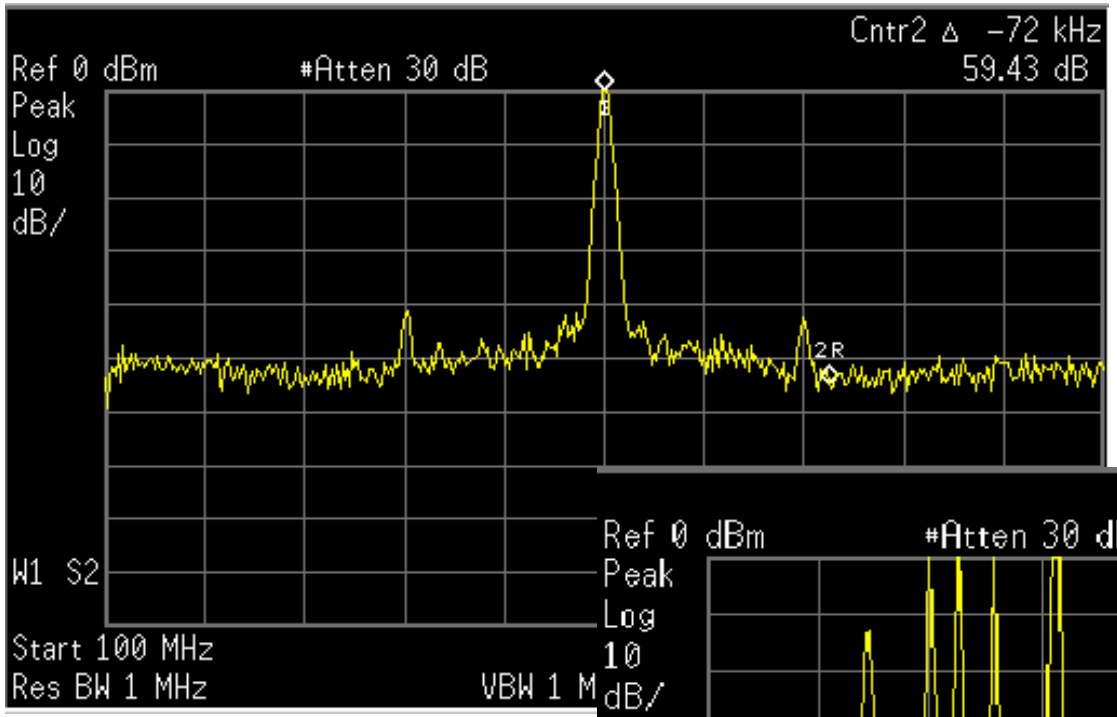
Bus Logic clock
1.6GHz

VFM, 1.2V

Core clock
2.14GHz

Bus Logic
clock 1.6GHz

Core Clock Spectral Content

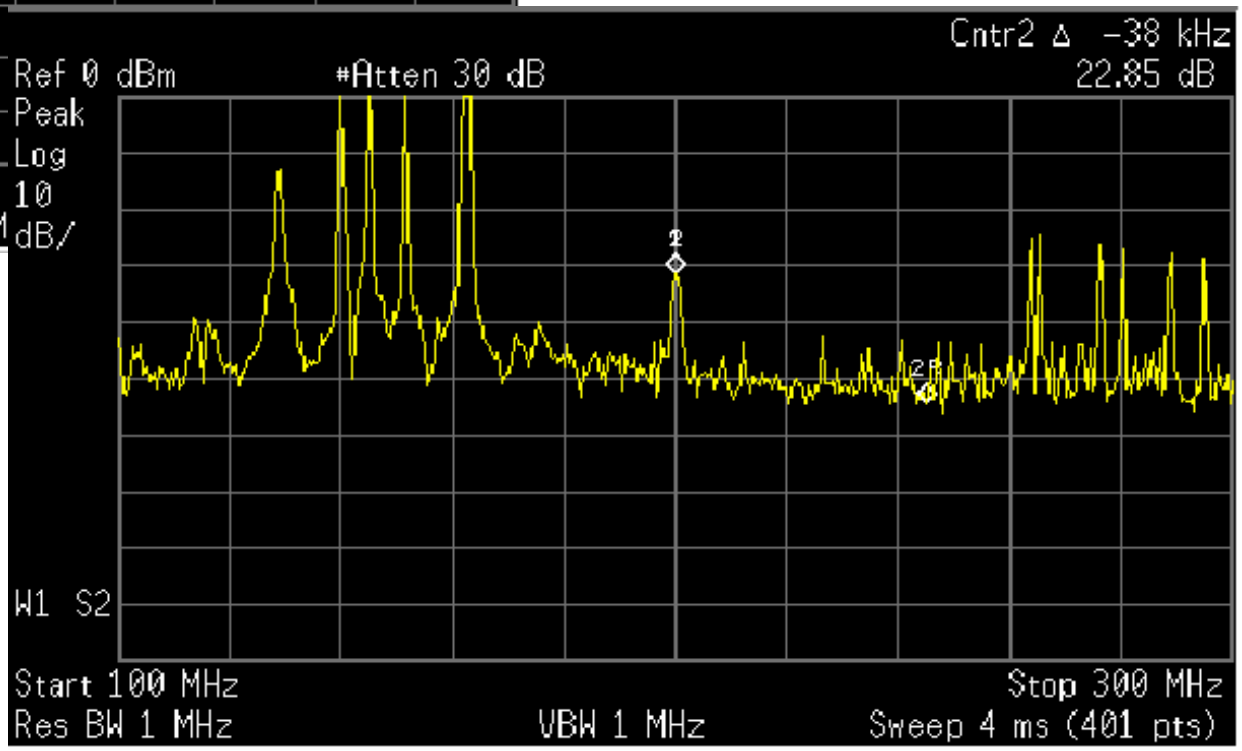


FFM

Fmax=2GHz,
Ffixed=1.6GHz,
1.2Vcore

VFM

Fmax=2GHz, 1.2
Vcore +/- 100mV,
slow RVD curve



Summary

- Clock system enables a dynamic voltage-scaling power management system (Foxton)
  - Generates low-skew fixed- and variable- frequency clocks
- High-BW Voltage-to-Frequency conversion (VFC)
  - Regional Voltage Detectors
  - Synchronized Digital Frequency Dividers
  - VFC follows programmed V/F response
  - VFC lock onto and tracks local supply voltage
    - Tracks high-BW switching transients:1 cycle VFC loop response
    - Tracks low-BW Foxton-based supply modulation
- Performance benefits through reduced guardband:
  - Fast response to switching transients (3-8%, path dependent)
  - Tracks process, temperature (3%)
- VFM operation demonstrated above 2GHz

Acknowledgements

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