16.5 A 92%-Efficiency Wide-Input-Voltage-Range Switched-Capacitor DC-DC Converter

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The traditional inductor-based buck converter has been the dominant design for step-down switched-mode voltage regulators for decades. Switched-capacitor (SC) DC-DC converters, on the other hand, have traditionally been used in low-power (<10mW) and low-conversion-ratio (<4:1) applications where neither regulation nor efficiency is critical. However, a number of SC converter topologies are very effective in their utilization of switches and passive elements, especially in relation to the ever-popular buck converters [1,2,5]. This work encompasses the complete design, fabrication, and test of a CMOS-based switched-capacitor DC-DC converter, addressing the ubiquitous 12 to 1.5V board-mounted point-of-load application. In particular, the circuit developed in this work attains higher efficiency (92% peak, and >80% over a load range of 5mA to 1A) than surveyed competitive buck converters, while requiring less board area and less costly passive components. The topology and controller enable a wide input voltage (V_{IN}) range of 7.5 to 13.5V with an output voltage (V_{OUT}) of 1.5V. Control techniques based on feedback and feedforward provide tight regulation ($30mV_{pp}$) under worst-case load-step (1A) conditions. This work shows that SC converters can outperform buck converters, and thus the scope of SC converter applications can and should be expanded.

Figure 16.5.1 shows the schematic of the Dickson SC converter [4] implemented in this work. In contrast to Dickson's original work on a voltage step-up converter, this work utilizes the Dickson topology as a step-down converter. The input voltage may range from 7.5 to 13.5V, while the converter outputs a nominal voltage of 1.5V, defined by an on-chip bandgap reference. Capacitors C_1 to C_9 are the power-train capacitors, and they are implemented with off-chip ceramic capacitors. The Dickson converter operates in 2 phases, and achieves voltage conversion through charge transfers among capacitors C_1 to C_9 [4]. Switches S_1 to S_{12} are the power switches, and the phase in which they are turned on is indicated by the number in bracket next to the switch label in the figure; the switch is turned off in the other phase. Switches S_{13} to S_{18} are also power switches, but they may turn on in either clock phase depending on the conversion ratio of the converter. For example, in order to attain a conversion ratio of 7.5 to 1, switches S_{13} and S_{15} are on while switches S_{14}, S_{16}, S_{17}, and S_{18} are off during clock phase 1, and switches S_{14} and S_{17} are on while switches S_{13}, S_{15}, S_{16}, and S_{18} are off during clock phase 2. The timing sequence of switches S_{13} to S_{18} allows the converter to attain 7 different conversion ratios, ranging from 5 to 1 to 8 to 1 with half integer steps. The integrated circuit implementation, in a 0.18µm triple-well CMOS process, is sub-divided into various voltage domains to allow the usage of low-voltage transistors (blocking a maximum of 4V) to accommodate moderate V_{IN} levels, as high as 13.5V [5].

This converter achieves regulation by adjusting its nominal conversion ratio, and by modulating the switch conductance of switches $S_{1,4,5}$ [6]. Switch conductance modulation [3] allows tight regulation for line and load variation whereas changing conversion ratio allows the converter to attain a high efficiency throughout the operating space. Furthermore, the converter modulates switching frequency to attain high efficiency at light-load conditions. Figure 16.5.2 shows the controller implemented in this converter. The control action is divided into an inner loop and an outer loop, the inner loop regulates switch conductance and switching frequency, whereas the outer loop chooses the nominal conversion ratio. Switch conductance modulation is achieved by modulating the gate drive voltage of PMOS switches $S_{1,4,5}$ using an error amplifier. The gate drive voltage, V_{GD}, is digitized using a simple flash analog-to-digital converter (ADC) and is used as a proxy for switch conductance. The inner-loop controller regulates switching frequency by slaving the clock to switch conductance. The outer-loop controller reduces conversion ratio when the switch conductance exceeds the designed maximum value (feedback action) or when V_{IN} is reduced rapidly (feedforward action). The conversion ratio is increased when ($V_{IN}/n - V_{OUT}$) is high and switch conductance is low, where n is the conversion ratio. The value ($V_{IN}/n - V_{OUT}$) is obtained by first dividing V_{IN} using a voltage divider, and then converting the result to the digital domain using a flash ADC. The voltage divider has a variable division ratio chosen to be n by the controller, and the flash ADC uses a reference voltage proportional to V_{OUT}. Auxiliary functions such as self startup, over-current protection and safe shutdown are also implemented.

Figure 16.5.3 shows the expected efficiency and measured efficiency of the converter versus I_{OUT} at around V_{IN} = 8.7V. As shown in the figure, this converter attains a peak efficiency of 92% and maintains efficiency higher than 80% over an output current range from 5mA to 1A. The efficiency of the converter reduces for I_{OUT} > ~700mA because a reduction in conversion ratio is needed to maintain regulation. When conversion ratio is reduced, ($V_{IN}/n - V_{OUT}$), which equals the voltage drop across the output-referred resistance of the converter, increases, and thus efficiency of the converter is reduced. Figure 16.5.4 shows the expected efficiency and measured efficiency of the converter versus V_{IN} with I_{OUT} at 220mA and at 50mA. As shown in the figure, this converter maintains efficiency higher than 85% from 7.5 to 13V with a nominal V_{OUT} of 1.5V. The expected efficiency curve is calculated assuming switching frequency is scaled linearly with switch conductance. Due to an approximation implemented in the frequency- modulation block, the converter may switch faster (which reduces the efficiency) or slower (which increases the efficiency) than the expected frequency. Figure 16.5.5 shows the load transient response of the converter during loading and unloading steps of 1A. On the loading transient, after first increasing switch conductances to their maximum values, the controller decreases the conversion ratio from 5.5 to 5, in order to meet the load condition. On the unloading transient, the controller immediately stops clocking, and then adjusts the conversion ratio back to 5.5 to be prepared to continue operation. Clocking is only initiated when the stored charge in the output capacitor is reduced, and the output recovers to its regulated value. The output voltage is regulated to within 30mV during the transient.

Figure 16.5.6 shows a graph comparing the peak efficiency of this converter with that of similarly rated converters. All the surveyed buck and SC converters achieve respectable efficiency, but show a general trend of reduced efficiency as conversion ratio increases. The present work shows a significant increase in efficiency when compared to similarly rated SC and buck converters. Figure 16.5.6 also shows a table that comparatively presents critical performance metrics of this work and other existing technologies. In addition to a higher peak efficiency, the reported device achieves a high efficiency for a wider range of load currents than that of other competitive designs. Peak-to-peak output-voltage transient during a full-load current step is also respectable while using similar values of input and output capacitances. This work also achieves an overall reduction in PCB area and passive component cost (data from Digikey) when compared to DC-DC converters with similar ratings. This PCB area calculation only includes that of the dominant passive components since chip PCB footprint is strongly dependent on the package chosen. The die area of this experimental converter is 11.55mm² in a 0.18µm CMOS process.

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References:

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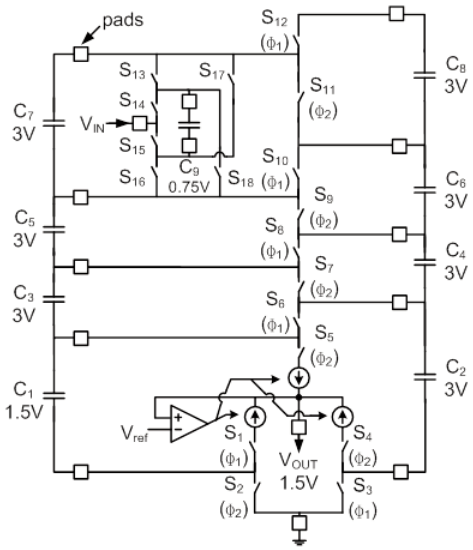


Figure 16.5.1: Circuit schematic of converter.

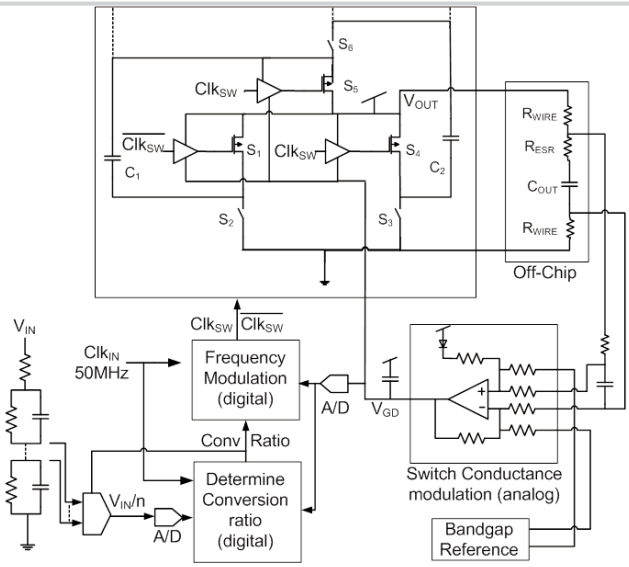


Figure 16.5.2: Overall block diagram of the controller.

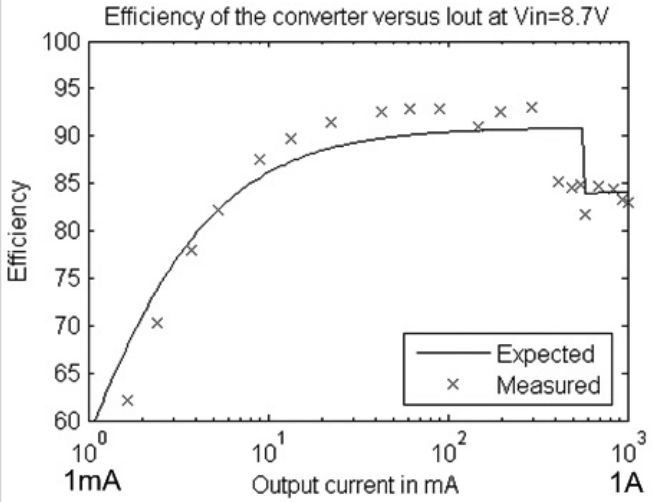


Figure 16.5.3: Efficiency versus I_{OUT} at around V_{IN}=8.7V.

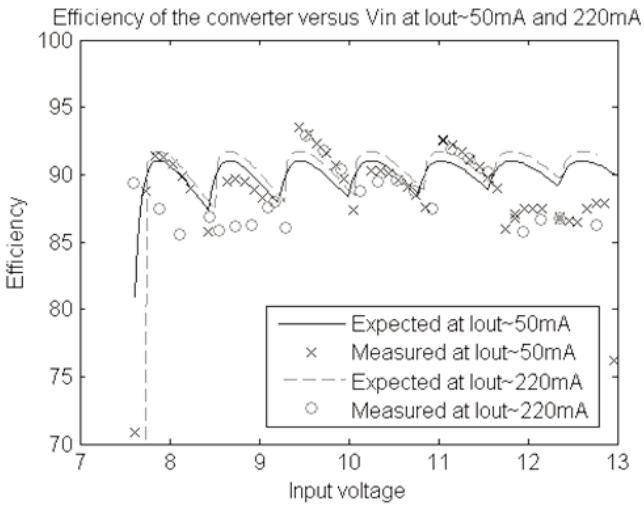


Figure 16.5.4: Expected and measured efficiency versus V_{IN} at I_{OUT}=50mA and 220mA.

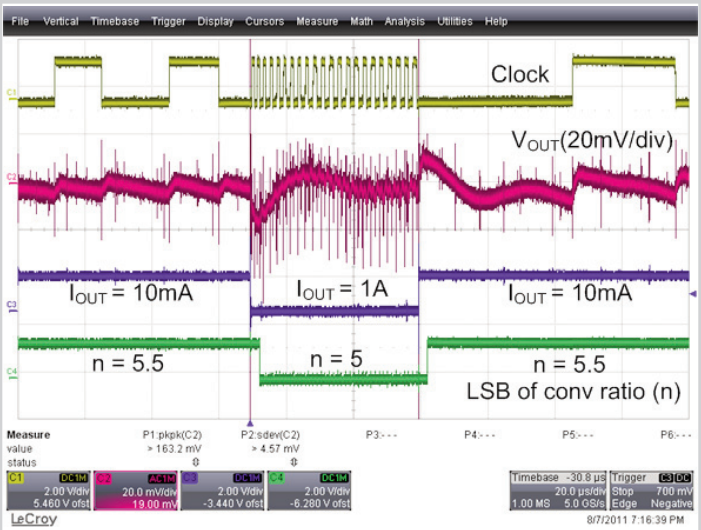
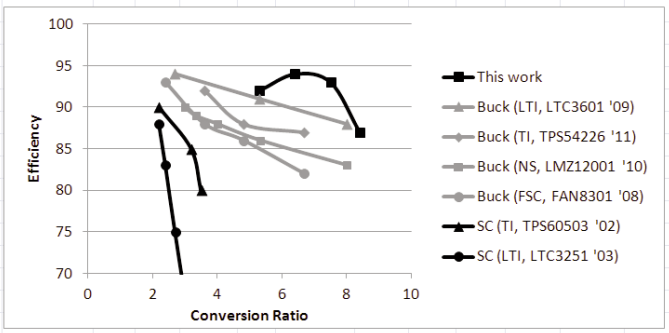


Figure 16.5.5: Oscilloscope plot of loading and unloading I_{OUT} step of 1A at V_{IN} = 9V. Time-base 20µs/div.



	V_{IN}	V_{OUT}	$I_{OUT,pk}$	Eff_{pk}	>80% eff	$tran_{pp}$	C_{IN}	C_{OUT}	Others	PCB	Cost
This work	11V	1.5V	1A	92%	5mA-1A	30mV	12µF	110µF	10µFx8	20mm^2	$1
SC TI '02	5V	1.5V	0.25A	85%	2-200mA	50mV	2.2µF	10µF	1µFx2	3.6mm^2	$0.10
SC LTI '03	5V	1.5V	0.5A	60%	-	50mV	1µF	10µF	1µFx2	2.7 mm^2	$0.10
buck NS '10	12V	1.5V	1A	83%	0.35A-1A	40mV	10µF	100µF	10µH	57 mm^2	$1
buck LTI '09	12V	1.8V	1.5A	88%	20mA-	100mV	22µF	22µF	2.2µH	27 mm^2	$1.20
buck FSC '08	12V	1.8V	2A	82%	0.4A-1.3A	500mV	10µF	22µF	15µH	57 mm^2	$1.70
buck TI '11	12V	1.8V	2A	87%	40mA-2A	30mV	20µF	44µF	2.2µH	30 mm^2	$1.50

Figure 16.5.6: Comparison between this work and similar works.

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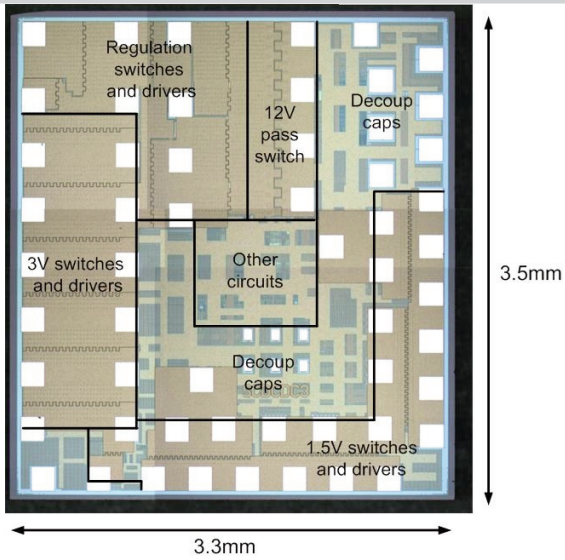

Figure 16.5.7: Die Photo.

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