95GHz Receiver with Fundamental Frequency VCO and Static Frequency Divider in 65nm Digital CMOS

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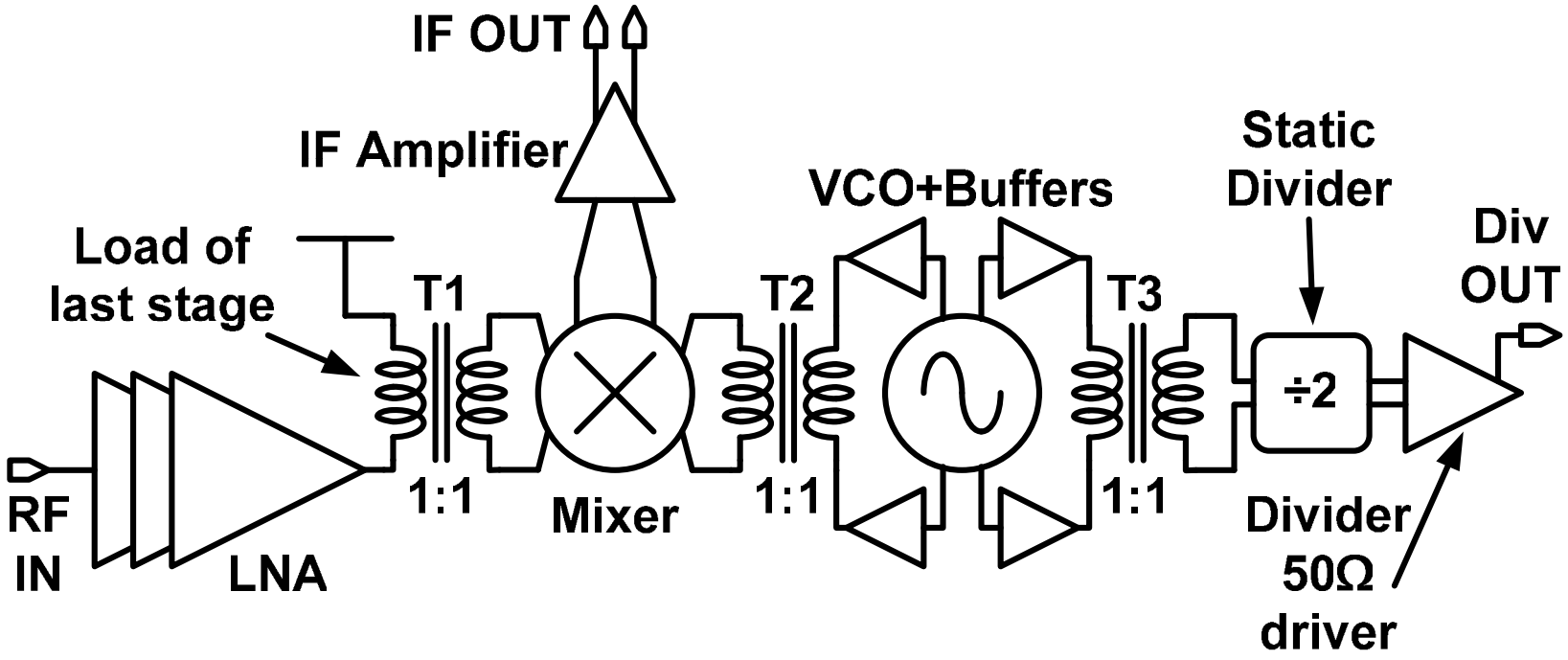
Outline

- Motivation
- Circuit schematics
- Fabrication technology and passives
- Test setup
- Measurement results
- Conclusion

Motivation / Applications

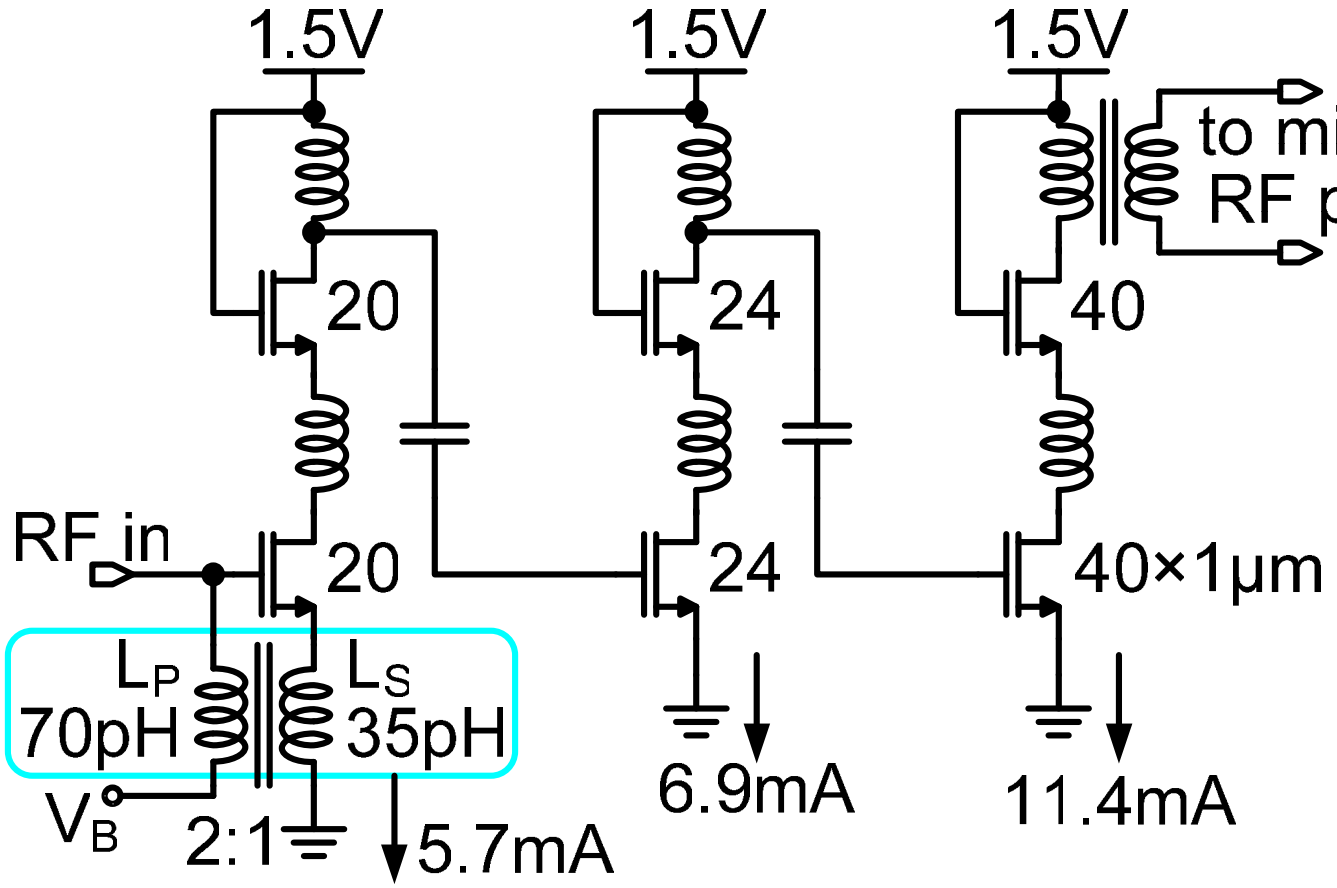
- DSB imaging / remote sensing receiver
- Receiver for 10+Gb/s data-rate communication
- Explore the capabilities of 65-nm CMOS
  - W-band operation
  - Technology scaling
  - System integration
- Higher frequency → better range resolution

Receiver Block Diagram

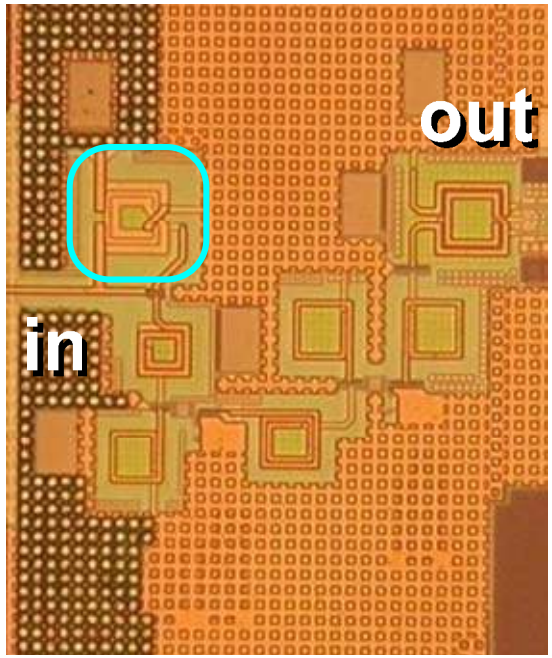


- Fundamental-frequency VCO at 90GHz
  - Fewer spurs on die
- Transformer-based signal distribution
  - Low-loss, no DC power, small size
  - Single-ended to differential conversion
  - Bias & supply plane isolation

Transformer-Feedback LNA



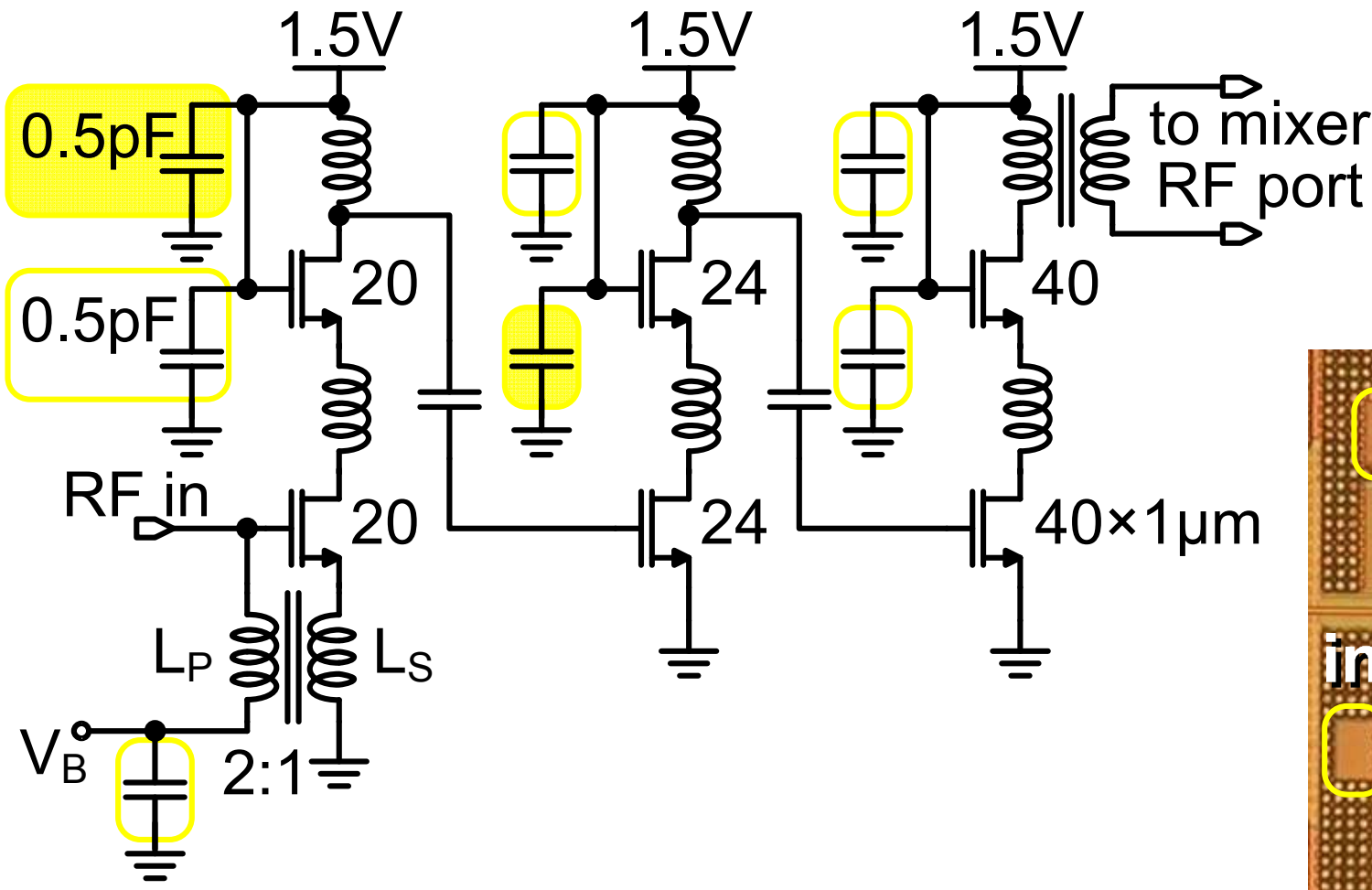
[K.W. Tang, CICC '07]



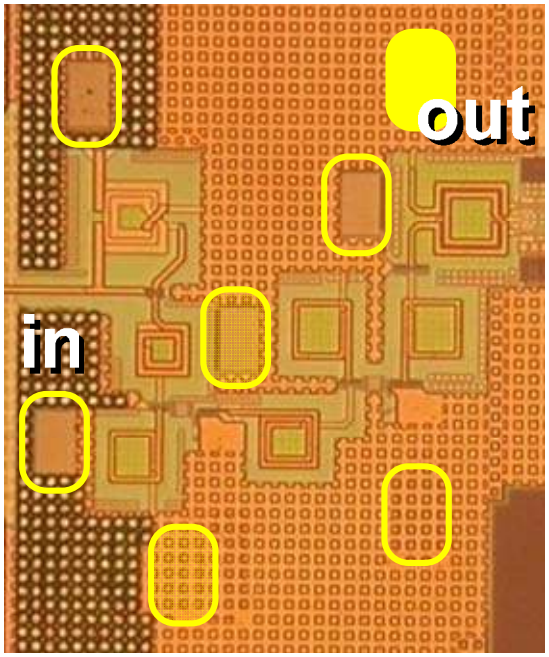
- Transistor biased at J_{SOPT}, sized to match R_{SOPT}
- Transformer chosen to match Z_{IN}
- Smaller devices for 50Ω match

$$\mathrm{Re}(Z_{IN}) = \frac{\sqrt{L_P}}{g_m k \sqrt{L_S}}$$

Transformer-Feedback LNA

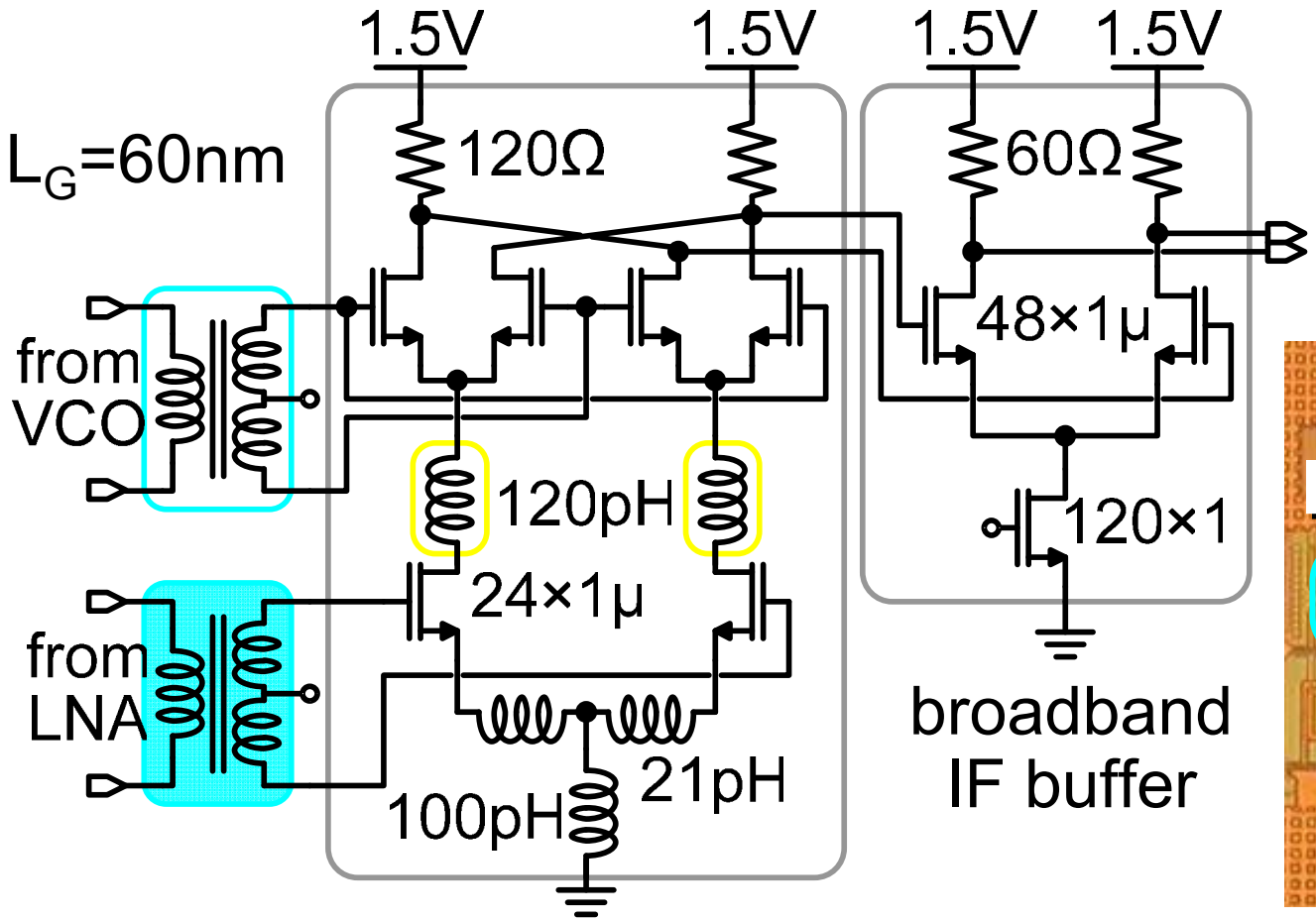


[K.W. Tang, CICC '07]

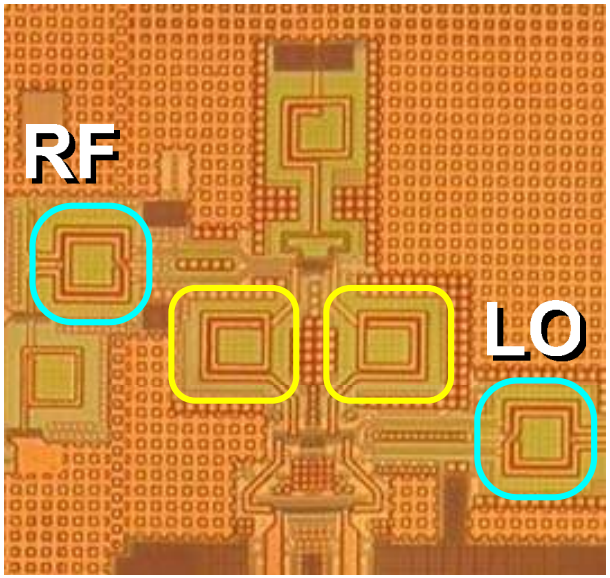


- 0.5pF decoupling at every bias node in layout
- Provides a low-L short-circuit at these nodes

Mixer and IF Buffer



[D. Alldred, CSICS '06
K.W. Tang, CICC '07]



- 76-95GHz Gilbert cell mixer
- 120pH inductors → NF & 2nd harmonic LO reject
- Biasing through transformer center tap

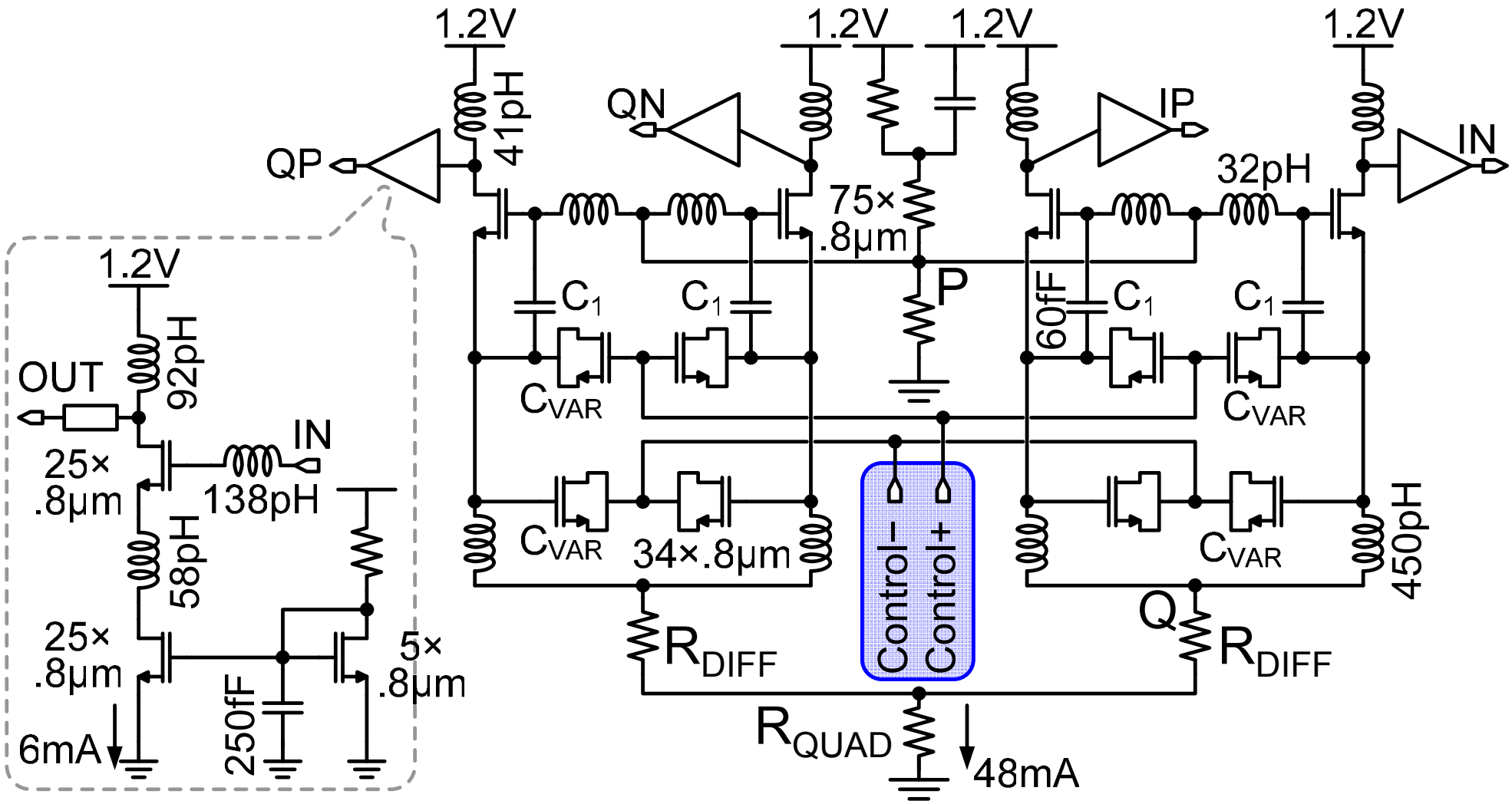
VCO Topology

- Need: VCO at 90 GHz fundamental
  Low phase noise
  High output power
  Distribute signal to mixer and divider
- From [K.W. Tang, CSICS'06]:

77 GHz	Cross-coupled	Colpitts VCO
$FOM = \left(\frac{f_{OSC}}{\Delta f}\right)^2 \frac{P_{OUT}}{L[\Delta f] P_{DC}}$	137.5	168.5

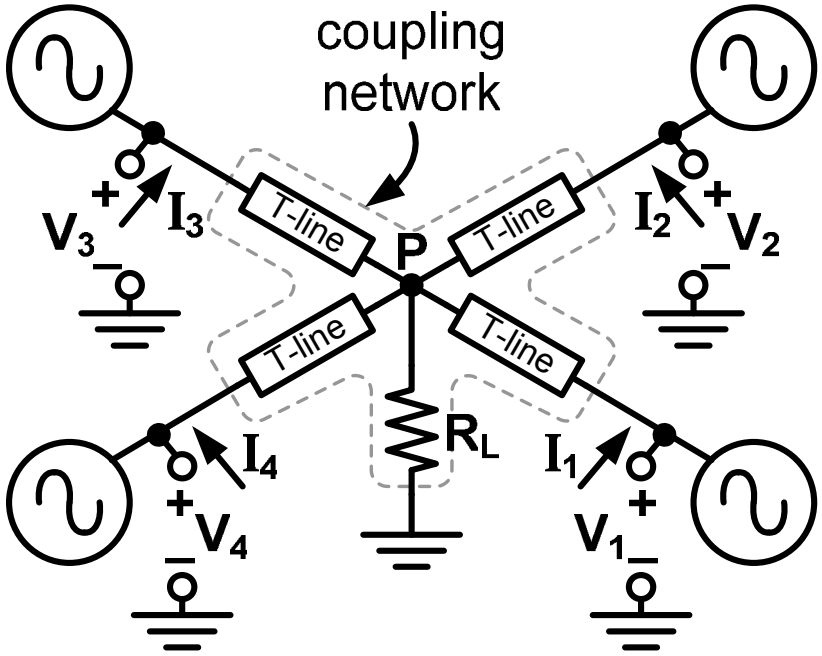
- Choose: Quadrature Colpitts VCO at 90 GHz
  Buffers to equalize tank loading

VCO Schematic

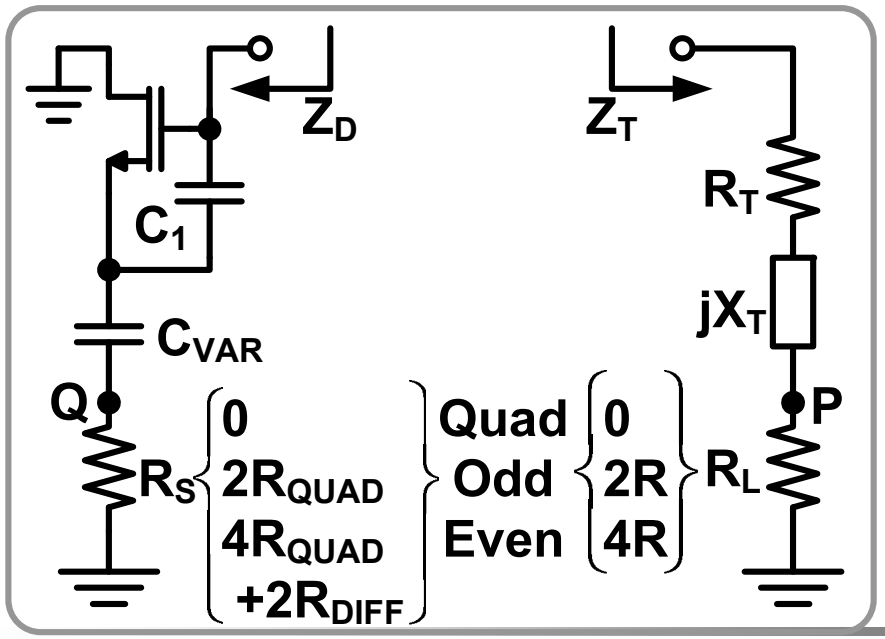


- 4 symmetrically coupled Colpitts VCOs
- VCO core: 0.2mA/µm, buffers: 0.3mA/µm

VCO Analysis



$$\begin{bmatrix} Z_{11} & Z_{12} & Z_{13} & Z_{12} \\ Z_{12} & Z_{11} & Z_{12} & Z_{13} \\ Z_{13} & Z_{12} & Z_{11} & Z_{12} \\ Z_{12} & Z_{13} & Z_{12} & Z_{11} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} = \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix}$$



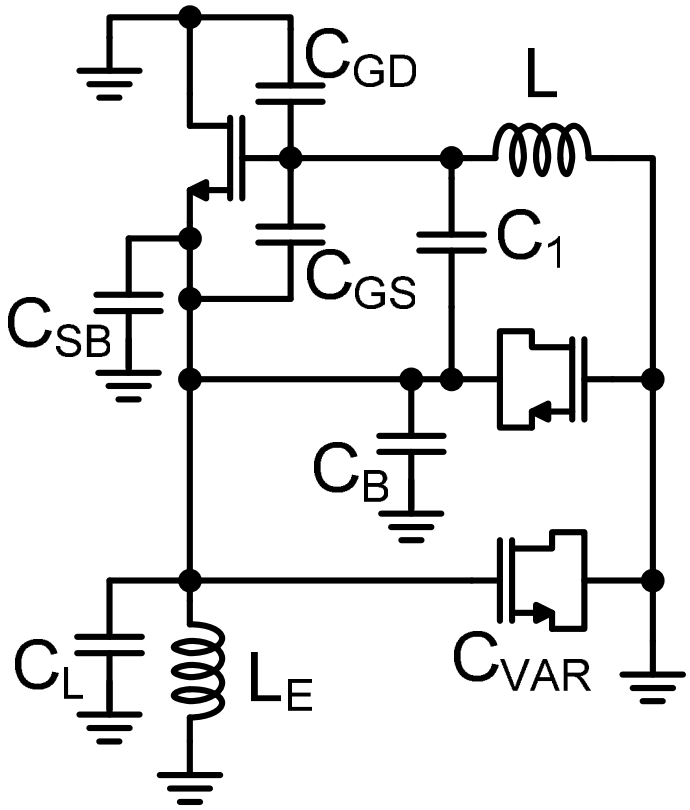
- Solution for quadrature oscillation mode:

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} = \begin{bmatrix} 1 \\ e^{j\frac{\pi}{2}} \\ e^{j\pi} \\ e^{j\frac{3\pi}{2}} \end{bmatrix} \qquad \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} = \begin{bmatrix} 1 \\ e^{-j\frac{\pi}{2}} \\ e^{-j\pi} \\ e^{-j\frac{3\pi}{2}} \end{bmatrix}$$

Colpitts VCO Frequency

$$\frac{1}{f_{OSC}} = 2\pi\sqrt{L\left(C_{GD} + \frac{(C_1 + C_{GS})(2C_{VAR} + C_{SB} + C_B + C_L)}{(C_1 + C_{GS}) + (2C_{VAR} + C_{SB} + C_B + C_L)}\right)}$$

- C_1=60fF, L=32pH
- NFET: 72×0.8μm×60nm
  - C_{GS}'=0.75fF/μm
  - C_{GD}'=0.4fF/μm
  - C_{SB}'=0.65fF/μm
- Varactor: 34×0.8μm×60nm
  - C_{VAR}=24fF → 41fF
  - C_B'=0.7fF/μm
  - C_L=3fF

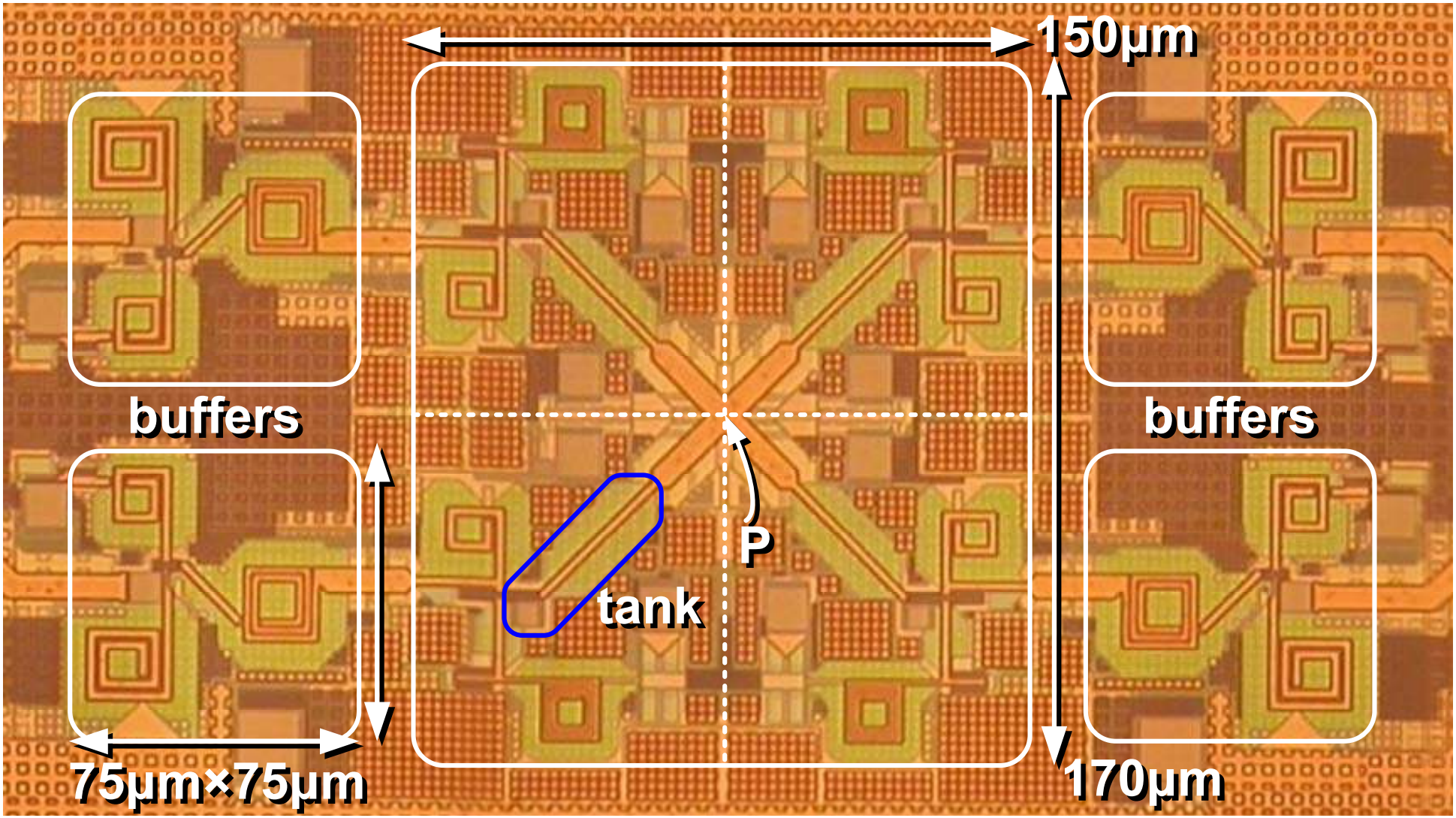


Colpitts VCO Frequency

f_{osc}	Upper limit	Lower limit
Hand analysis	101 GHz	96.7 GHz
Simulated (no extraction)	107.2 GHz	100.2 GHz
Simulated (with extraction)	91.5 GHz	88.4 GHz
Measured	91.2 GHz	88.2 GHz

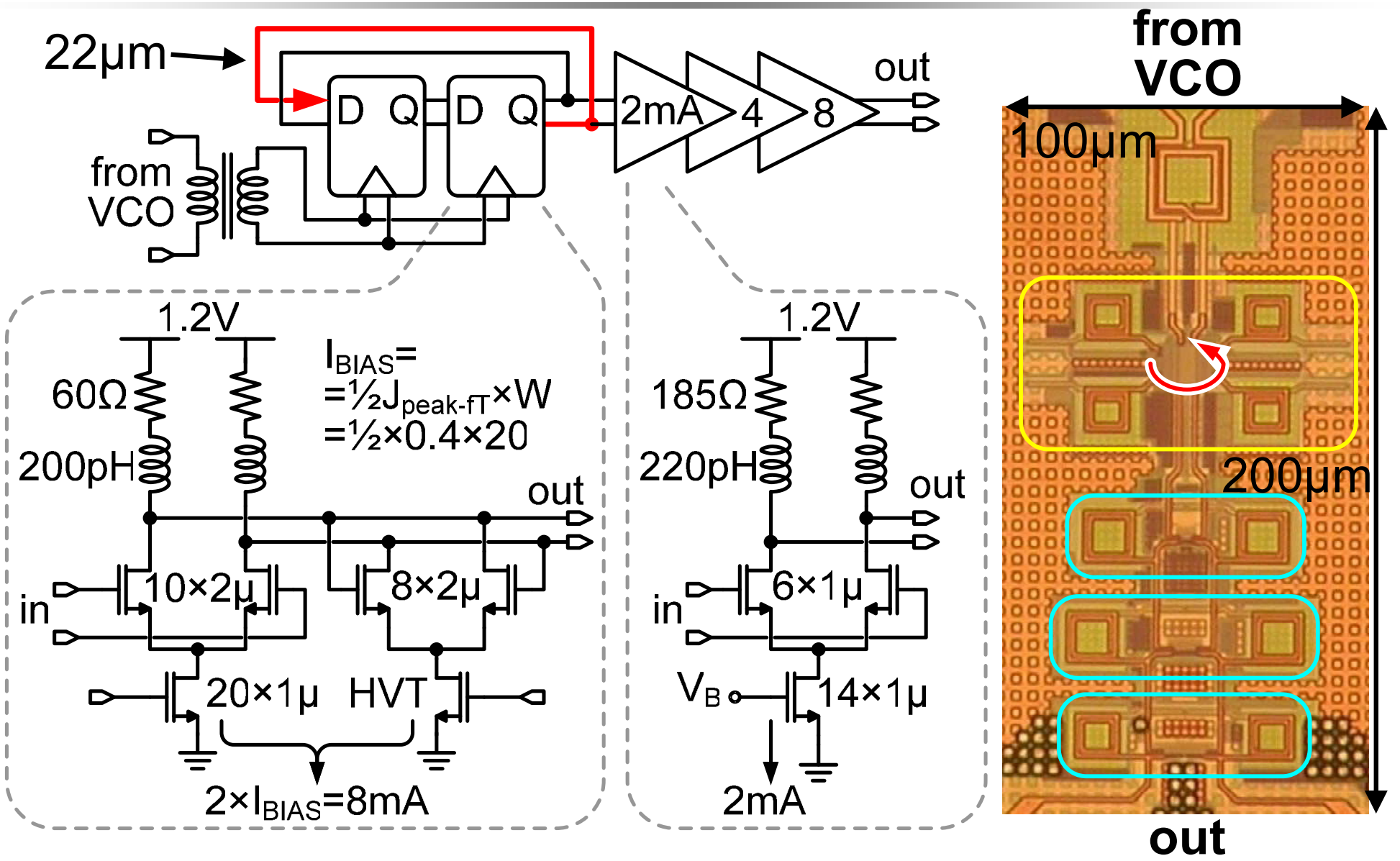
- Accurate prediction by hand analysis
- Agreement between simulated & measured f_{OSC}

VCO and Buffers



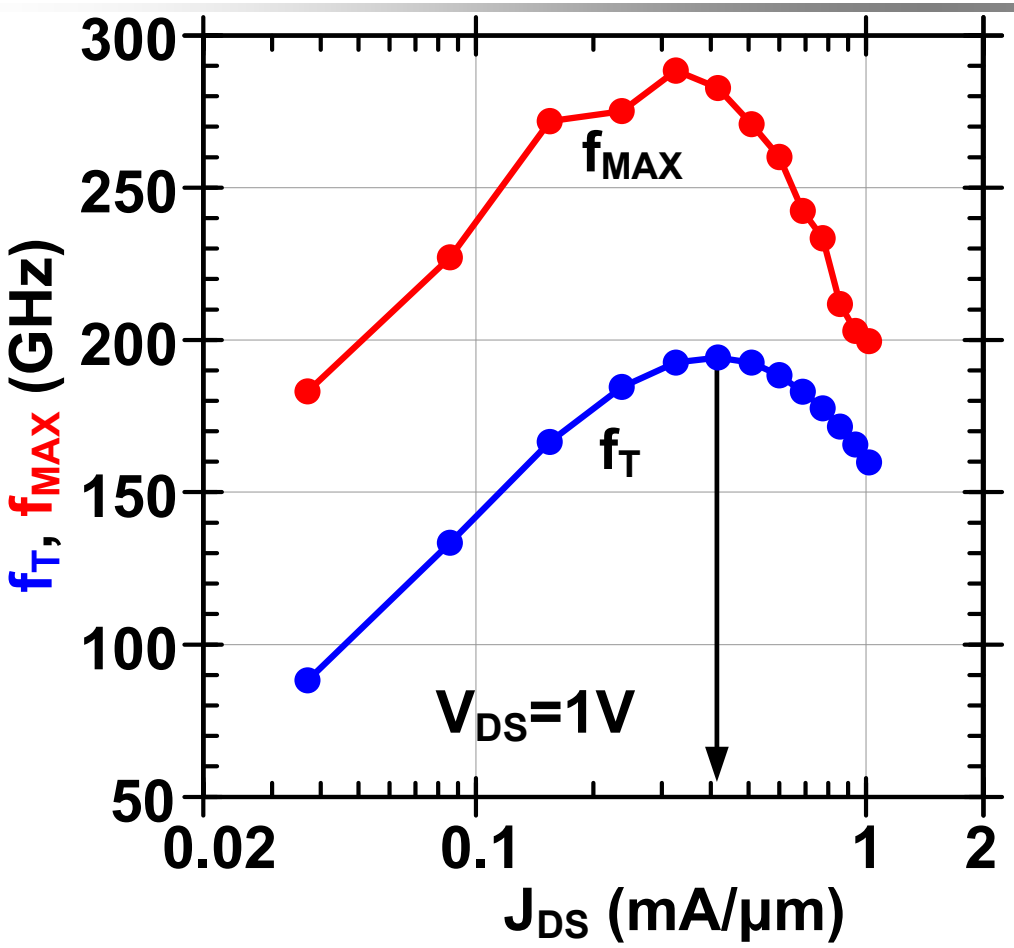
- Symmetry is maintained throughout VCO

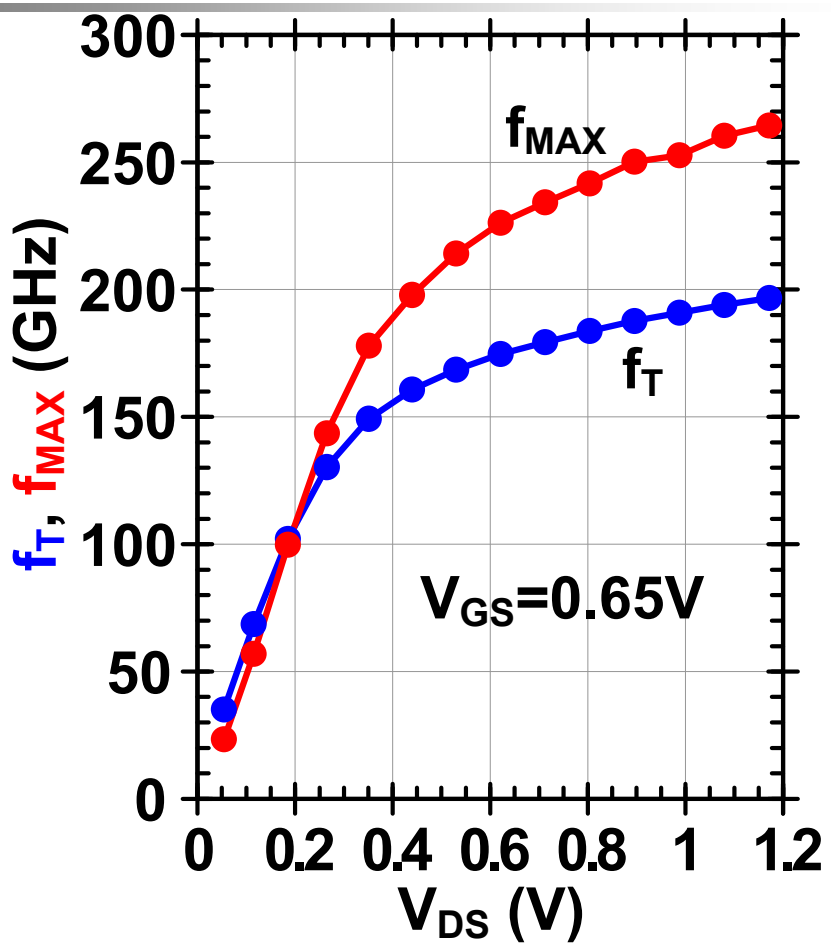
Frequency Divider



- Layout designed to minimize critical path delay

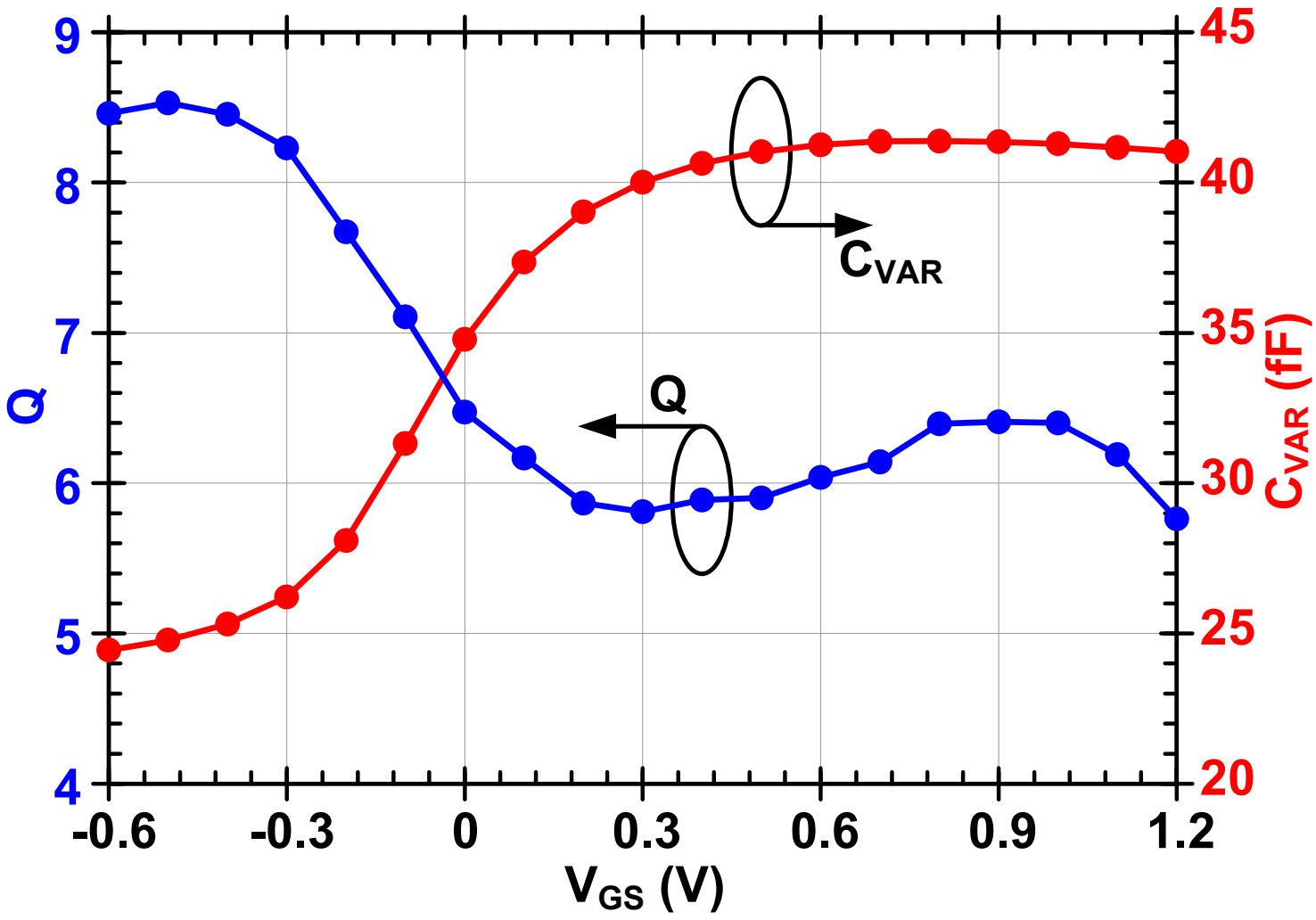
Technology – 65nm GP CMOS

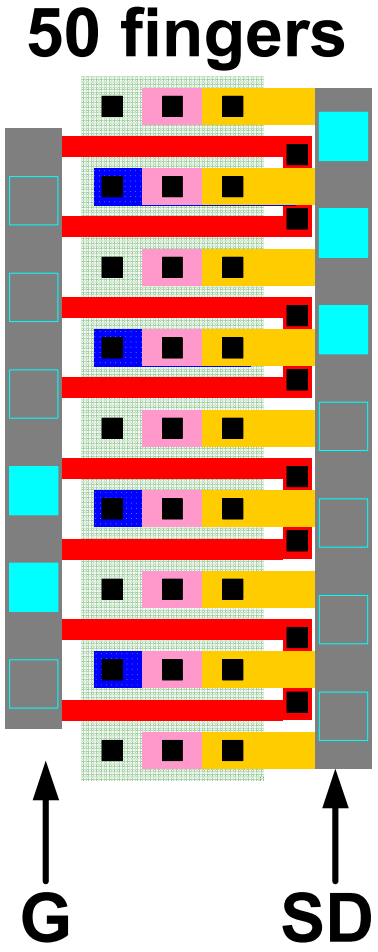




- f_{MAX}=280GHz, f_T=195GHz
- Device: 80×60nm×1μm, one side gate contact
- 7 metal backend, Metal-Over-Metal capacitors

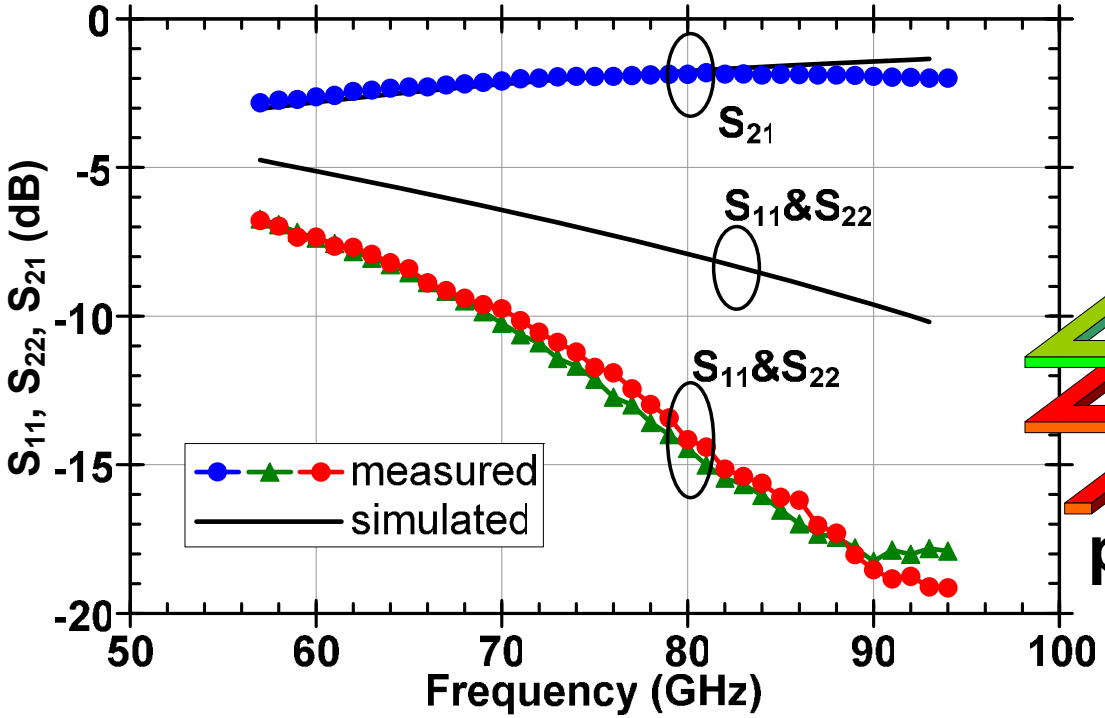
Measured varactor at 94 GHz

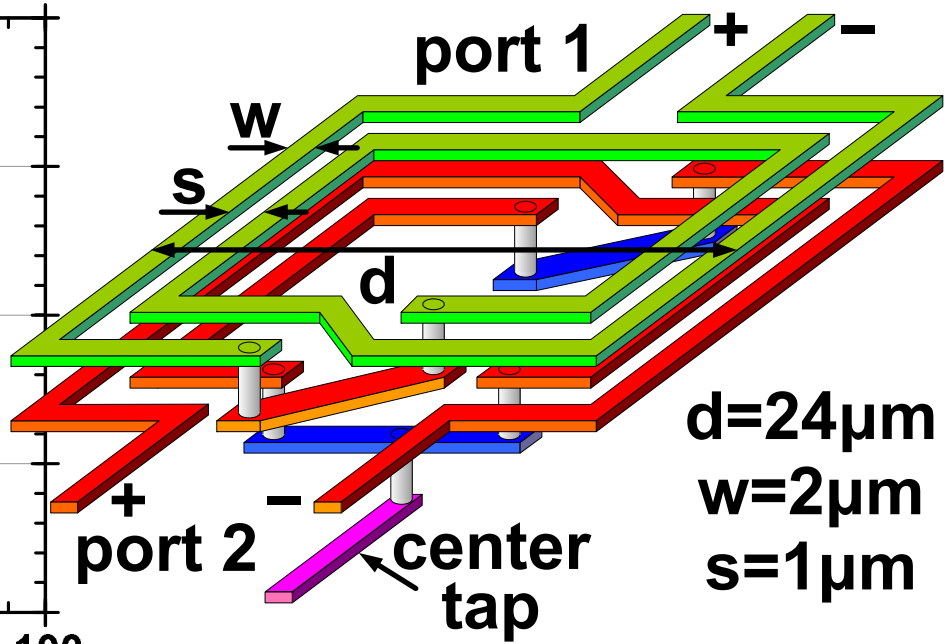




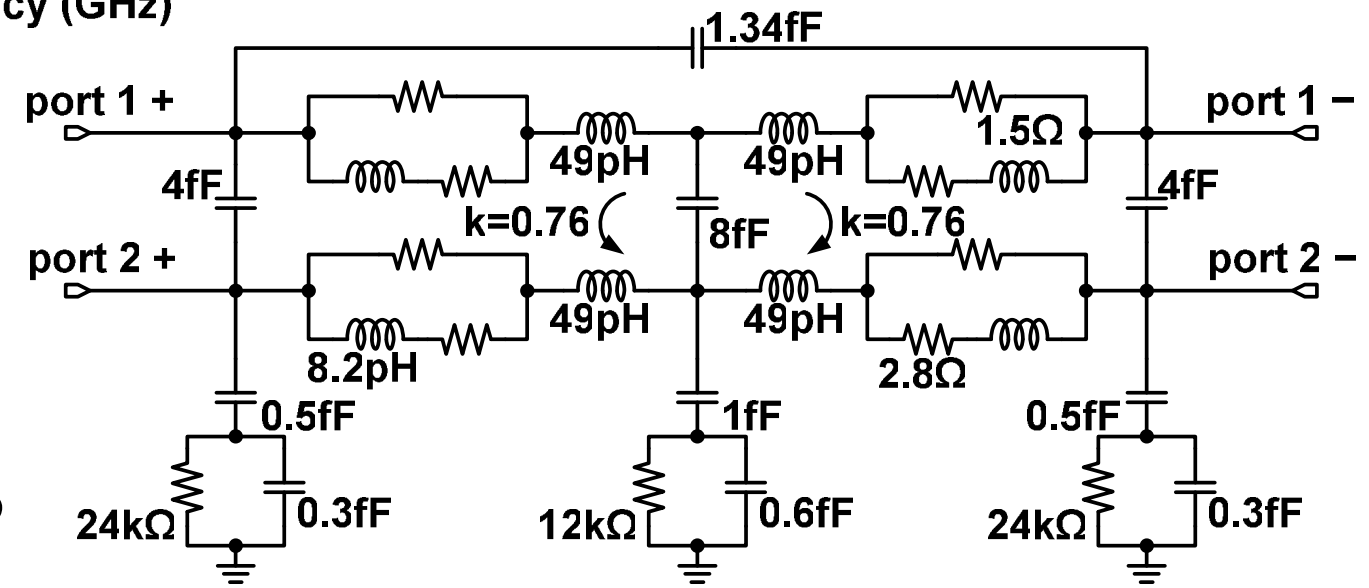
- L_G=60nm, W_{total}=27.5µm, C_{VAR}'=1.53fF/µm^2
- C variation: 25fF – 42fF, Q: 6 – 8 at 94 GHz

Measured 24-µm 1:1 transformer

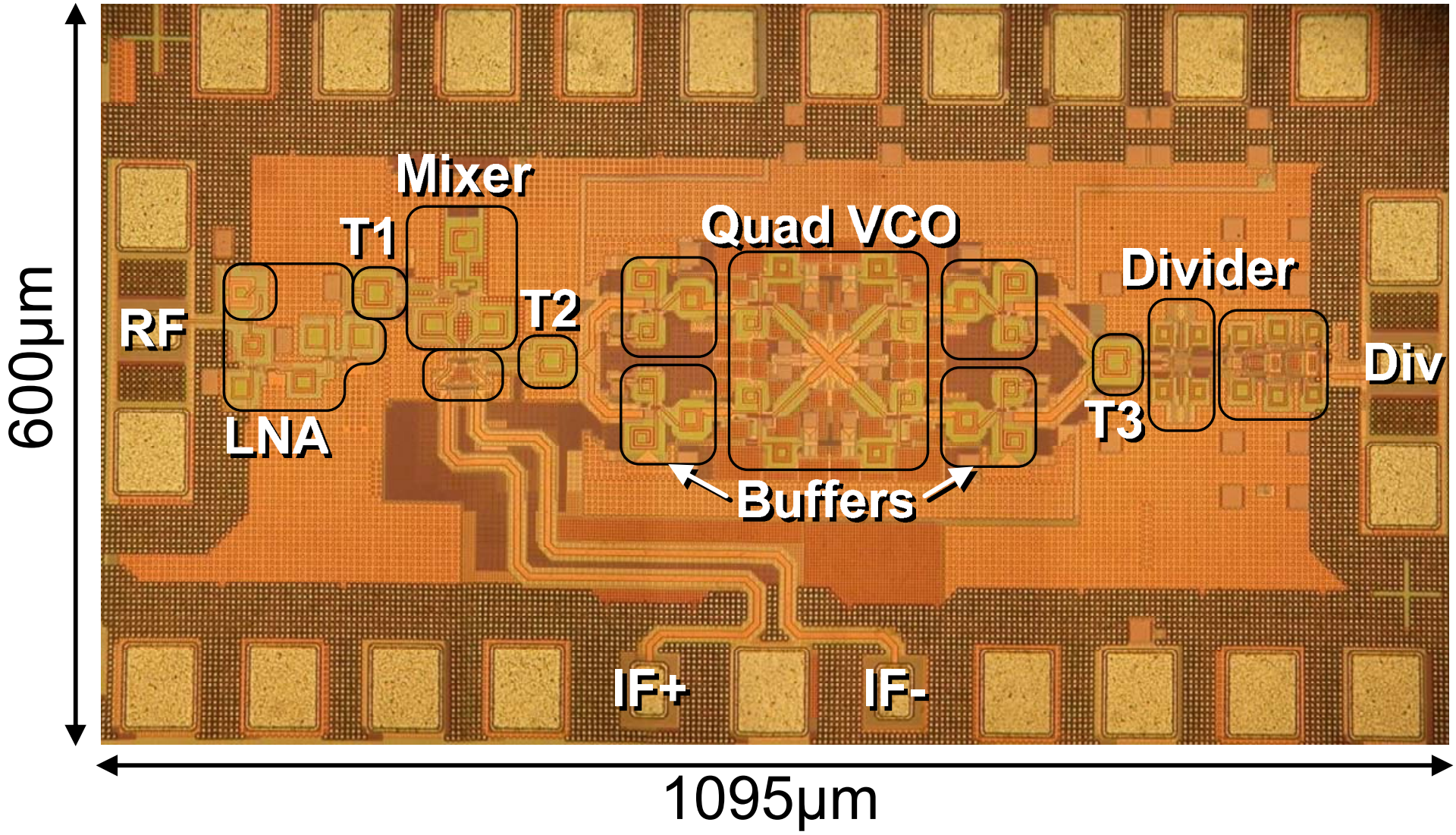




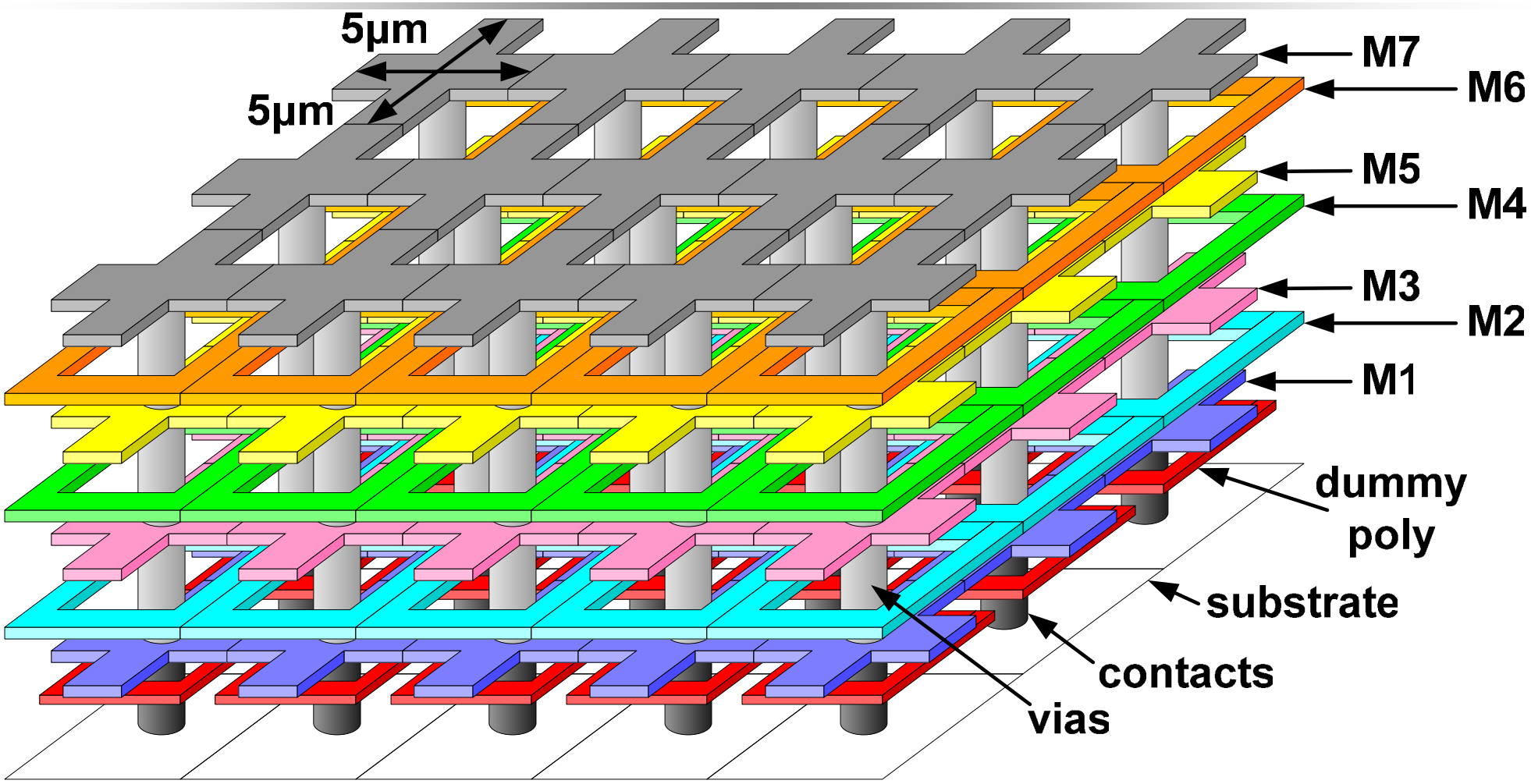
- Transformer:
  - VCO & Div
  - VCO & Mixer
  - LNA & Mixer
- MAG < -1.5dB



Receiver Die Photo

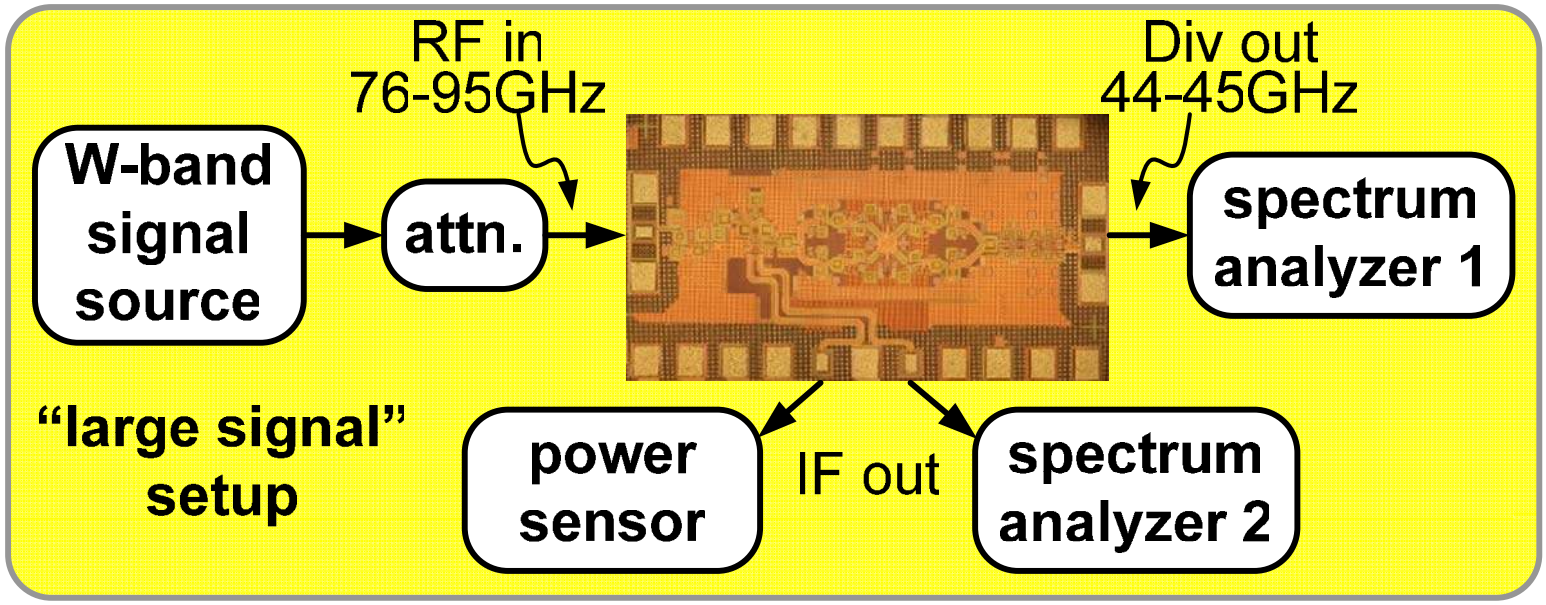


Bias Distribution

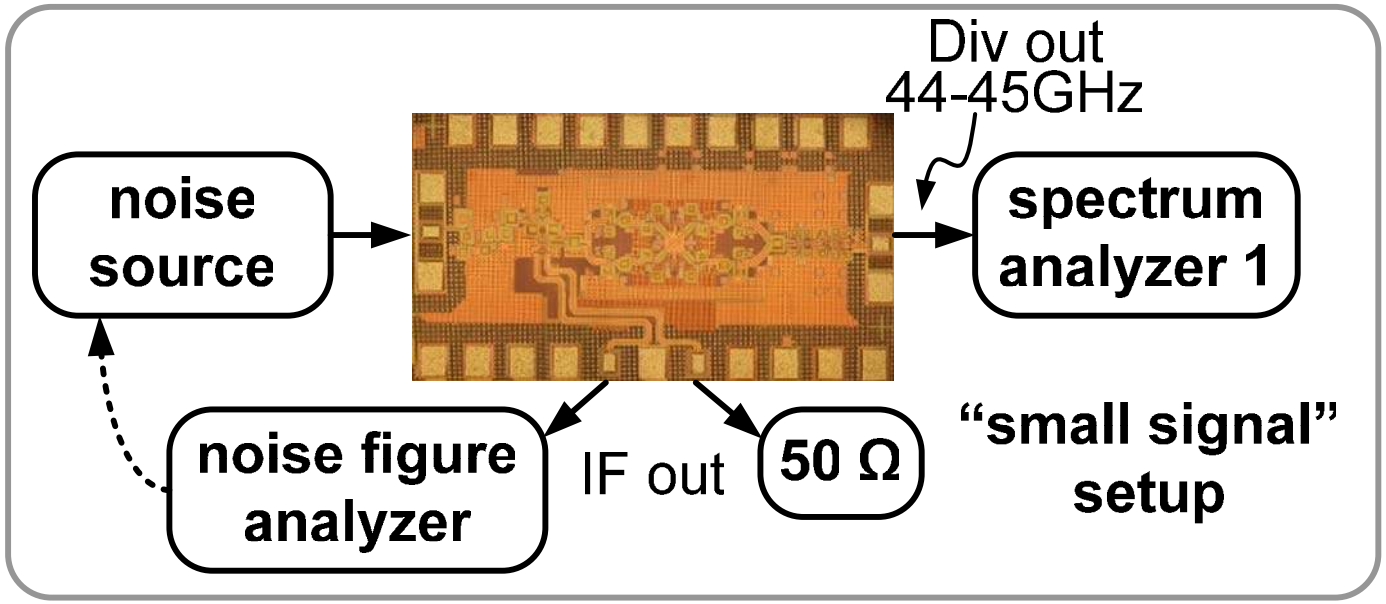


- Metal mesh distributes ground, V_{DD}, bias to all cells
- Substrate contacts, distributed decoupling, low R, L
- Meets all density rules

Measurement Setup



- SSB gain
- Linearity
- Phase noise
- Tuning range
- Divider

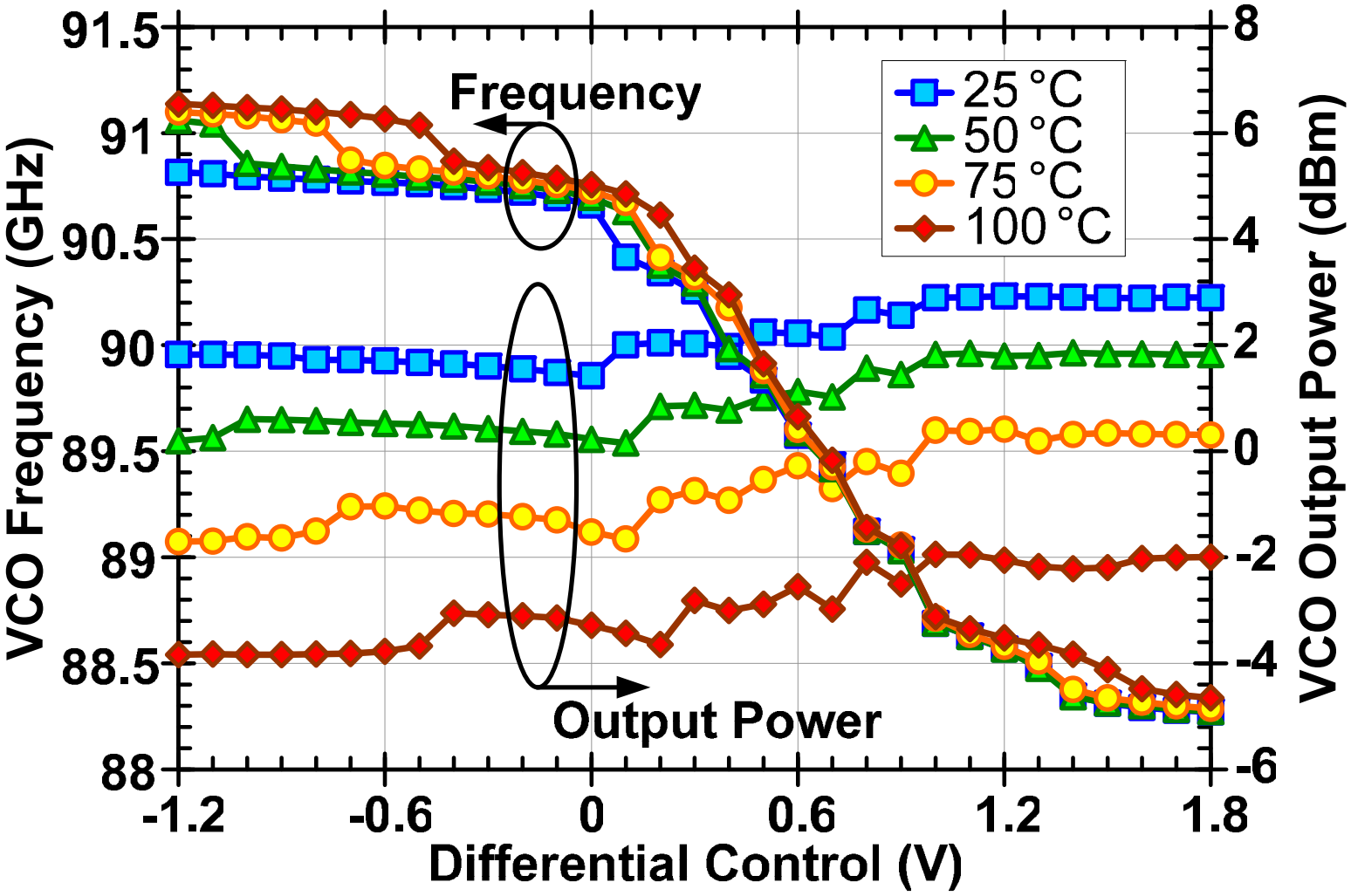


- DSB NF
- DSB gain

DC Power Consumption

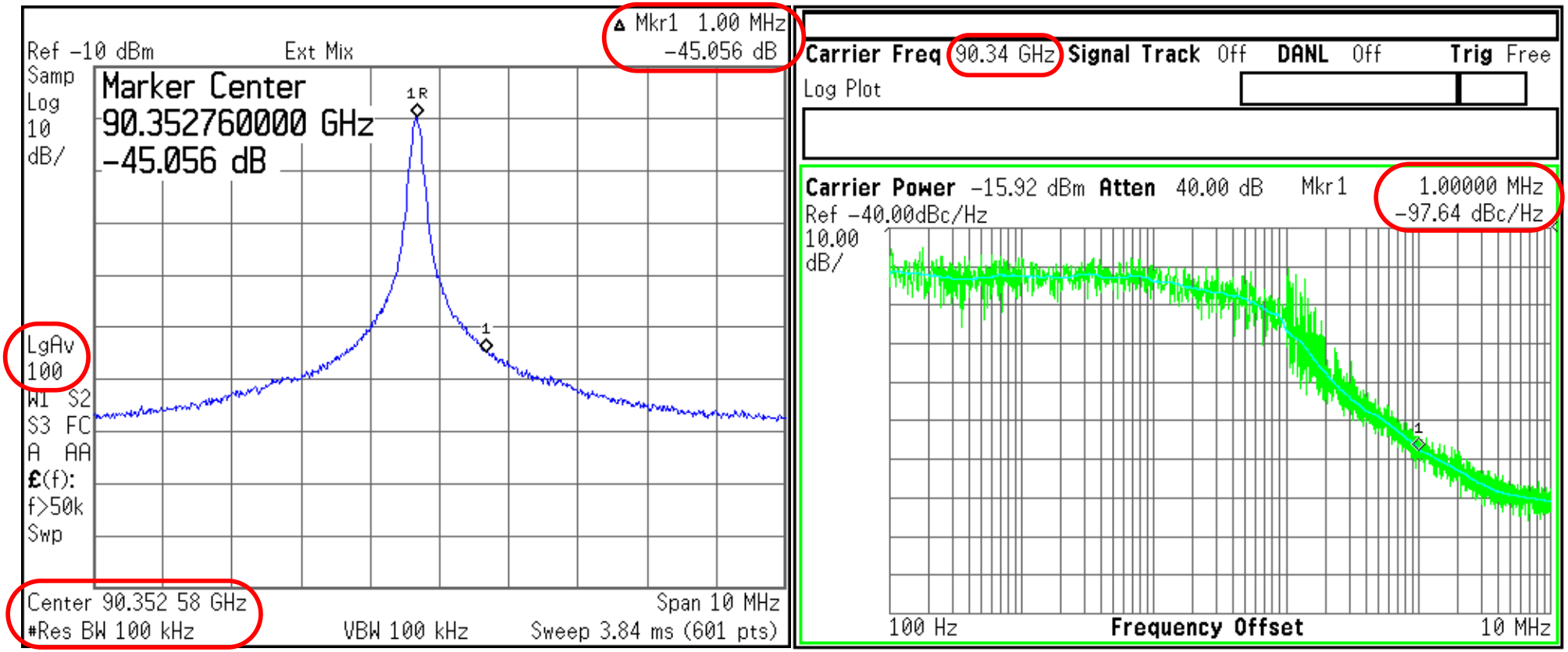
Block	Current (mA)	Supply (V)	Power (mW)
LNA	24	1.5	36
Mixer	9		13.5
50-Ω IF amplifier	19		28.5
Quadrature VCO	48	1.2	57.6
4 VCO buffers	24		28.8
Divider	18.6		22.4
Divider 50-Ω driver	16.3		19.6
Total:			206.4 (158)

VCO Tuning & Output Power



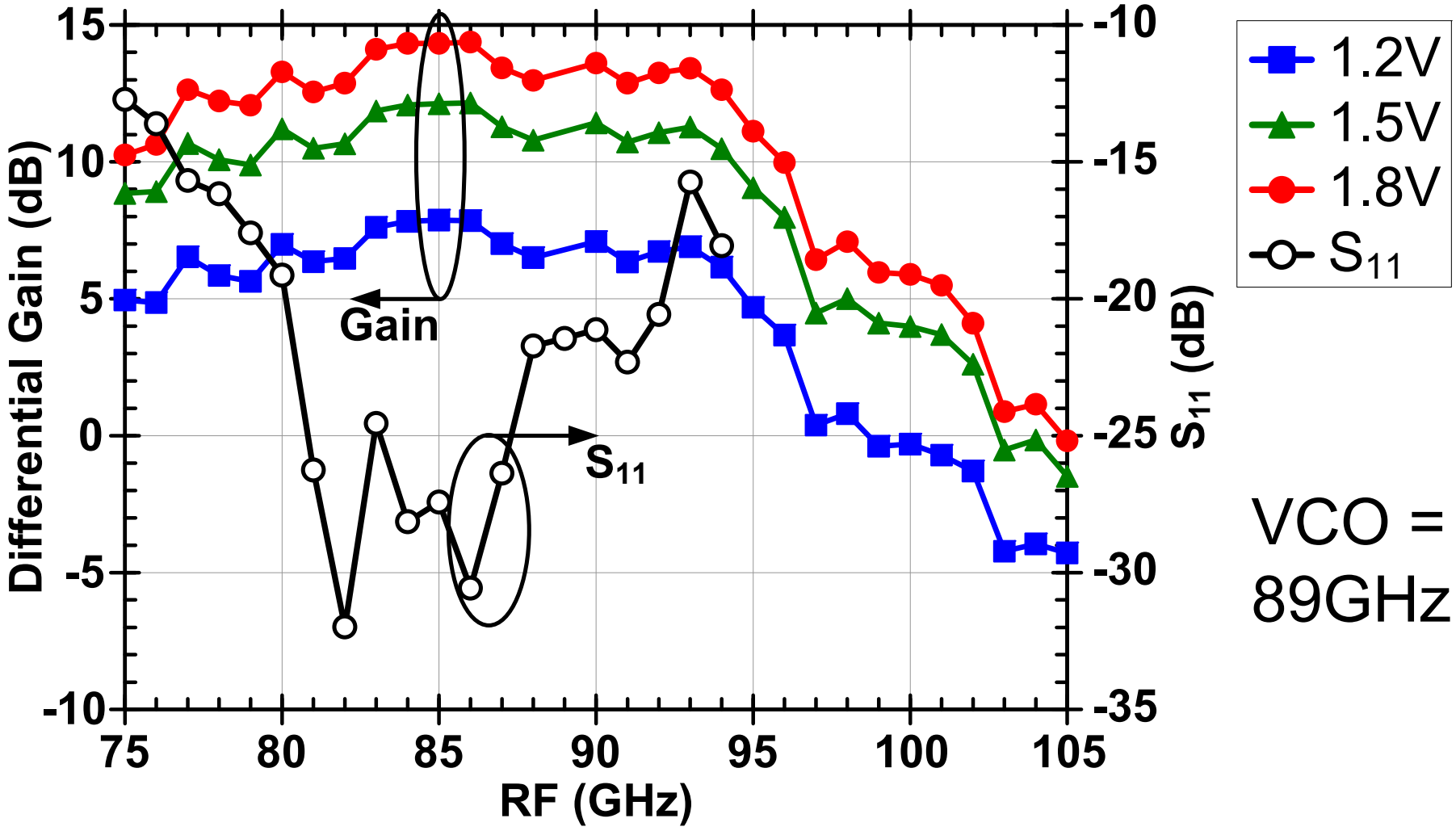
- 88.2 – 91.2GHz tuning range for all temperatures
- +3dBm to -4dBm total VCO output power

Measured VCO Phase Noise



- -95dBc/Hz at 1MHz offset
- Measured at 90.3GHz
- 100 averages

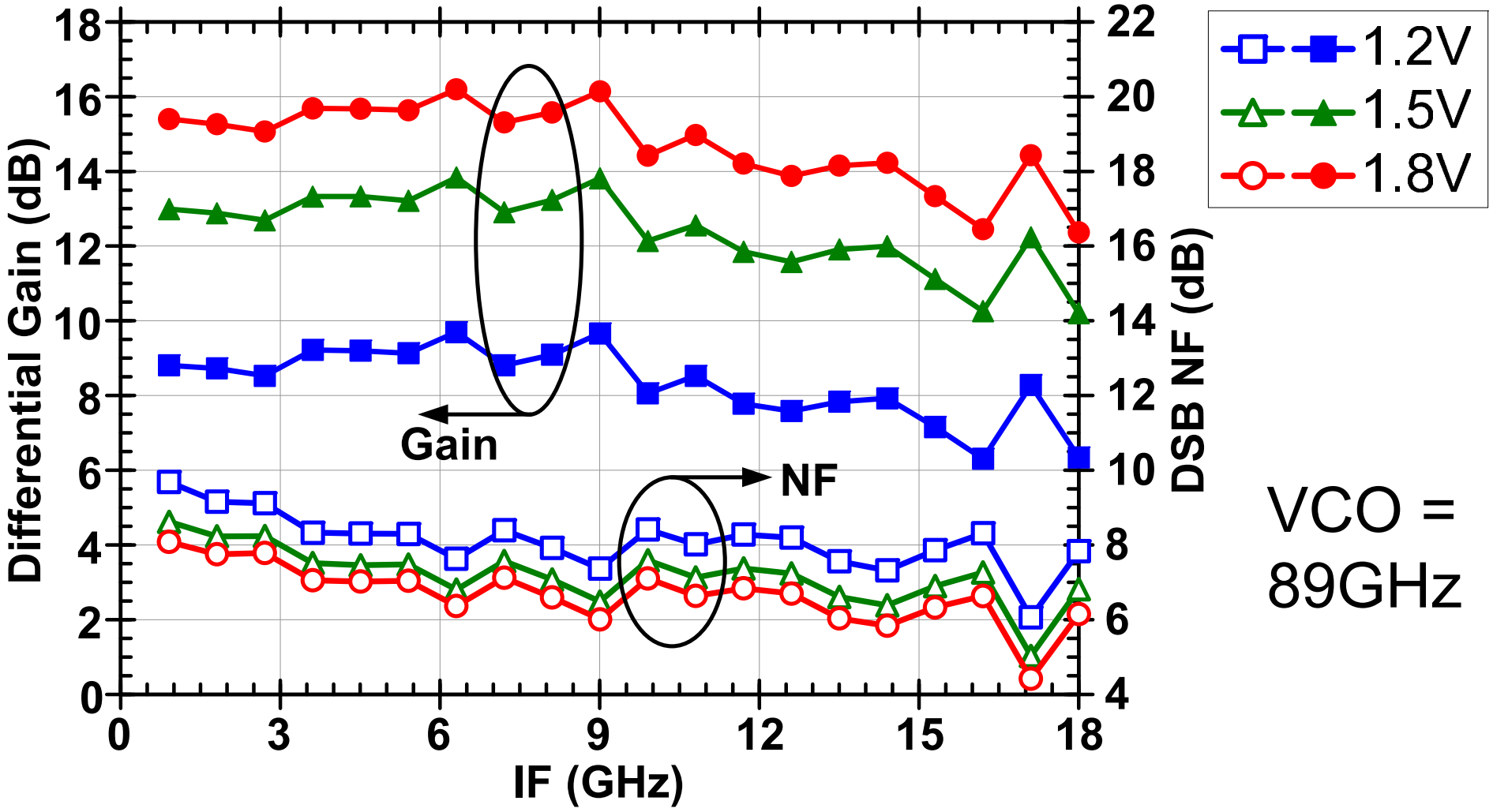
SSB Receiver Conversion Gain



VCO = 89GHz

- 12 dB differential gain with nominal bias
- S_{11} better than -15 dB over the BW

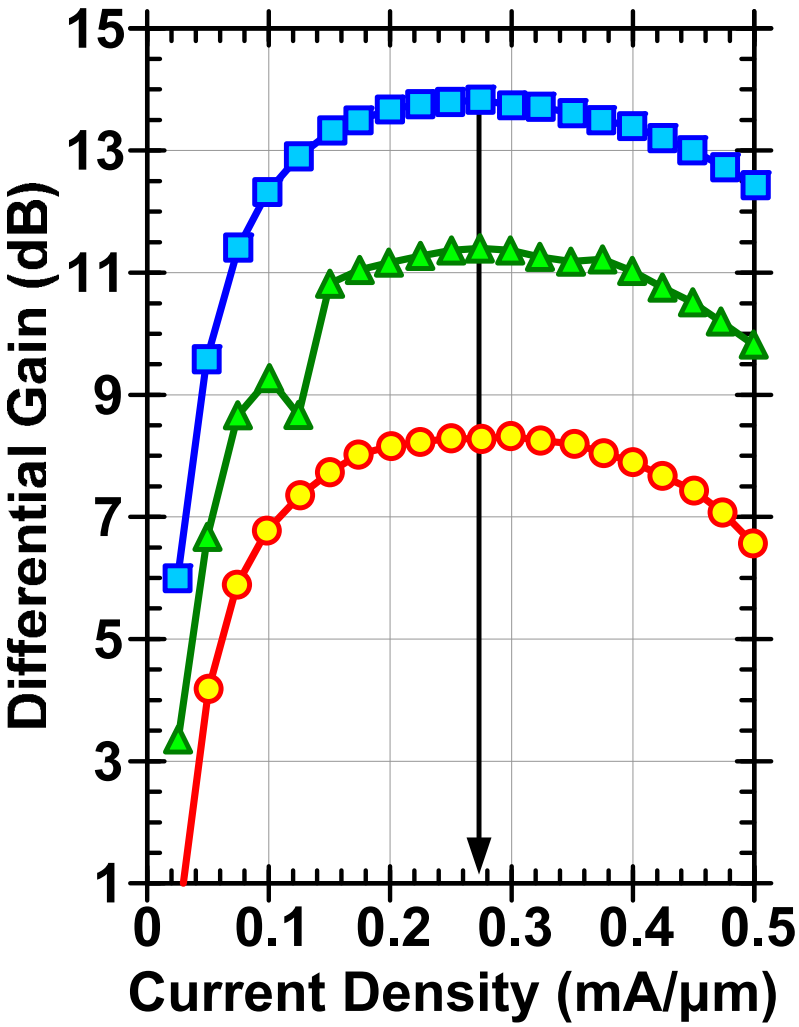
Measured Receiver DSB NF

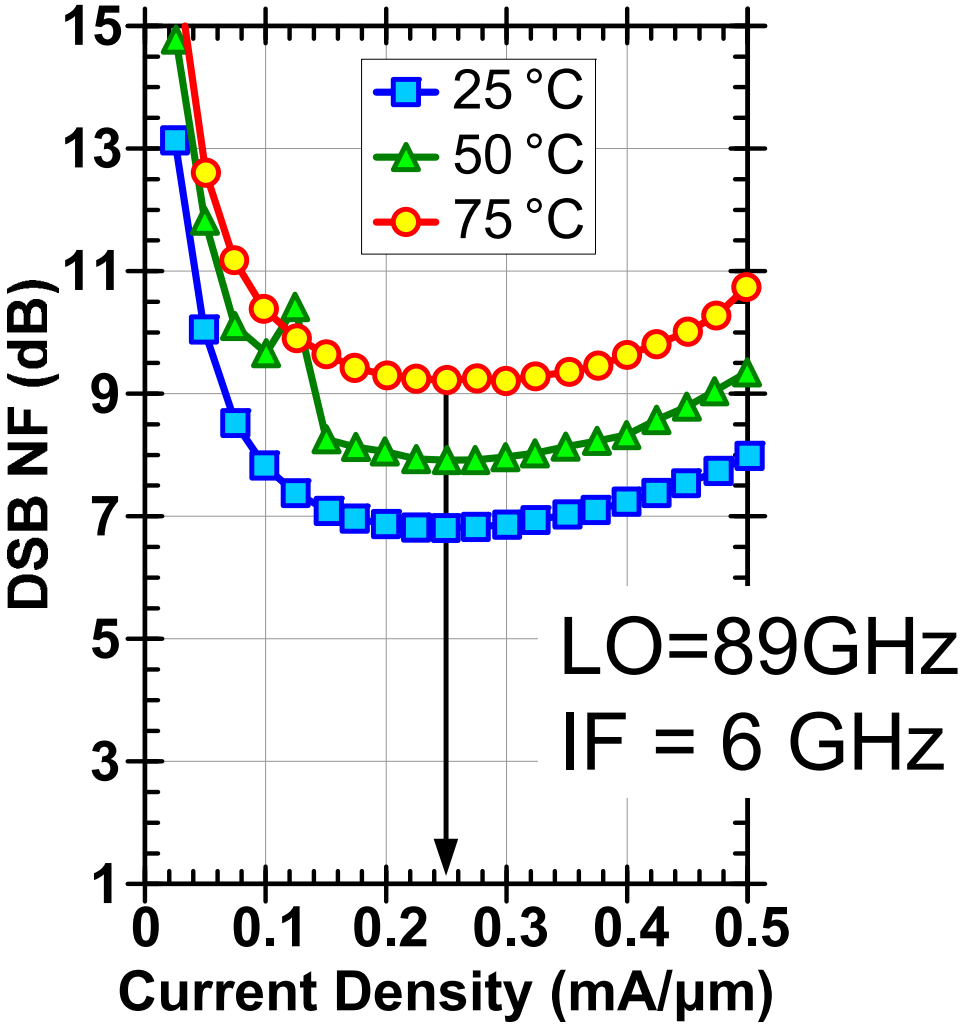


VCO = 89GHz

- 6 – 9.5 dB DSB NF
- Gain confirmed by NF measurement

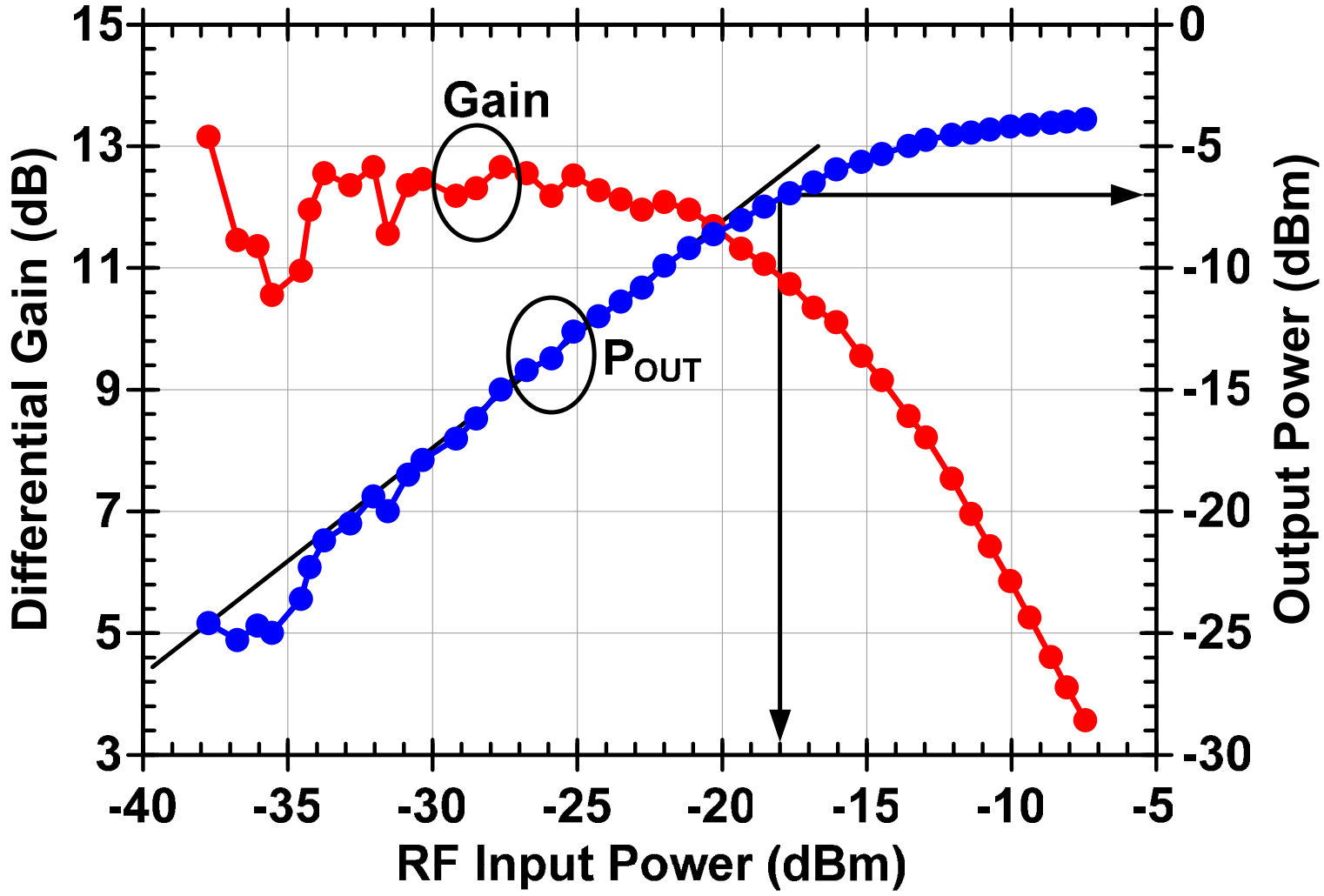
Measured Rx Optimal Bias





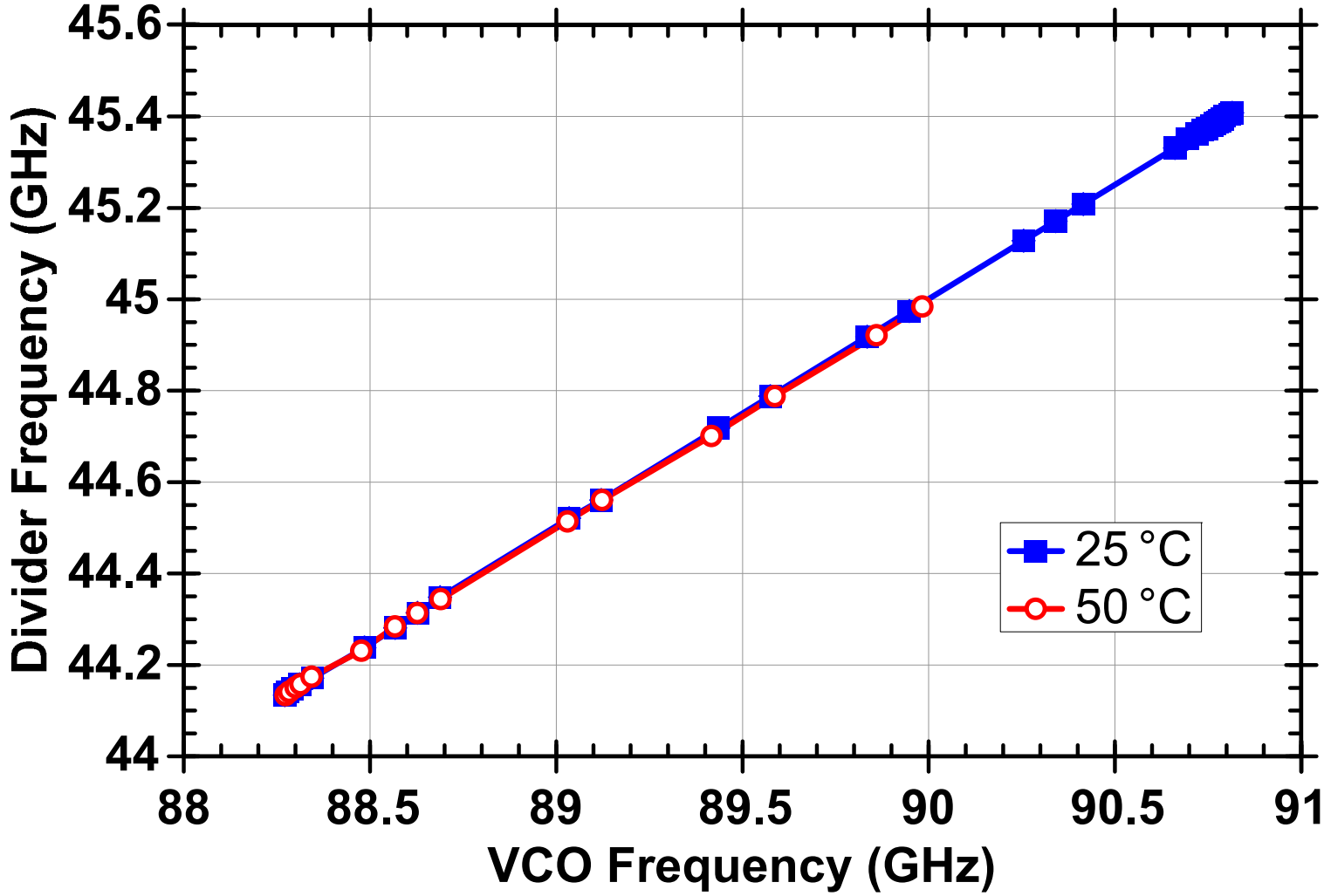
- Current swept in the 1st LNA stage
- $J_{GAIN,OPT} > J_{NFMIN,OPT}$, insensitive to V_T, I_{bias} variation

Measured Receiver Linearity



- RF = 85 GHz, LO = 89 GHz
- Input $P_{1\text{-}dB}$ = -18 dBm

Measured Static Divider Operation



- Measured by observing the VCO and divider signals simultaneously

Comparison to Previous Work: 60G

Spec.	This Work	B. Floyd, ISSCC06	S. Emami, ISSCC07
Integration level	fundamental VCO, LNA, mixer, 50-Ω IF amp, static divider	LNA, super-heterodyne receiver, PLL, BB amp.	VCO, doubler, LNA, mixer, IF amplifier
3-dB BW	76 – 95 GHz	59 – 64 GHz	57 – 63 GHz
Power Gain	12.5 dB	38-40 dB	11.8 dB
NF	7 dB	5-6.7 dB	10.4
Input $P_{1\text{-dB}}$	-18 dBm	-36 dBm	-15.8 dBm
VCO Freq.	88.3-91.3GHz	16.8-18.3GHz	28.4-29.4GHz
VCO PN @ 1MHz off.	-95 dBc/Hz (at 90.3GHz)	-90dBc/Hz	-93dBc/Hz (at 29GHz)
DC Power	206.4 mW	527 mW	76.8 mW
Supply	1.2 V / 1.5 V	2.7 V	1.2V
Die Area	0.66 mm^2	5.78 mm^2	3.8 mm^2
Technology	65-nm GP CMOS	0.13μm SiGe BiCMOS	0.13μm CMOS

Comparison to Previous Work: 77G

Spec.	This Work	Babakhani, ISSCC'06	Nicolson, MTT'08
Integration level	fundamental VCO, LNA, mixer, 50-Ω IF amp, static ÷ 2	VCO, LNA, mixer, injection locked divider	VCO, mixer, LNA, 50-Ω IF amplifier, static ÷ 64
3-dB BW	76 – 95 GHz	76 – 80 GHz	85 – 96 GHz
Power Gain	12.5 dB	35 dB	31 dB
NF	7 dB	8-10 dB	5.2 dB
Input $P_{1\text{-dB}}$	-18 dBm	-27.5 dBm	-30 dBm
VCO Freq.	88.3-91.3GHz	52 GHz	76 GHz
VCO PN @ 1MHz off.	-95 dBc/Hz (at 90.3GHz)	-95 dBc/Hz (at 54GHz)	-99 dBc/Hz
DC Power	206.4 mW	186 mW	700 mW
Supply	1.2 V / 1.5 V	3.3 / 5 V	1.8 / 2.5 / 3.3 V
Die Area	0.66 mm^2	6.46 mm^2	1.02 mm^2
Technology	65-nm GP CMOS	250 f_{MAX} SiGe HBT	230/300GHz f_T/f_{MAX} 0.13μm SiGe HBT

Conclusion

- 76-95GHz receiver with 90-GHz VCO and divider
- Clock distribution using transformers
- Unique bias distribution & isolation scheme
- Operation verified up to 100°C
- Highest-frequency CMOS receiver (for now)
- W-band receiver integration demonstrated

Acknowledgements

- Alexander Tomkins for varactor measurements
- Kenneth Yau for transistor measurements
- STMicroelectronics for fabrication
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- NSERC for funding