A Back-Wafer Contacted Silicon-On-Glass Integrated Bipolar Process—Part II: A Novel Analysis of Thermal Breakdown

Nebojša Nenadović, *Student Member, IEEE*, Vincenzo d'Alessandro, Lis K. Nanver, *Member, IEEE*, Fabrizio Tamigi, Niccolò Rinaldi, *Member, IEEE*, and Jan W. Slotboom, *Member, IEEE*

***Abstract*—Analytical expressions for the electrothermal parameters governing thermal instability in bipolar transistors, i.e., thermal resistance R_{TH}, critical temperature T_{crit} and critical current $J_{\mathrm{C,crit}}$, are established and verified by measurements on silicon-on-glass bipolar NPNs. A minimum junction temperature increase above ambient due to selfheating that can cause thermal breakdown is identified and verified to be as low as 10–20 °C. The influence of internal and external series resistances and the thermal resistance explicitly included in the expressions for T_{crit} and $J_{\mathrm{C,crit}}$ becomes clear. The use of the derived expressions for determining the safe operating area of a device and for extracting the thermal resistance is demonstrated.**

***Index Terms*—Bipolar transistors, radio frequency (RF) technologies, silicon-on-glass, thermal breakdown, thermal management, thermal resistance.**

I. Introduction

In PART I of this paper, a novel back-wafer contacted silicon-on-glass integrated bipolar technology for radio frequency (RF) applications was presented [1]. Considerable reduction of device size and parasitics was achieved by using substrate transfer to glass, trench isolation and low-ohmic collector contacting via the back-wafer. The use of isolating materials (mainly glass, oxide, and nitride) not only yields a perfect RF isolation but also provides an almost perfect thermal isolation. The heat generated within the device itself can only spread very slowly into the substrate and is largely confined to the silicon lattice of the active device. This results in an extremely large equivalent thermal resistance of the silicon-on-glass NPNs and a strong electrothermal feedback during device operation. Even in small, single-emitter devices operating at relatively low power levels thermal instabilities are readily observed. In bulk-silicon processes, on the other hand, thermal instability is seen only in large high power devices. Observations of such phenomena date back even to the late '50s [2]–[4]. Several efforts have been devoted towards determining the conditions that lead to thermal instability. Some detailed theories at carrier level have been proposed [5]–[7], in which the authors focus on evaluation of the local hot-spot temperature that triggers thermal breakdown in single-emitter devices. Such mechanisms are usually related to operation regimes under very high currents and voltages. Conditions were sought for which a perturbation of the current distribution at one place leads to a localized increase in the power density and temperature, which can cause thermal breakdown. A different, circuit-level approach has been pursued by yet other authors, who concentrate on the derivation of the biasing conditions and associated temperature that lead to thermal breakdown in multicellular devices. These approaches can be classified as either analytical [8]–[10], semi-analytical [11], [12] or numerical [13]. The present silicon-on-glass transistors are the first silicon-based devices, in which the absence of efficient heat sinks enables the experimental study of thermal breakdown at such low current levels that neither high-current/voltage effects nor series resistances dominate the device behavior. In such single-emitter, low-power transistors a perfect thermal isolation is combined with a limited device size and it is safe to assume that the junction temperature is constant along the device. Under these conditions it has been possible to get a clear view of the selfheating and thermal breakdown mechanism, whereby very simple device models could be formulated and verified experimentally.

First, a temperature-independent formulation for the base–emitter voltage temperature coefficient is established. This enabled the definition of a new compact analytical model for the rise in junction temperature, called the critical temperature rise ΔT_{crit}, necessary for thermal breakdown. It is proven here that for bipolar transistors with very high thermal resistance and small series resistances, such as RF devices, the critical temperature rise above ambient is a weak function of both the device biasing conditions and thermal resistance, and can be as low as 10–20 °C. Similar results have been achieved by previous authors [11], [14]–[16]. The formulation of the critical temperature presented here is, however, complete, explicit and analytical, and also verified experimentally. Among the other things the role of internal and external series resistances for the electrothermal response of the transistor becomes clear from this new model. The applicability of this formulation for the extraction of thermal resistance is demonstrated by the experiments described in Part I. Moreover, the formulation of ΔT_{crit} leads to a novel equation for determining the critical current $J_{\mathrm{C,crit}}$

Manuscript received April 21, 2003. The review of this paper was arranged by Editor T. Skotnicki.

N. Nenadović and L. K. Nanver are with Laboratory of ECTM, DIMES, Delft University of Technology, Feldmannweg 17, 2600 GB Delft, The Netherlands (e-mail: nanver@dimes.tudelft.nl).

V. d'Alessandro, F. Tamigi, and N. Rinaldi are with Department of Electronics and Telecommunications Engineering, University of Naples "Federico II," 80125 Naples, Italy.

J. W. Slotboom is with Laboratory of ECTM, DIMES, Delft University of Technology, Feldmannweg 17, 2600 GB Delft, The Netherlands. He is also with Philips Research Laboratories, 5656 AA Eindhoven, The Netherlands.

Digital Object Identifier 10.1109/TED.2003.820654

0018-9383/04$20.00 © 2004 IEEE

leading to thermal breakdown. Finally, the applicability of the $V_{\rm CB}$–$V_{\rm BE}$ characteristics for determining the safe operating area of devices that exhibit measurable selfheating is analyzed and a generally applicable, straightforward measurement technique is defined for predicting the critical biasing conditions. All results are supported by electrical measurements, numerical device simulations and nematic liquid crystal imaging of the device temperature.

II. Nomenclature and Basic Assumptions

The lumped-resistor model of the transistor and biasing conventions used in the following derivations are given in the circuit diagram shown in Fig. 1 along with a subcircuit describing the electrothermal feedback. The dissipated power is related to the device temperature as

$$R_{\rm TH} = \frac{T - T_0}{P} \tag{1}$$

where $R_{\rm TH}$ is the equivalent thermal resistance, P is the dissipated power, T_0 is the ambient temperature, and T is the junction temperature [17]. The thermal resistance $R_{\rm TH}$ is assumed to be bias independent. This is a reasonable assumption when the thermal resistance is dominated by the device surroundings and not by size modulation of the heat source [18], [19]. The emitter, base, and collector series resistances are denoted r_E, r_B, and r_C, respectively, for internal parasitics and R_E, R_B, and R_C, respectively, for external (ballasting) resistors. The voltage that drops across the base–emitter junction itself is defined as the internal emitter–base voltage $V_{\rm BEint}$. The externally applied voltages are specified by the suffix ext. The relationship between the $V_{\rm BEext}$ and $V_{\rm BEint}$ is given by

$$V_{\rm BEint} = V_{\rm BEext} - AJ_C R_{\rm EB} \tag{2}$$

where A is the emitter area, J_C is the collector–current density, and $R_{\rm EB}$ is given by

$$R_{\rm EB} = \frac{1}{\beta}(R_B + r_B) + \frac{\beta + 1}{\beta}(R_E + r_E)$$

where β is the current gain of the device. Only forward active mode of operation is examined so the dissipated power in the device can be expressed as

$$P = AJ_C(V_{\rm CEext} - AJ_C R_{\rm EC}). \tag{3}$$

where

$$R_{\rm EC} \approx R_E + R_C$$

The device is biased through the external resistors in a common–base configuration. Either a current or voltage source is applied to the emitter terminal. In the forward linear region of interest here the current gain dI_C/dI_B is much larger than unity and I_C will be assumed equal to I_E.

Since the devices under consideration show thermal breakdown at low power levels with correspondingly low collector–current levels, high-current effects can be assumed negligible. The following analytical expression is therefore used to relate J_C to $V_{\rm BEint}$ [20], [21]

$$J_C = CT^{4-m} \exp\left(\frac{V_{\rm BEint} - V_{G0}}{V_T}\right) \tag{4}$$

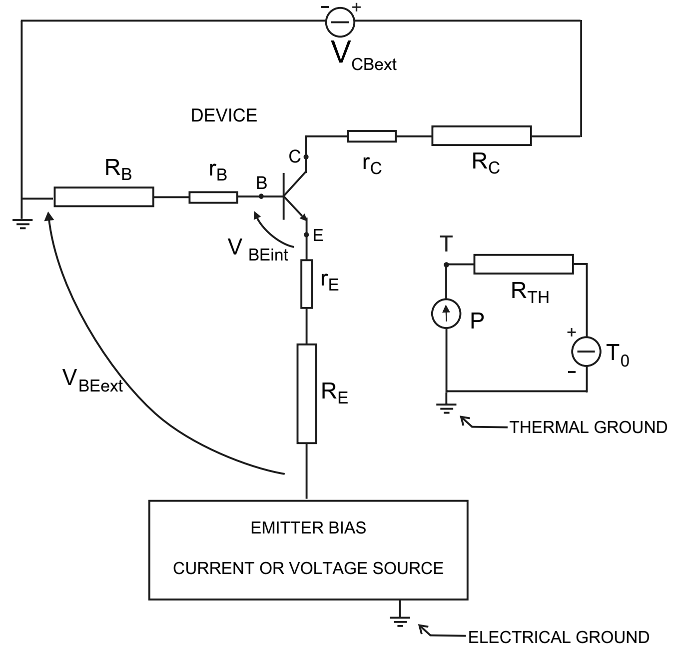


Fig. 1. DC circuit diagram of an ideal BJT with lumped resistors and a subcircuit accounting for selfheating. Emitter can be biased in current-controlled mode or voltage-controlled mode.

where m is the mobility power factor, C is a temperature independent coefficient, V_{G0} is the extrapolated silicon bandgap voltage in the base at 0 K, and V_T is the thermal voltage. Avalanching and Early effects are also assumed negligible, and the temperature distribution across the device is assumed to be uniform. All these assumptions are shown in the following to be valid for the small, thermally well-isolated silicon-on-glass devices that are studied experimentally here.

III. The Base–Emitter Voltage Temperature Coefficient Model

A parameter generally adopted to describe the electrothermal behavior of a bipolar transistor is the base–emitter voltage temperature coefficient φ [9], [13]. This coefficient is defined as the $V_{\rm BE}$ shift required to keep the collector–current constant as the junction temperature changes [8], [22]

$$\varphi = \left.\frac{\partial V_{\rm BE}}{\partial T}\right|_{J_C}. \tag{5}$$

Since J_C always increases with temperature, φ is negative, regardless of the material in which the transistor is fabricated. As a first step toward a formulation of $\Delta T_{\rm crit}$, an analytical expression for φ is derived. Equation(5) can be applied to both the internal and external base–emitter voltages and two corresponding coefficients φ_{int} and φ_{ext} are defined. By inserting (2) and (4) in (5) a straightforward calculation gives

$$\varphi_{int}(J_C, T) = -\frac{k}{q}(4 - m) + \frac{k}{q}\ln\frac{J_C}{CT^{4-m}} \tag{6}$$

$$\varphi_{ext}(J_C, T) = \varphi_{int}(J_C, T) + f(J_C, T) \tag{7}$$

where k is Boltzmann's constant, q is the electron charge and

$$f(J_C, T) = AJ_C \left.\frac{\partial R_{\rm EB}}{\partial T}\right|_{J_C}.$$

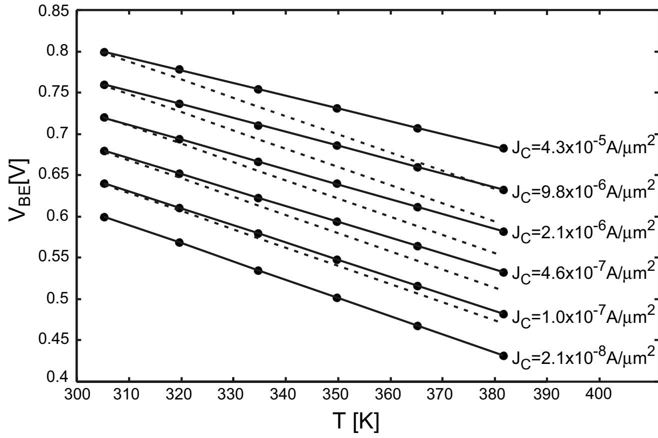


Fig. 2. Base–emitter voltage as a function of temperature for different values of collector–current density. The base–emitter voltage temperature coefficient is extracted as the slope of the curves through the (symbols) measurement results. The dashed lines are parallel to the lowest J_C curve.

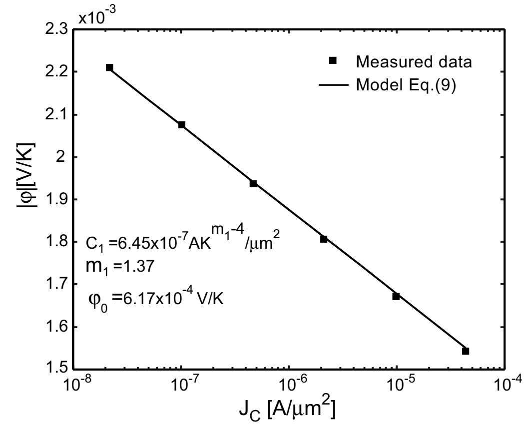


Fig. 3. Base–emitter voltage temperature coefficient as a function of collector-current density. Experimentally extracted values (symbols) are compared to the (solid line) model of (9).

In Appendix A the term $f(J_C, T)$ is evaluated and found to be negligible with respect to φ_{int}. Thus

$$\varphi_{ext}(J_C, T) \cong \varphi_{int}(J_C, T) = -\frac{k}{q}(4-m) + \frac{k}{q}\ln\frac{J_C}{CT^{4-m}} \tag{8}$$

whereby φ_{ext} is shown to be a function of the current density and temperature. To further simplify the expression for φ_{ext}, the relationship to J_C and T has been evaluated experimentally. Measurements presented in this paper were performed on silicon-on-glass transistors with an emitter area $A = 20 \times 1\ \mu\text{m}^2$ using a HP4156B parameter analyzer and a Cascade probe station equipped with a thermal chuck. Gummel plots were measured at different substrate temperatures ranging from 300 K to 380 K, which amply covers the expected range of T_{crit}. The measurements were performed in pulsed mode on a device with the lowest available thermal resistance and with $V_{\text{CB}} = 0$ V. Fig. 2 shows the base–emitter voltage as a function of temperature for different fixed collector–current densities. The slope is given by the differential of each curve. These are all linear and thus φ_{ext} is temperature independent. There is, however, a clear dependence on J_C, which is accentuated in the graph by the dashed lines that are parallel to the curve for the lowest J_C value. Based on this experimental evidence a temperature-independent model has therefore been adopted

$$\varphi_{ext}(J_C) = -\varphi_0 + \frac{k}{q}\ln\frac{J_C}{C_1 T_0^{4-m_1}} \tag{9}$$

where the values for φ_0, C_1 and m_1 are extracted from the measurements. Fig. 3 shows the agreement between the model and the experimental data for this particular device. Theoretically this temperature-independent approximation is also expected to be quite accurate because the logarithmic relationship to T in (8) makes φ_{ext} a weak function of the junction temperature itself. The dependence on J_C, on the other hand, cannot be neglected because in the usual operating regime of the transistor the current varies by several decades.

IV. Model for the Critical Junction Temperature

In Part I of this work, several Gummel plot measurements of silicon-on-glass NPN BJT's are shown for both the voltage-controlled mode and the current-controlled mode. Thermal runaway is readily observed in the voltage-controlled mode as a sharp increase in collector–current with base–emitter voltage, leading to the immediate burnout of the transistor. The point of onset of thermal instability can be detected in the current-controlled Gummel plot as the boundary point between the positive and the negative differential resistance region (*flyback point* or *snapback point*). This *critical point* is found as the biasing point for which [23]

$$\left.\frac{dV_{\text{BEext}}}{dJ_C}\right|_{V_{\text{CBext}}} = 0 \tag{10}$$

that is equivalent to [7], [11], [24]

$$\left.\frac{\partial J_C}{\partial T}\right|_{V_{\text{BEext}},V_{\text{CBext}}} \left.\frac{\partial T}{\partial J_C}\right|_{V_{\text{BEext}},V_{\text{CBext}}} - 1 = 0. \tag{11}$$

Thus for each applied collector-base voltage a critical collector–current density $J_{\text{C,crit}}$ can be determined from these relationships. The $J_{\text{C,crit}}(V_{\text{CEext}})$ values set a limit for safe device operation. Since the thermal runaway is a feedback phenomenon in which the collector–current increases due to a temperature increase and vice versa, it is essential to accurately determine both $J_{\text{C,crit}}$ and T_{crit}.

In the following a theoretical formulation for the critical temperature as a function of $J_{\text{C,crit}}$ is obtained by inserting (1)–(4) and (9) in (10). The complete derivation is given in Appendix B and results in a compact analytical expression for the temperature increase above ambient at the critical point ΔT_{crit} as a function of biasing conditions and series resistances. The ΔT_{crit} is expressed as the sum of three individual temperature rises

$$\Delta T_{\text{crit}} = \Delta T_{\min} + \Delta T_{\text{R,EB}} + \Delta T_{\text{R,EC}} \tag{12}$$

where

1) The first term $\Delta T_{\min}$ is the temperature rise necessary for reaching thermal runaway in the absence of any series

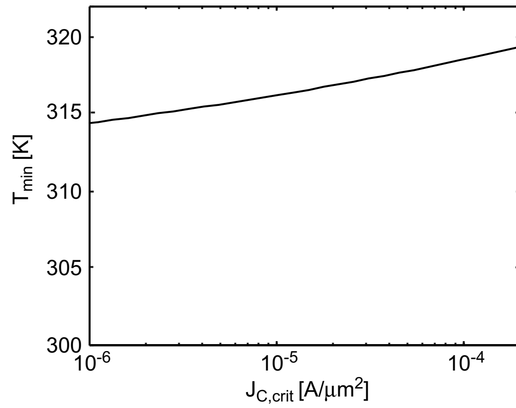


Fig. 4. Minimum junction temperature necessary for thermal runaway versus critical collector–current density for a device where series resistance is not playing any role.

resistances, either parasitic or externally applied, and is given by

$$\Delta T_{\min} = \frac{\frac{kT_0}{q}}{|\varphi_{ext}(J_{\mathrm{C,crit}})| - \frac{k}{q}} \tag{13}$$

where the base–emitter voltage temperature coefficient φ_{ext} is temperature independent as in (9).

2) The second term $\Delta T_{\mathrm{R,EB}}$ represents the temperature rise necessary to compensate for the voltage drop $V_{\mathrm{BEext,crit}}$–$V_{\mathrm{BEint,crit}}$ across the emitter and base series resistances, $R_E + r_E$ and $R_B + r_B$, shown in Fig. 1

$$\Delta T_{\mathrm{R,EB}} = \frac{V_{\mathrm{BEext,crit}} - V_{\mathrm{BEint,crit}}}{|\varphi_{ext}(J_{\mathrm{C,crit}})| - \frac{k}{q}}. \tag{14}$$

3) The third term $\Delta T_{\mathrm{R,EC}}$ is the temperature rise necessary to compensate for the influence of the external collector and emitter series resistance R_{EC} on the applied voltage V_{CE}

$$\Delta T_{\mathrm{R,EC}} = \frac{A^2 J_{\mathrm{C,crit}}^2 R_{\mathrm{EC}} R_{\mathrm{TH}}}{1 - \frac{\frac{k}{q}}{|\varphi_{ext}(J_{\mathrm{C,crit}})|}}. \tag{15}$$

Equation (12) can be rewritten in terms of T_{crit}

$$T_{\mathrm{crit}} = \frac{T_0 + \frac{AJ_{\mathrm{C,crit}} R_{\mathrm{EB}}}{|\varphi_{ext}(J_{\mathrm{C,crit}})|} + A^2 J_{\mathrm{C,crit}}^2 R_{\mathrm{EC}} R_{\mathrm{TH}}}{1 - \frac{\frac{kT_0}{q}}{|\varphi_{ext}(J_{\mathrm{C,crit}})| T_0}}. \tag{16}$$

Both (12) and (16) are generally applicable. From (1) the thermal resistance can be expressed as

$$R_{\mathrm{TH}} = \frac{T_{\mathrm{crit}} - T_0}{P_{\mathrm{crit}}} = \frac{T_{\mathrm{crit}} - T_0}{AJ_{\mathrm{C,crit}}(V_{\mathrm{CEext}} - AJ_{\mathrm{C,crit}} R_{\mathrm{EC}})} \tag{17}$$

which, by inserting in (16) and solving for R_{TH} is equivalent to [see (18), shown at the bottom of the page]. Thus both T_{crit} and R_{TH} can be found if $J_{\mathrm{C,crit}}$ is known.

Very often the $J_{\mathrm{C,crit}}$ is too high to be measured and alternative methods are used to estimate reasonable values of R_{TH}. By using such a value of R_{TH} and assuming φ_{ext} to be constant, an equation for $J_{\mathrm{C,crit}}$ can be derived from (16) and (17)

$$J_{\mathrm{C,crit}}^2 A^2 R_{\mathrm{EC}} R_{\mathrm{TH}} \left(2|\varphi_{ext}| - \frac{k}{q}\right) + J_{\mathrm{C,crit}} A \left[R_{\mathrm{EB}} + \left(\frac{k}{q} - |\varphi_{ext}|\right) R_{\mathrm{TH}} V_{\mathrm{CEext}}\right] + \frac{kT_0}{q} = 0. \tag{19}$$

Thus, by means of (16), (18), and (19) the complete set of parameters (R_{TH}, T_{crit}, and $J_{\mathrm{C,crit}}$) can be found if one of the three is known. If T_{crit} is approximated by T_0, and the influence of each individual series resitance is not explicitly taken into account, the expression for $J_{\mathrm{C,crit}}$ can be simplified to give

$$I_{\mathrm{C,crit}} = J_{\mathrm{C,crit}} A = \frac{\frac{kT_0}{q}}{|\varphi| V_{\mathrm{CE}} R_{\mathrm{TH}} - R_E} \tag{20}$$

as was already found in previous works [8], [25].

$\Delta T_{\min}$ given by (13) represents the minimum temperature rise that can cause thermal breakdown in a bipolar transistor. The T_{crit} increases for each added series resistance through which the internal device is biased. In the situation with no added external resistors (i.e., $R_{\mathrm{EC}} \approx 0$) and very high thermal resistance, where the onset of thermal instability occurs at such low current levels that the internal series resistances have no influence, (16) becomes

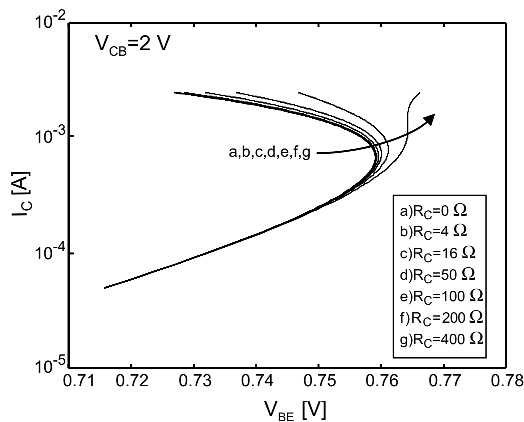
$$T_{\mathrm{crit}} = T_{\min} = \frac{T_0}{1 - \frac{\frac{kT_0}{q}}{|\varphi_{ext}(J_{\mathrm{C,crit}})| T_0}}. \tag{21}$$

The graphical representation of (21) is shown in Fig. 4, where $T_{\min}$ is plotted versus the critical collector–current density $J_{\mathrm{C,crit}}$. It can be seen that the minimum junction temperature that can lead to thermal breakdown in silicon BJT's is small and almost constant (314–320 K) within a wide range of critical current densities. The $J_{\mathrm{C,crit}}$ follows the thermal resistance and collector-emitter voltage, so it is concluded that the exact values of R_{TH}, and V_{CE} are not of a great significance for the critical junction temperature as long as the thermal resistance is very high.

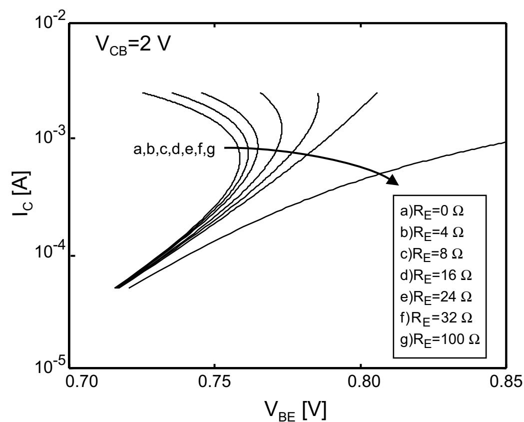
A. Electrical Measurements

The influence of external resistors on $J_{\mathrm{C,crit}}$ and the associated T_{crit} has been studied by performing emitter current-controlled measurements on a silicon-on-glass NPN BJT where resistors of different values were connected to either the emitter or collector. The I_C–V_{BE} plots are shown in Fig. 5(a) and (b). Note that an emitter ballasting resistor has a much greater effect on the electrothermal feedback than a collector resistor of the

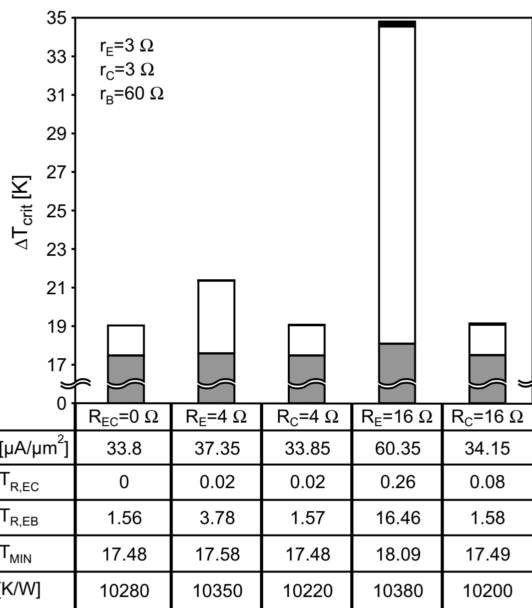
$$R_{\mathrm{TH}} = \frac{\frac{kT_0}{q} + AJ_{\mathrm{C,crit}} R_{\mathrm{EB}}}{AJ_{\mathrm{C,crit}} \left[AJ_{\mathrm{C,crit}} R_{\mathrm{EC}} \left(\frac{k}{q} - 2\left|\varphi_{ext}(J_{\mathrm{C,crit}})\right|\right) + V_{\mathrm{CEext}} \left(\left|\varphi_{ext}(J_{\mathrm{C,crit}})\right| - \frac{k}{q}\right)\right]} \tag{18}$$



(a)



(b)

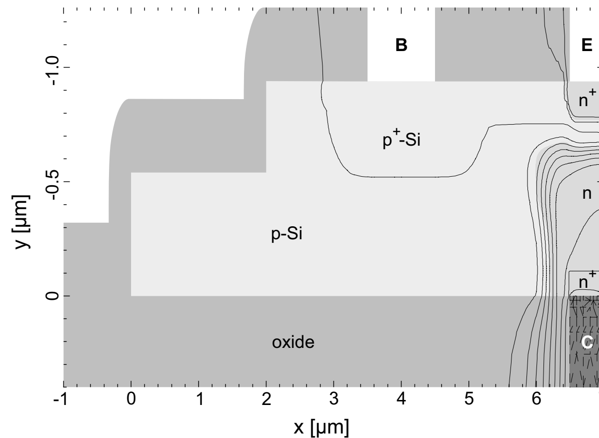


	R_{EC}=0 Ω	R_E=4 Ω	R_C=4 Ω	R_E=16 Ω	R_C=16 Ω
$J_{C,crit}$[μA/μm²]	33.8	37.35	33.85	60.35	34.15
■ $\Delta T_{R,EC}$	0	0.02	0.02	0.26	0.08
□ $\Delta T_{R,EB}$	1.56	3.78	1.57	16.46	1.58
▩ ΔT_{MIN}	17.48	17.58	17.48	18.09	17.49
R_{TH} [K/W]	10280	10350	10220	10380	10200

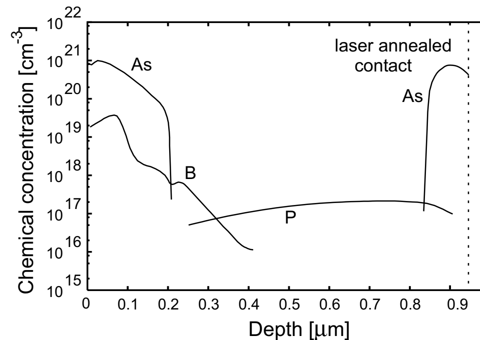
(c)

Fig. 5. Current-controlled I_C–$V_{\rm BE}$ Gummel plots for different values of (a) R_C and (b) R_E. (c) Influence of the ballasting resistors on $T_{\rm crit}$.

same value. Simultaneous extraction of $R_{\rm TH}$ and $T_{\rm crit}$ is performed using the results shown in Fig. 5(a) and (b) and following the procedure explained above. Each temperature term of (12) that contributes to the overall temperature increase is plotted in the histogram presented in Fig. 5(c). It can be seen that $\Delta T_{\rm R,EB}$



(a)



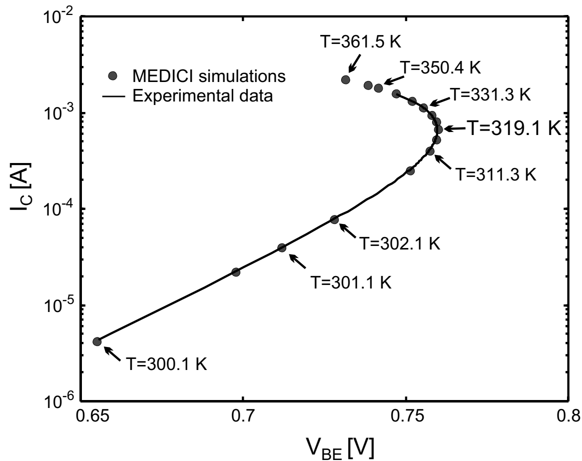
(b)

Fig. 6. (a) Simulated NPN transistor. (b) Doping profiles of the E-B-C region imported into MEDICI.

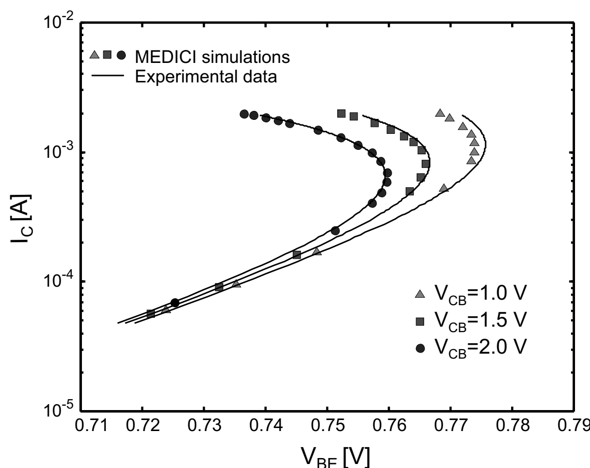
significantly changes with R_E and can become dominating for large resistance values. On the other hand, the impact of $\Delta T_{\rm R,EC}$ on $\Delta T_{\rm crit}$ is noticeable only for very high values of R_C and/or R_E. The extracted thermal resistance values are also shown in Fig. 5(c). They are quite constant, showing that the measurement method is not sensitive to variations in biasing condition.

B. Device Simulations

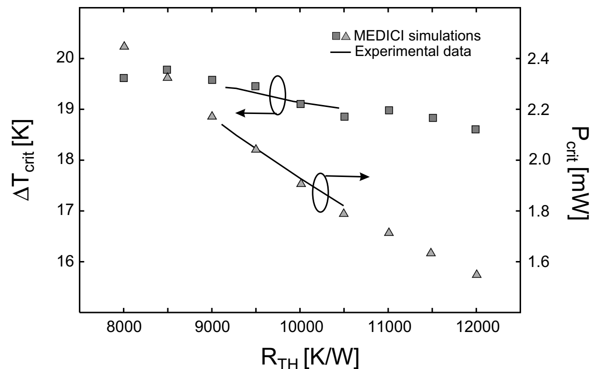
The device simulator MEDICI [26], where selfheating can be included by solving the lattice heating equation, has also been used here to verify the theoretical formulation of $\Delta T_{\rm crit}$. The NPN transistor shown in Fig. 6(a) was used in the simulations. The vertical doping profiles of the active E-B-C regions, shown in Fig. 6(b), were imported into MEDICI. The thermal electrode was defined at the emitter side of the device and a lumped thermal resistance of 10^4 K/W was connected to this electrode. The ambient temperature was set to 300 K and a voltage $V_{\rm CB} = 2$ V was applied. Fig. 7(a) shows the comparison between the simulated and measured I_C–$V_{\rm BE}$ characteristics. Excellent agreement is achieved: MEDICI derives a maximum lattice temperature of 319.1 K in the critical point, while the analytical model gives 319 K. The situations for $V_{\rm CB} = 1$ V and $V_{\rm CB} = 1.5$ V are also depicted in Fig. 7(b) to illustrate the decrease in $I_{\rm C,crit}$ and $V_{\rm BE,crit}$ with increasing $V_{\rm CB}$. MEDICI has also been used to investigate the effect of different equivalent thermal resistances (i.e., different heat spreaders) on $\Delta T_{\rm crit}$,



(a)



(b)



(c)

Fig. 7. (a) Simulated and measured I_C–$V_{\rm BE}$ characteristics at $V_{\rm CB} = 2$ V for the device shown in Fig. 6(a) with a lumped thermal resistance of $R_{\rm TH} = 10^4$ K/W. The temperature derived by MEDICI is also indicated. (b) Comparison between simulated and measured I_C–$V_{\rm BE}$ characteristics at different $V_{\rm CB}$ for the same device. (c) Comparison between simulated and measured $P_{\rm crit}$ and $\Delta T_{\rm crit}$ as a function of device thermal resistance.

by connecting different lumped thermal resistances in the range from $8 \cdot 10^3$ to $1.2 \cdot 10^4$ K/W to the thermal electrode. In Fig. 7(c) the numerical results are compared to results of the analytical model applied to the experimental characteristics of devices with different heat spreaders presented in Part I. In this figure $P_{\rm crit}$ is seen to decrease with increasing $R_{\rm TH}$ as would be expected.

C. Nematic Liquid Crystal Measurements

In Part I, nematic liquid crystal (NLC) temperature mapping has been used to visualize the heat distribution over and around silicon-on-glass devices. NLC measurement of the critical temperature is given here as a further support to the proposed analytical formulation. The measured device geometry is sketched in Fig. 8(a). In Fig. 8(b) and (c), microscope images of the devices covered with a thin layer of NLC and contacted at the base, collector and upper emitter E1, are shown. The device was biased at the critical point and the chuck temperature was varied by steps of 0.5 °C. The image shown in Fig. 8(c) was taken when a dark region appeared over the top emitter finger. Since the clearing point of the applied NLC is 56.5 °C and the chuck temperature was set to 32 °C, a corresponding $\Delta T_{\rm crit}$ of 24.5 °C was concluded. Similar values of $\Delta T_{\rm crit}$, ranging from 22 °C to 25 °C, were also obtained for various other devices. The $T_{\rm crit}$ measured by this method is slightly higher than expected from the simulated and electrically measured values. This can very well be ascribed to an increased series resistance when contacting the device terminal pads with probe needles through the liquid crystal layer and the higher ambient temperature.

V. Determination of Critical Biasing Conditions From $V_{\rm BE}$–$V_{\rm CB}$ Characteristics

It is shown in this section that the $V_{\rm BE}$–$V_{\rm CB}$ characteristics for fixed collector–currents can be used to extract the critical power $P_{\rm crit}$ that leads to thermal breakdown. Under forward active operation, two concurrent mechanisms give an increase of I_C for increasing $V_{\rm CB}$ and fixed $V_{\rm BE}$: one is the Early effect (*electrical feedback*) and the other is the selfheating effect (*thermal feedback*) [27]. For a fixed I_C these mechanisms lead to a $V_{\rm BE}$ decrease with increasing $V_{\rm CB}$. If the thermal feedback is dominating, which is the case for most modern RF devices, it can be derived that $V_{\rm BE}$ is a linear function of $V_{\rm CB}$ and the slope of one $V_{\rm BE}$–$V_{\rm CB}$ characteristic is given by

$$\left.\frac{\partial V_{\rm BEext}}{\partial V_{\rm CBext}}\right|_{J_C} = \gamma(R_{\rm TH}, J_C) = \frac{\varphi_{ext}(J_C) R_{\rm TH} A J_C}{1 - \varphi_{ext}(J_C) R_{\rm TH} A J_C}. \tag{22}$$

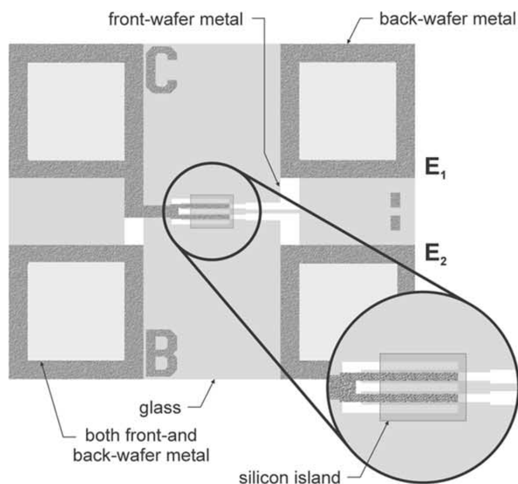
This slope is negative since the base–emitter voltage temperature coefficient φ_{ext} is negative. Equation (22) is used below to find the increase in $V_{\rm CB}$ that is necessary for inducing thermal breakdown at a given J_C. Since the currents and voltages applied over the device determine the dissipated power, $P_{\rm crit}$ can then be found.

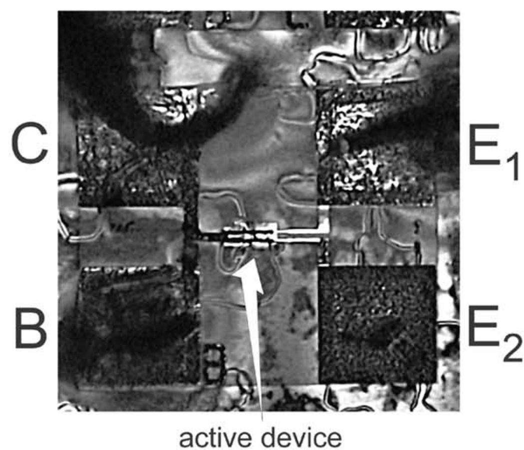
We define $\Delta V_{\rm BEext,crit}$ as the change of $V_{\rm BE}$ induced by a junction temperature change going from $T|_{V_{\rm CBext}=0}$ to $T_{\rm crit}$

$$\Delta V_{\rm BEext,crit} = V_{\rm BEext}(V_{\rm CBext,crit}) - V_{\rm BEext}(V_{\rm CBext} = 0) = \int_{T|_{V_{\rm CBext}=0}}^{T_{\rm crit}} \varphi_{ext}(J_C) dT. \tag{23}$$

Since the coefficient φ_{ext} can be assumed temperature independent, (23) becomes

$$\Delta V_{\rm BEext,crit} = \varphi_{ext}(J_C) \Delta T_{\rm crit} - \varphi_{ext}(J_C) \left(T|_{V_{\rm CBext}=0} - T_0\right). \tag{24}$$





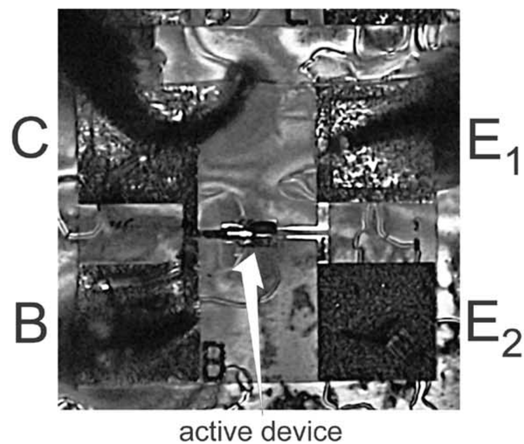
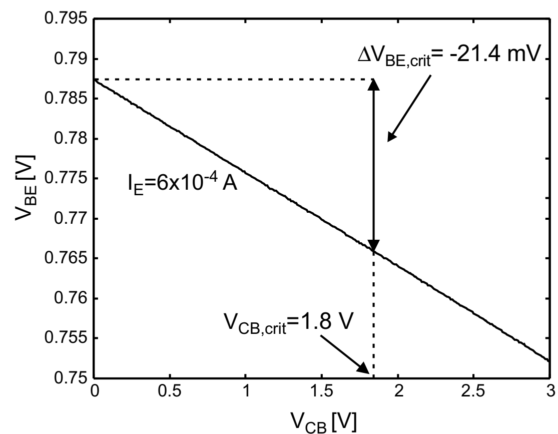


Fig. 8. Detection of the critical temperature using NLC mapping. (a) Schematic of the measured silicon-on-glass BJT. (b) Unbiased device covered with a thin layer of NLC. (c) The same device biased at the critical point. The dark region completely covering the active device finger B-C-E_1 is clearly visible in (c).

By inserting (1) and (3) with $V_{\rm CBext} = 0$ and $T = T|_{V_{\rm CBext}=0}$

$$T|_{V_{\rm CBext}=0} - T_0 = AJ_C R_{\rm TH} \left(V_{\rm BEext}|_{V_{\rm CBext}=0} - AJ_C R_{\rm EC}\right). \quad (25)$$



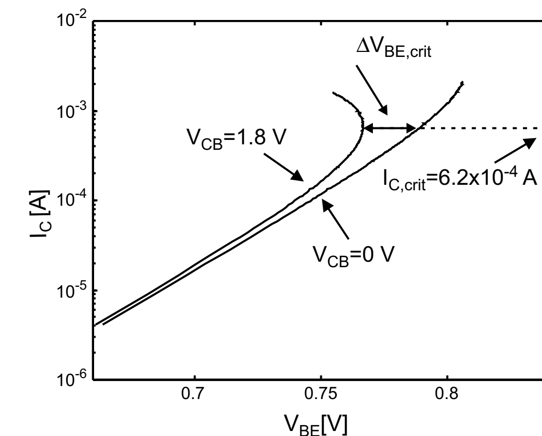


Fig. 9. (a) Measurement of $V_{\rm BE}$ versus $V_{\rm CB}$ for $I_C = 0.6$ mA with the calculated values of $V_{\rm CB,crit}$ and $\Delta V_{\rm BE,crit}$ indicated. (b) The corresponding I_C–$V_{\rm BE}$ characteristics at $V_{\rm CB} = 0$ V and 1.8 V show the same $\Delta V_{\rm CB,crit}$ and $\Delta V_{\rm BE,crit}$ relationship.

At the critical point, (22) implies that

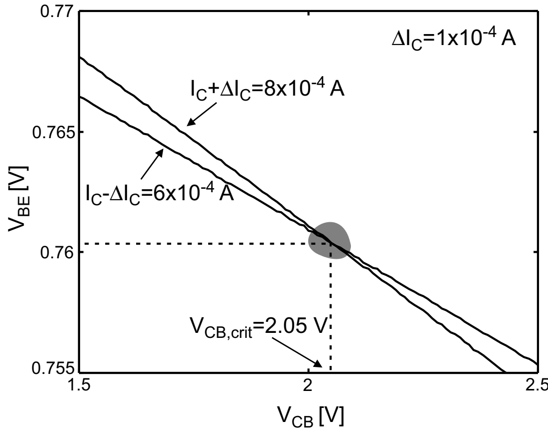
$$V_{\rm CBext,crit} = \frac{\Delta V_{\rm BEext,crit}}{\gamma}. \quad (26)$$

By combining and rearranging (22) and (24)–(26), $V_{\rm CBext,crit}$ becomes

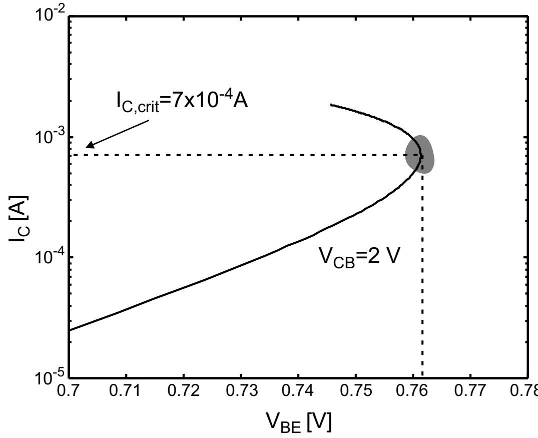
$$V_{\rm CBext,crit}(J_C) = \frac{\varphi_{ext}(J_C)\Delta T_{\rm crit}(J_C)}{\gamma} - \frac{1}{\gamma+1} V_{\rm BEext}|_{V_{\rm CBext}=0}(J_C) + \frac{1}{\gamma+1} AJ_C R_{\rm EC}. \quad (27)$$

To illustrate the use of this formula for determining $V_{\rm CBext,crit}$, consider the measurement shown in Fig. 9(a). For a given NPN BJT the $V_{\rm BE}$–$V_{\rm CB}$ characteristic has been measured with a forced collector–current of 0.6 mA. The values of $\gamma = -0.0119$ and $V_{\rm BEext}|_{V_{\rm CBext}=0} = 0.787$ V are directly extracted from the measurement and used to calculate a $V_{\rm CBext,crit}$ value of 1.8 V from (27). To validate this result, the current-controlled I_C–$V_{\rm BE}$ characteristics for both $V_{\rm CBext} = 0$ and 1.8 V have also been measured as shown in Fig. 9(b). The critical point for $V_{\rm CBext} = 1.8$ V occurs at a collector–current of 0.62 mA.

The above analytical method of finding $V_{\rm CB,crit}$ demands a calculation of $T_{\rm crit}$ and thus values for φ_0, C_1 and m_1 from (9)

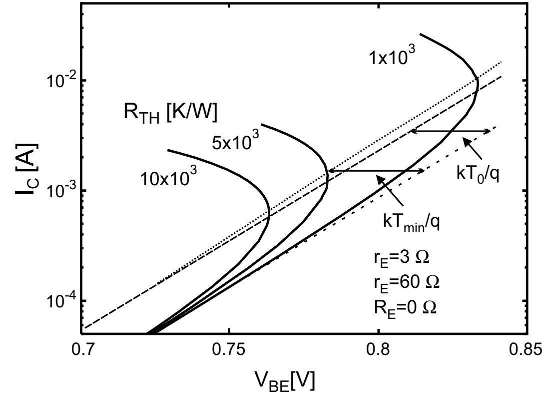


(a)

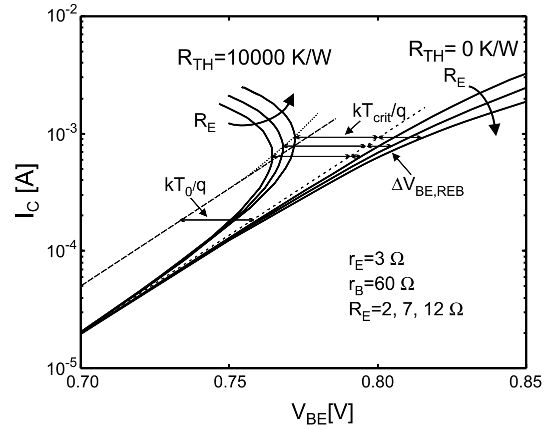


(b)

Fig. 10. (a) Detection of the critical collector-base voltage $V_{\mathrm{CB,crit}} = 2.05$ V at the intersection point of two experimentally measured V_{BE}–V_{CB} curves. (b) Verification of this $V_{\mathrm{CB,crit}}$ by measurement of the I_C–V_{BE} characteristic at $V_{\mathrm{CB}} = 2$ V.



(a)



(b)

Fig. 11. (a) MEDICI simulated I_C–V_{BE} characteristics of a device without externally added series resistance plotted for different lumped thermal resistance values. The (dashed line) I_C versus V_{BE}, I_C versus (long-dashed line) $(V_{\mathrm{BE}} - kT_0/q)$, and I_C versus (dotted line) $(V_{\mathrm{BE}} - kT_{\min}/q)$ for $R_{\mathrm{TH}} = 0$ K/W are indicated as well. (b) MEDICI-simulated I_C–V_{BE} characteristics for two devices with an R_{TH} of 0 K/W and 10^4 K/W plotted for different lumped emitter series resistors. The I_C versus (dashed line) V_{BEint}, I_C versus (long-dashed line) $(V_{\mathrm{BEint}} - kT_0/q)$, and I_C versus (dotted line) $(V_{\mathrm{BEint}} - k(T_0 + \Delta T_{\mathrm{crit}})/q)$ for $R_{\mathrm{TH}} = 0$ K/W are also shown.

must also be extracted from measurements. Moreover, in general the influence of both the thermal and electrical V_{BE}–V_{CB} feedback on the slope γ must accurately be taken into account.

A more direct, geometrical way of measuring $V_{\mathrm{CBext,crit}}$ for a fixed I_C, which is not sensitive to the V_{BE}–V_{CB} electrical feedback, is made possible by using the following equivalency:

$$V_{\mathrm{BEext}}(I_C - \Delta I_C)|_{V_{\mathrm{CBext}}} = V_{\mathrm{BEext}}(I_C + \Delta I_C)|_{V_{\mathrm{CBext}}} \quad \text{for } \Delta I_C \to 0$$

$$\Longleftrightarrow$$

$$\left.\frac{dV_{\mathrm{BEext}}}{dI_C}\right|_{V_{\mathrm{CBext}}} = 0 \tag{28}$$

that states that the intersection point of two V_{BE}–V_{CB} curves for the currents $I_C - \Delta I_C$ and $I_C + \Delta I_C$ tends toward the critical point (as defined in the $V_{\mathrm{BE}} - I_C$ plane) for ΔI_C going to zero. An example of such a measurement is shown in Fig. 10. Here I_C and ΔI_C have been chosen equal to 0.7 mA and 0.1 mA, respectively, and the V_{BE}–V_{CB} characteristics for $I_C = 0.6$ mA and 0.8 mA have been measured. The intersection point of the two lines occurs at $V_{\mathrm{CBext,crit}} = 2.05$ V. The validity of this result is substantiated by the corresponding current-controlled I_C–V_{BE} characteristic for $V_{\mathrm{CBext}} = 2$ V, for which $I_{\mathrm{C,crit}}$ is found to be 0.7 mA. Usage of the intersection point to determine $V_{\mathrm{CBext,crit}}$ extends the possibilities of actually measuring P_{crit} to situations where the intersection point lies at V_{CB} values that are too large to measure (i.e., the thermal resistance is lower). If the selfheating is high enough to allow an accurate determination of the slope γ then the intersection point can be extrapolated. The method was also validated by MEDICI simulations [28].

VI. Discussion and Conclusions

In this paper, a set of analytical expressions have been derived for the parameters R_{TH}, T_{crit} and $J_{\mathrm{C,crit}}$, which describe the electrothermal bipolar transistor behavior. If one of these parameters is known, the other two can be determined. In the present silicon-on-glass devices the critical current $J_{\mathrm{C,crit}}$ is known because it is low enough to be accurately measured as a flyback point in the current-controlled Gummel plot. The critical temperature T_{crit} and thermal resistance R_{TH} could therefore be derived and the results are substantiated by numerical simulations and nematic liquid crystal temperature mapping. The analytical expression for T_{crit} is particularly interesting because

it is an explicit function of thermal resistance and the biasing conditions at thermal breakdown. It gives an excellent basis for understanding the influence of thermal resistance and biasing conditions on the temperature rise $\Delta T_{\rm crit}$ necessary for reaching thermal instability. The significance of each term contributing to $\Delta T_{\rm crit}$ as expressed by (12) is better understood by looking at the simulation examples shown in Figs. 11(a) and (b).

MEDICI-simulated emitter current-controlled I_C–$V_{\rm BE}$ characteristics of a silicon-on-glass device where no series resistances attenuate the collector or base current (i.e., $V_{\rm BEext} = V_{\rm BEint} = V_{\rm BE}$) are shown in Fig. 11(a). Typical thermal resistance values for low-power RF devices are chosen in the range 1000–10 000 K/W for which $J_{\rm C,crit}$ goes from 500 $\mu{\rm A}/\mu{\rm m}^2$ down to 34 $\mu{\rm A}/\mu{\rm m}^2$. In the situation with a very high $R_{\rm TH}$, $\Delta T_{\rm crit}$ is equal to the first term $\Delta T_{\rm min}$ in (12) as given in (13). This $\Delta T_{\rm min}$ expresses the minimum temperature rise that, for a given $J_{\rm C,crit}$, can lead to thermal runaway in voltage-controlled mode. From (5), (9) and (13) it is clear that selfheating will have reduced $V_{\rm BE}$ at the critical point by an amount of

$$\begin{aligned}\Delta V_{\rm BE,min} &= |\varphi_{ext}(J_{\rm C,crit})|\,\Delta T_{\rm min}\\ &= \frac{k(\Delta T_{\rm min}+T_0)}{q}\\ &= \frac{kT_{\rm min}}{q}.\end{aligned} \tag{29}$$

With this definition, the critical $V_{\rm BE}$ can be written as

$$V_{\rm BE,crit} = V_{\rm BE} - \Delta V_{\rm BE,min}. \tag{30}$$

The I_C versus $V_{\rm BE}$, I_C versus $(V_{\rm BE} - kT_0/q)$ and I_C versus $(V_{\rm BE} - kT_{\rm min}/q)$ for $R_{\rm TH} = 0$ K/W are also indicated in Fig. 11(a). The $\Delta T_{\rm min}$ and thus also $\Delta V_{\rm BE,min}$ increases with $J_{\rm C,crit}$ but for a room temperature ambient the increase is only marginal over the $R_{\rm TH}$ range of interest here. In principle, for $R_{\rm TH} \to 0$, $\Delta V_{\rm BE,min}$ will continue to increase, but at some point the assumptions that the temperature distribution across the device is uniform and that the effect of the series resistances can be neglected will no longer hold. For $R_{\rm TH} \to \infty$, $\Delta V_{\rm BE,min}$ will approach kT_0/q. This result is noteworthy in two respects:

1) $\Delta V_{\rm BE,min}$ is essentially the same for all devices and approximately equal to kT_0/q as long as $R_{\rm TH}$ is very high (as is the case with silicon-on-glass devices).
2) The value of $\Delta V_{\rm BE,min} (\approx 0.0259$ V) is very small compared to the built-in voltage over the e-b junction ($\sim$1 V). In the case where $J_{\rm C,crit}$ is low, $V_{\rm BE,crit}$ is also low so the effective potential over the e-b junction is high, for example $\sim$0.5 V. In this situation the current flowing through the junction at the critical point is obviously much too low to create a flatband situation, which has sometimes been suggested to be the situation necessary for inducing thermal runaway [29], [30]. Since $\Delta V_{\rm BE,min}$ is almost independent of $J_{\rm C,crit}$, it can be concluded that it is the very high rate of current increase with increasing temperature at the critical point, and not a drastic reduction of the potential across the e-b junction, that is essential for thermal instability. However, after the onset of thermal instability in voltage-controlled mode, the current and temperature could continue to rise and eventually lead to a flatband situation.

The significance of the last two terms in (12) is illustrated in Fig. 11(b). These two terms include the influence of emitter/base series resistances (second term) and emitter/collector series resistance (third term). Several I_C–$V_{\rm BE}$ characteristics are shown in which R_E is varied for $R_{\rm TH}$ fixed at 0 K/W (case without selfheating) and 10 000 K/W (case with selfheating). In the case without selfheating, the voltage drop over R_E will lower the voltage over the intrinsic device junctions and effectively reduce I_C. The I_C versus $V_{\rm BEint}$, I_C versus $(V_{\rm BEint} - kT_0/q)$, and I_C versus $(V_{\rm BEint} - k(T_0 + \Delta T_{\rm crit})/q)$ for $R_{\rm TH} = 0$ K/W are also shown. Since $\Delta T_{\rm crit}$ depends on R_E through $J_{\rm C,crit}$, and R_E increases $J_{\rm C,crit}$ through the second and third term in (12), $\Delta T_{\rm crit}$ is increased slightly more above $\Delta T_{\rm min}$ than if R_E were absent. As has been demonstrated through the results presented in the histogram given in Fig. 5(c), the bulk of the increase of $\Delta T_{\rm crit}$ above $\Delta T_{\rm min}$ comes from the second term itself, which accounts for a $V_{\rm BE}$ shift of

$$\Delta V_{\rm BE,REB} = V_{\rm BEext,crit} - V_{\rm BEint,crit}. \tag{31}$$

This $V_{\rm BE}$ shift exactly counteracts the attenuation due to the voltage drop over series resistances $R_{\rm EB}$. In the same way, the third term $\Delta T_{\rm R,EC}$ accounts for a current increase to compensate for the attenuation due to emitter/collector series resistance.

In advanced RF BJTs where very high frequencies are reached at high current densities, emitter contact resistance becomes a limiting factor and reduction of it has become a very important issue. However, it has been demonstrated here that any decrease in the device series resistances will lower both the $J_{\rm C,crit}$ and $T_{\rm crit}$. Thus, there is a trade-off between electrical and thermal isolation that becomes more and more critical as RF device design pushes toward perfect dielectric isolation and elimination of all parasitics, making selfheating and coupling thermal effects critical design parameters in RFIC's.

The analytical formulation of $T_{\rm crit}(J_{\rm C,crit})$ gives a valuable tool for analyzing the mechanism of thermal instability. Combined with the $V_{\rm BE}$–$V_{\rm CB}$ measurement technique, it increases the possibilities of identifying the critical biasing conditions of a given device.

APPENDIX A

In this section, we provide a short description of the derivation of (8).

The term

$$f(J_C, T) = AJ_C \frac{\partial R_{\rm EB}}{\partial T}\bigg|_{J_C} \tag{A.1}$$

can be reasonably approximated by

$$f(J_C, T) = AJ_C \frac{\partial}{\partial T}\left(\frac{1}{\beta}(R_B + r_B) + (R_E + r_E)\right) \tag{A.2}$$

when the current gain is greater than unity as in forward active mode.

In order to evaluate the order of magnitude of $f(J_C, T)$, it is possible to assume that the internal resistances r_B and r_E are temperature independent. This leads to

$$f(J_C, T) = AJ_C(R_B + r_B)\frac{\partial}{\partial T}\left(\frac{1}{\beta}\right)\Big|_{J_C}. \tag{A.3}$$

The current gain β increases as temperature increases [31], and this dependence can be described by means of the following law [32]:

$$\beta(T) = \beta_0 \exp\left[-\frac{\Delta E_G(N_E)}{k}\left(\frac{1}{T} - \frac{1}{T_0}\right)\right] \tag{A.4}$$

where β_0 is the current gain at ambient temperature and $\Delta E_G(N_E)$ is the emitter bandgap narrowing [20]. On the basis of the expression given by (A.4), the function $f(J_C, T)$ becomes

$$f(J_C, T) \cong -AJ_C(R_B + r_B)\frac{\Delta E_G(N_E)}{\beta k T^2}. \tag{A.5}$$

In the absence of base ballasting resistors

$$f(J_C, T) \cong -AJ_C r_B \frac{\Delta E_G(N_E)}{\beta k T^2}. \tag{A.6}$$

By inserting $T = 300\ K$, typical values for N_E, r_B, A, and J_C and applying the Slotboom formula to evaluate the bandgap narrowing for a given emitter doping, values of about 10^{-5} V/K are obtained. Therefore, this term is two orders of magnitude smaller than φ_{int} and stays small even if an external base ballasting resistor is present.

APPENDIX B

In this appendix, (12)–(15), that give an analytical formulation of ΔT_{crit}, are derived from the condition given in (10)

$$\frac{dV_{\mathrm{BEext}}}{dJ_C}\Big|_{V_{\mathrm{CBext}}} = \frac{\partial V_{\mathrm{BEext}}}{\partial J_C}\Big|_{V_{\mathrm{CBext}},T} + \frac{\partial V_{\mathrm{BEext}}}{\partial T}\Big|_{V_{\mathrm{CBext}},J_C}\frac{dT}{dJ_C}\Big|_{V_{\mathrm{CBext}}} = 0. \tag{B.1}$$

Moreover, it is apparent that

$$\frac{dT}{dJ_C}\Big|_{V_{\mathrm{CBext}}} = \frac{\partial T}{\partial J_C}\Big|_{V_{\mathrm{CBext}},V_{\mathrm{BEext}}} + \frac{\partial T}{\partial V_{\mathrm{BEext}}}\Big|_{V_{\mathrm{CBext}},J_C}\frac{dV_{\mathrm{BEext}}}{dJ_C}\Big|_{V_{\mathrm{CBext}}}. \tag{B.2}$$

By substituting (B.2) into (B.1), (10) becomes equivalent to

$$\frac{\partial V_{\mathrm{BEext}}}{\partial J_C}\Big|_{V_{\mathrm{CBext}},T} + \frac{\partial V_{\mathrm{BEext}}}{\partial T}\Big|_{V_{\mathrm{CBext}},J_C}\frac{\partial T}{\partial J_C}\Big|_{V_{\mathrm{CBext}},V_{\mathrm{BEext}}} = 0. \tag{B.3}$$

The first differential term from (B.3) can be derived using (2) and (4)

$$\frac{\partial V_{\mathrm{BEext}}}{\partial J_C}\Big|_{V_{\mathrm{CBext}},T} = AR_{\mathrm{EB}} + \frac{kT_{\mathrm{crit}}}{q}\frac{1}{J_{\mathrm{C,crit}}}. \tag{B.4}$$

The second differential term from (B.3) is given by (5) and the third one can be derived using (1) and (3)

$$\frac{\partial T}{\partial J_C}\Big|_{V_{\mathrm{CBext}},V_{\mathrm{BEext}}} = \frac{\Delta T_{\mathrm{crit}}}{J_{\mathrm{C,crit}}} - A^2 J_{\mathrm{C,crit}} R_{\mathrm{EC}} R_{\mathrm{TH}}. \tag{B.5}$$

Equation (B.3) can then be written as

$$\Delta T_{\mathrm{crit}} = T_{\mathrm{crit}} - T_0 = \frac{\frac{kT_{\mathrm{crit}}}{q}}{|\varphi_{ext}(J_{\mathrm{C,crit}})|} + \frac{AJ_{\mathrm{C,crit}}R_{\mathrm{EB}}}{|\varphi_{ext}(J_{\mathrm{C,crit}})|} + A^2 J_{\mathrm{C,crit}}^2 R_{\mathrm{EC}} R_{\mathrm{TH}} \tag{B.6}$$

which is equivalent to

$$\Delta T_{\mathrm{crit}} = \frac{\frac{kT_0}{q}}{|\varphi_{ext}(J_{\mathrm{C,crit}})| - \frac{k}{q}} + \frac{V_{\mathrm{BEext,crit}} - V_{\mathrm{BEint,crit}}}{|\varphi_{ext}(J_{\mathrm{C,crit}})| - \frac{k}{q}} + \frac{A^2 J_{\mathrm{C,crit}}^2 R_{\mathrm{EC}} R_{\mathrm{TH}}}{1 - \frac{\frac{k}{q}}{|\varphi_{ext}(J_{\mathrm{C,crit}})|}}. \tag{B.7}$$

ACKNOWLEDGMENT

The authors would like to acknowledge the DIMES IC-Processing Group, in particular H. Schellevis and H. W. van Zeijl, for their contributions to the silicon-on-glass device fabrication, T. Nathoeni and W. Verveer for assistance with electrical measurements, and V. Zieren and D. B. de Mooij for performing the nematic liquid crystal thermomapping measurements.

REFERENCES

[1] L. K. Nanver, N. Nenadović, V. d'Alessandro, H. Schellevis, H. W. van Zeijl, R. Dekker, D. B. de Mooij, V. Zieren, and J. W. Slotboom, "A back-wafer contacted silicon-on-glass integrated bipolar process—Part I: The conflict electrical versus thermal isolation," *IEEE Trans. Electron Devices*, pp. 42–50, Jan., 2004.

[2] C. G. Thornton and C. D. Simmons, "A new high current mode of transistor operation," *IRE Trans. Electron Devices*, vol. ED–5, pp. 6–10, 1958.

[3] H. A. Schafft and J. C. French, "'Second breakdown' in transistors," *IRE Trans. Electron Devices*, vol. 9, pp. 129–136, 1962.

[4] ——, "A survey of second breakdown," *IEEE Trans. Electron Devices*, vol. ED–13, pp. 613–618, Aug./Sept. 1966.

[5] H. Melchior and M. J. O. Strutt, "Secondary breakdown in transistors," *Proc. IEEE*, vol. 52, pp. 439–440, 1964.

[6] A. C. English, "Mesoplasmas and 'second breakdown' in silicon junctions," *Solid-State Electron.*, vol. 6, pp. 511–521, 1963.

[7] A. Amerasekera, M.-C. Chang, J. A. Seitchik, A. Chatterjee, K. Mayaram, and J.-H. Chern, "Self-heating effects in basic semiconductor structures," *IEEE Trans. Electron Devices*, vol. 40, pp. 1836–1844, Oct. 1993.

[8] R. H. Winkler, "Thermal properties of high-power transistors," *IEEE Trans. Electron Devices*, vol. ED–14, pp. 260–263, May 1967.

[9] W. Liu, S. Nelson, D. G. Hill, and A. Khatibzadeh, "Current gain collapse in microwave multifinger heterojunction bipolar transistors operated at very high power densities," *IEEE Trans. Electron Devices*, vol. 40, pp. 1917–1927, Nov. 1993.

[10] W. Liu, "Thermal coupling in 2-finger heterojunction bipolar transistors," *IEEE Trans. Electron Devices*, vol. 42, pp. 1033–1038, June 1995.

[11] B. Krabbenborg, "Modeling and Simulation of Electrothermal Interaction in Bipolar Transistors," Ph.D. dissertation, Univ. of Twente, Enschede, The Netherlands, 1996.

[12] L. L. Liou, B. Bayraktaroglu, and C.-I. Huang, "Theoretical thermal runaway analysis of heterojunction bipolar transistors: junction temperature rise threshold," *Solid State Electron.*, vol. 39, no. 1, pp. 165–172, 1996.

[13] W. Liu and A. Khatibzadeh, "The collapse of current gain in multifinger heterojunction bipolar transistors: its substrate temperature dependence, instability criteria, and modeling," *IEEE Trans. Electron Devices*, vol. 41, pp. 1698–1707, Oct. 1994.

[14] J. Olsson, "selfheating effects in SOI bipolar transistors," *Microelectron Eng.*, vol. 56, pp. 339–352, 2001.
[15] P. A. H. Hart, Ed., *Bipolar and Bipolar-MOS Integration*. Amsterdam, The Netherlands: Elsevier, 1994, pp. 418–419.
[16] K. J. Negus, M. M. Yovanovich, and D. J. Roulston, "An introduction to thermal-electrical coupling in bipolar transistors," in *Proc. ASME-JSME Thermal Engineering Conf.*, 1987, pp. 395–401.
[17] C. Popescu, "Selfheating and thermal runaway phenomena in semiconductor devices," *Solid-State Electron.*, vol. 13, pp. 441–450, 1970.
[18] D. T. Zweidinger, S.-G. Lee, and R. M. Fox, "Compact modeling of BJT selfheating in SPICE," *IEEE Trans. Computer-Aided Design*, vol. 12, pp. 1368–1375, Sept. 1993.
[19] V. d'Alessandro and N. Rinaldi, "A critical review of thermal models for electrothermal simulation," *Solid State Electron.*, vol. 46, no. 4, pp. 487–496, 2002.
[20] J. W. Slotboom and H. C. de Graaff, "Measurements of bandgap narrowing in Si bipolar transistors," *Solid State Electron.*, vol. 19, pp. 857–862, 1976.
[21] ——, "Bandgap narrowing in silicon bipolar tranwsistors," *IEEE Trans. Electron Devices*, vol. ED–24, pp. 1123–1125, Aug. 1977.
[22] P. L. Pritchard, *Electrical Characteristics of Transistors*: McGraw-Hill, Inc., 1967.
[23] R. P. Arnold and D. S. Zoroglu, "A quantitative study of emitter ballasting," *IEEE Trans. Electron Devices*, vol. 21, pp. 385–391, July 1974.
[24] N. Rinaldi, "Small-signal operation of semiconductor devices including selfheating, with application to thermal characterization and instability analysis," *IEEE Trans. Electron Devices*, vol. 48, pp. 323–331, Feb. 2001.
[25] M. G. Adlerstein, "Thermal stability of emitter ballasted HBT's," *IEEE Trans. Electron Devices*, vol. 45, pp. 1653–1655, Aug. 1998.
[26] TMA Inc., MEDICI User's Manual, Palo Alto, California, 1992.
[27] J. J. Sparkes, "Voltage feedback and thermal resistance in junction transistors," in *Proc. IRE*, vol. 48, 1958, pp. 1305–1306.
[28] N. Nenadović, V. d'Alessandro, L. K. Nanver, N. Rinaldi, H. Schellevis, and J. W. Slotboom, "Analytical formulation and electrical measurements of selfheating in silicon BJTs," in *Proc. IEEE BCTM*, 2002, pp. 24–27.
[29] H. Hagino, J. Yamashita, A. Uenishi, and H. Haruguchi, "An experimental and numerical study on the forward biased SOA of IGBT's," *IEEE Trans. Electron Devices*, vol. 43, pp. 490–500, Mar. 1996.
[30] V. Khemka, V. Parthasarathy, R. Zhu, A. Bose, and T. Roggenbauer, "Experimental and theoretical analysis of energy capability of RESURF LDMOSFET's and its correlation with static electrical safe operating area (SOA)," *IEEE Trans. Electron Devices*, vol. 49, pp. 1049–1058, June 2002.
[31] P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 3rd ed. New York: Wiley, 1993, pp. 28–29.
[32] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. New York: Wiley, 1981, pp. 140–144.

Nebojša Nenadović (S'02) was born in Belgrade, Serbia and Montenegro, on September 13, 1976. He received the M.Sc. degree (cum laude) in electrical engineering from the University of Belgrade, Serbia and Montenegro in September 2000. He joined the Laboratory of Electronic Components, Technology and Materials of DIMES Research Institute, Delft, The Netherlands, where he is currently pursuing the Ph.D. degree.

During the summers of 1998 and 1999 he was involved in the investigation of the transitions in the quantum hall regime at the Department of Condensed Matter Physics of Weizmann Instite of Science, Israel. His research experience at the Department of Physical Electronics, Faculty of Electrical Engineering, University of Belgrade includes modeling and simulations of optoelectronic devices, in particular quatum-wire lasers. His current research interests are design, fabrication and characterization of BJTs and RF power MOSFETs in silicon and silicon-on-glass technology, and investigation of electrothermal interaction within semiconductor devices.

Mr. Nenadović received the Best Student Paper Awards for his contributions to the Topical RF Meeting in 2001, and the MIEL Conference in 2002.

Vincenzo d'Alessandro received the "laurea" degree in electrical engineering, and the Ph.D. degree from the University of Naples "Federico II," Naples, Italy, in 1999 and 2003, respectively.

From January 2002 to December 2002, he joined as a Visiting Scientist the ECTM Group at the University of Technology of Delft, The Netherlands, working on simulation and modeling of electrothermal effects in last-generation Silicon-On-Anything RF transistors. In February 2003, he taught a course in digital electronics at University "Federico II." His current research area is in electrothermal and thermal modeling/simulation of semiconductor devices, with particular regard to multicellular power VDMOSTs and GaAs/AlGaAs HBTs.

Lis K. Nanver (S'80–M'83) received the M.Sc. degree in physics in 1979 from the University of Aarhus, Aarhus, Denmark. In 1982 she received the Dr.ing. degree from the Ecole Nationale Superieure des Telcommunications, Paris, France, where she worked on the simulation of CCD structures. In 1987 she received her Ph.D. degree from the Delft University of Technology, Delft, The Netherlands, where she developed a medium-frequency BIFET process.

In 1988, she joined the DIMES IC Process Research Sector as Bipolar Process Research Manager. She became Associate Professor and later Professor with the Faculty of Electrical Engineering, Mathematics and Computer Science, Delft University of Technology, detached at Delft Institute of Microelectronics and Submicron Technology (DIMES) Technology Center in 1994 and 2001, respectively. Within the Laboratory of Electrical Components, Technology and Materials she manages the research on advanced Si-based devices that is mainly directed toward optimization and development of high-frequency Si BJT/SiGe HBT devices and the integration of passives. This research involves technologies such as AP/LPCVD epitaxy, dopant activation by excimer laser annealing and substrate transfer techniques.

Prof. Nanver has served on the committees of ESSDERC and BCTM.

Fabrizio Tamigi was born in Castellammare di Stabia, Italy, in 1973. He received the "laurea" degree in electrical engineering from the University of Naples "Federico II." He is currently pursuing the Ph.D. in Naples.

In 2002, he entered as an Erasmus student at Delft Institute of Microelectronics and Submicron Technology (DIMES), Delt University of Technology, the Netherlands. His present interests focus on thermal issues in power and integrated devices, and on novel silicon device manufacturing technologies.

Niccolò Rinaldi (M'95) graduated (cum laude) from the University of Naples "Federico II," Italy, in 1990, and received the Ph.D. degree in 1994.

In February 1994, he became a Research Assistant at the University of Naples "Federico II." From July 1996 to December 1996, he was Research Fellow at the University of Delft, The Netherlands, working on the modeling of high-speed bipolar devices. In November 1998 he has been appointed Associate Professor at the University of Naples "Federico II." Since November 2002 he has been Full Professor at the University of Naples. His present research interests include the modeling of bipolar and power MOS transistors, self-heating effects in solid-state circuits and devices, electrothermal simulation, and design of RF and microwave circuits and devices. He has authored or co-authored more than 50 publications in international journals and conferences.

Prof. Rinaldi has been a Reviewer for IEEE TRANSACTIONS ON ELECTRON DEVICES, Solid-State Electronics, Microelectronics Journal, IEEE ELECTRON DEVICE LETTERS, Fizika A and B, International Journal of Electronics, as well as for international conferences. He currently is Vice Chairman of the IEEE Electron Device Chapter (Central and South Italy Section).

Jan W. Slotboom (M'82) was born in Utrecht, The Netherlands, on December 26, 1942. He received the M.Sc. degree in electrical engineering from the Technical University of Delft, Delft, The Netherlands, in 1966, and the Ph.D. degree from the Technical University of Eindhoven, Eindhoven, The Netherlands, in 1977, performing his dissertation on two-dimensional numerical device simulation of bipolar transistors and pioneering experiments on bandgap-narrowing in heavily-doped silicon.

In 1967, he joined the Philips Research Laboratories, Eindhoven, where he worked on bipolar device modeling, numerical simultions, and experimental silicon device physics. He was involved in the development of CCD memories for video applications and exploratory research of high-density memories. His current research activities are on research of novel silicon devices (e.g., SiGe bipolar transistors), hot-carrier effects, and new memory cells. He has authored and co-authored over 70 papers and holds 17 patents. Since 1994, he has been a part-time Professor with the Delft Institute of Microelectronics and Submicron Technology (DIMES), Delt University of Technology.

Dr. Slotboom was a member of the Solid-State Devices Subcommittee of the IEDM in 1980, 1983,and 1984, respectively. He was Vice Chairman and Chairman of International Arrangements for Europe of the IEDM. He has served as a Program Subcommittee Member of the IEDM in 1991 and 1992 and of the BCTM 1995 Conference. He has been a member of the Technical Program Committee of the ESSDERC for the last six years.