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A Background Timing-Skew Calibration Technique for Time-Interleaved Analog-to-Digital Converters

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***Abstract*—This paper presents a background timing-skew calibration technique for time-interleaved analog-to-digital converters (ADCs). The timing skew between any two adjacent analog–digital (A/D) channels is detected by counting the number of zero crossings of the ADCs input while randomly alternating their sampling sequence. Digitally controlled delay units are adjusted to minimize the timing skews among the A/D channels caused by the mismatches among the clock routes. The calibration behaviors, including converging speed and timing jitter, are theoretically analyzed and verified with simulations. A 6-bit 16-channel ADC is used as an example.**

***Index Terms*—Analog–digital (A/D) conversion, calibration, timing.**

I. Introduction

A TIME-INTERLEAVED analog-to-digital converter (ADC) employs multiple analog–digital (A/D) conversion channels to increase the achievable sampling rate for a given IC technology. Fig. 1 shows a time-interleaved ADC consisting of M A/D channels, i.e., $\mathrm{ADC}_1, \mathrm{ADC}_2, \ldots, \mathrm{ADC}_M$. Operating at a clock rate of f_c, each A/D channel includes a sample-and-hold amplifier (SHA) for input sampling followed by a quantizer (QTZ) for amplitude digitization. Controlled by clocks with an identical frequency of f_c and M uniformly spaced phases $\phi_1, \phi_2, \ldots, \phi_M$, the M SHAs sample the input, $x(t)$, sequentially and periodically. The final digital output code $x[l]$ is produced by multiplexing the outputs from the A/D channels, $x_1[k], x_2[k], \ldots, x_M[k]$. Thus, with each A/D channel operating at a clock rate of f_c, the overall system's sampling rate becomes $f_s = M \times f_c$.

Although each A/D channel needs only to operate at the f_c clock rate, mismatched A/D characteristics among the channels can degrade the overall A/D resolution. Those mismatches include A/D offset error, A/D gain error, and sampling timing skew. Since those mismatches are sensitive only to temperature and supply voltage variations and vary slowly in time, there are techniques that can calibrate the mismatches in the background without interrupting the normal A/D operation [1], [2].

Consider only the timing-skew issue. If the input is a narrow-band signal, the skew information can be extracted directly from the digital outputs of the A/D channels [1], [2].

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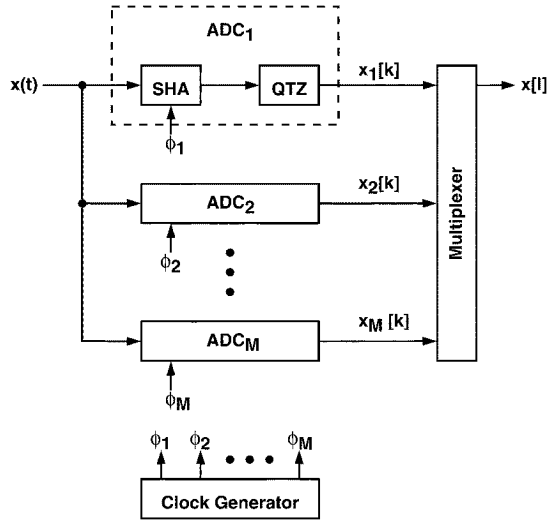

Fig. 1. Time-interleaved ADC architecture.

But these techniques cannot operate with a wide-band input that causes aliasing in each A/D channel. Using a single SHA can avoid the timing skew problem all together. But the SHA has to operate at a clock rate of $M \times f_c$. The timing skew can be calibrated by applying a reference signal to the ADC's input and then observing the phase difference between the outputs of adjacent A/D channels [3]. However, the calibration procedures cannot be performed without interrupting the normal A/D operation. It is possible to apply the reference signal for calibration during the normal A/D operation, and then separate the reference signal from the normal input by using correlation technique [4]. In this approach, the injected reference needs to be accurate and it also degrades the available dynamic range of the analog signal path.

This paper presents a background calibration scheme to correct the timing skew. It assumes that the M clocks from the local clock generator $\phi_1, \phi_2, \ldots, \phi_M$ are accurate and have uniformly spaced phases. The mismatches among the clock routes from the clock genertor to the SHAs cause the timing skews. The proposed scheme detects the timing skews by simply counting the number of zero crossings of input signal among the A/D channels while randomly changing their sampling sequence. The obtained informaton is used to adjust the digitally controlled delay units inserted between the clock generator and the SHAs, so that the timing skews can be minimized. The propoed technique allows inputs with wide bandwidth that can cause aliasing in each A/D channel. The maximum allowable bandwith for the input can be as high as $f_s/2$.

The rest of this paper is organized as follows. Section II introduces the principle of timing-skew detection. Section III describes the proposed calibration scheme between two A/D channels. Section IV describes the calibration scheme for a multi-channel ADC, which is based on the two-channel calibration scheme. Section V presents a 6-bit 16-channel ADC example. Finally, Section VI draws conclusions.

II. Timing-Skew Detection

Assuming all A/D channels shown in Fig. 1 are linear and without gain and offset errors, the digital output of the ADC_j can be expressed as

$$x_j[k] = x\left((M \times k + j)\,T_s + t_0 + \tau_j\right) \tag{1}$$

where $T_s = 1/f_s$ is the nominal sampling interval. The t_0 represents the initial sampling time at $k = 0$ for the ADC_1. The t_0 has a value between 0 and $M \times T_s$. The τ_j is the timing difference between the clock generator and the jth SHA caused by routing. The t_0 is defined in such a way that the mean of τ_j, for $j = 1, 2, \ldots M$, is zero, i.e., $\tau_1 + \tau_2 + \cdots + \tau_M = 0$. A timing skew occurs when $\tau_a \neq \tau_b$ for $a \neq b$. Notable, the sampling interval for each A/D channel is $T_c = M \times T_s$, and the clock frequency is $f_c = 1/T_c$. Equation (1) neglects the effects of amplitude quantization.

First assume that the sampling rate, f_s, is larger than the Nyquist sampling frequency of the $x(t)$ input, i.e., larger than twice the $x(t)$'s bandwidth. Since $x(t)$ is continuous in time and in amplitude, there is one and only one moment between two consecutive sampling instant that the $x(t)$ crosses over the zero if the input's values sampled by the corresponding A/D channels, ADC_j and the subsequent ADC_{j+1}, have opposite signs, i.e., $x_j[k] \times x_{j+1}[k] < 0$. Second, assume that the $x(t)$ is a stationary Gaussian process with zero mean. Then, the probability of a zero crossing between ADC_j and ADC_{j+1}, $P^z_{j,j+1}$, is a bivariate normal distribution [5], [6], and can be expressed as

$$P^z_{j,j+1} = \frac{1}{2} - \frac{1}{\pi}\sin^{-1}\rho_{j,j+1} \tag{2}$$

with

$$\rho_{j,j+1} = \frac{E[x_j \times x_{j+1}]}{\sigma_j \times \sigma_{j+1}} \tag{3}$$

where σ_j and σ_{j+1} are the standard deviations of the x_j and x_{j+1} random variables respectively. The $\rho_{j,j+1}$ of (3) denotes the cross-correlation between x_j and x_{j+1}.

The upper half of Fig. 2 illustrates the proposed timing-skew detection scheme. Two choppers, a clock chopper and a data chopper, are placed at the outputs of clock generator and at the outputs of the A/D channels. The two choppers are controlled by a binary-valued random sequence, $q[k] \in \{-1, +1\}$. When $q[k] = +1$, the choppers' outputs are the same as its corresponding inputs. When $q[k] = -1$, the choppers' outputs are exchanged. Thus, the sampling interval between the ADC_j and the ADC_{j+1} can be expressed as

$$\Delta T_{j,j+1} = T_s + q[k] \times (\tau_j - \tau_{j+1}). \tag{4}$$

As manifested by (7) and (8) shown later, the $P^z_{j,j+1}$ is a monotonic function of $\Delta T_{j,j+1}$ for an $x(t)$ input with limited bandwidth. Thus, the polarity of the timing skew $\tau_j - \tau_{j+1}$ can be detected by observing the change in $P^z_{j,j+1}$ whenever $q[k]$ changes. The $q[k]$ is chosen to be random to minimize the input dependence of the detection scheme. To ensure the detection accuracy, it is critical that the clock chopper in Fig. 2 does not introduce additional timing skew.

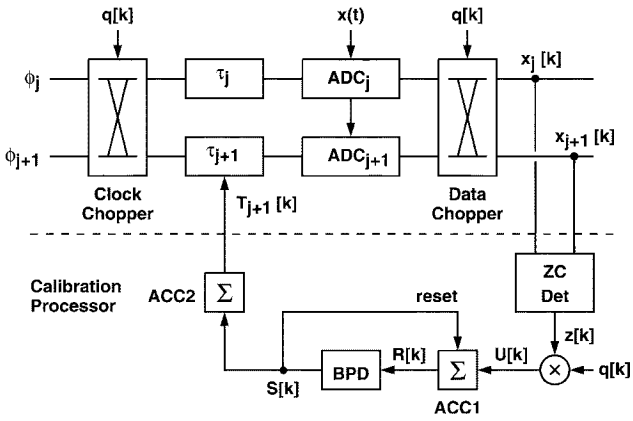

Fig. 2. Timing-skew detection and calibration for two channels.

III. Two-Channel Timing-Skew Calibration

The bottom half of Fig. 2 shows the block diagram of the proposed timing-skew calibration processor (CP) between the two adjacent A/D channels ADC_j and ADC_{j+1}. Since only the polarity of the $\tau_j - \tau_{j+1}$ timing skew can be detected, this CP empolys a similiar approach used in a comparator offset calibration scheme [7]. For the zero-crossing detector (ZC Det), its output $z[k] = 1$ whenever $x_j[k] \times x_{j+1}[k] < 0$, otherwise $z[k] = 0$. The $z[k]$ sequence is then correlated with the $q[k]$ sequence and integrated on the ACC1 accumulator. The ACC1s output is $R[k]$. The rate of long-term change in $R[k]$ is proportional to the probability difference, $\Delta P^z_{j,j+1}$

$$\Delta P^z_{j,j+1} = P^z_{j,j+1}\big|_{q[k]=+1} - P^z_{j,j+1}\big|_{q[k]=-1}. \tag{5}$$

The bilateral peak detector (BPD) monitors the value of $R[k]$ and generates a corresponding triple-valued output $S[k] \in \{+1, 0, -1\}$. The BPD has two thresholds $+N_C$ and $-N_C$. When $R[k] > +N_C$, $S[k] = +1$. When $R[k] < -N_C$, $S[k] = -1$. Otherwise, $S[k] = 0$. In addition, the ACC1 accumulator is reset to zero whenever $S[k] = +1$ or $S[k] = -1$. Thus, $-(N_C + 1) \leq R[k] \leq +(N_C + 1)$, and $S[k]$ can only remain as $+1$ or -1 for one clock cycle. The $S[k]$ sequence is integrated by the ACC2 accumulator. Its output, $T_{j+1}[k]$, controls the digitally controlled τ_{j+1} delay unit, such that

$$\tau_{j+1}[k] = \tau_{j+1,0} + \mu_t \times T_{j+1}[k] \tag{6}$$

where μ_t is the delay unit's step size for digital control and $\tau_{j+1,0}$ is the time delay of τ_{j+1} when $T_{j+1}[k] = 0$. The CP adjusts τ_{j+1} automatically to minimize the difference between τ_j and τ_{j+1}.

There are two design parameters in this calibration scheme, μ_t and N_C. Together with $P^z_{j,j+1}$ and $\Delta P^z_{j,j+1}$, they affect the calibration behaviors, such as the converging speed and the sampling jitter due to the disturbance of the $x(t)$ input. Detailed analyses have been given in [7]. Generally, large μ_t and small N_C result in fast converging speed but large timing jitter in τ_{j+1}.

On the other hand, small μ_t and large N_C result in small timing jitter but also slow converging speed.

The calibration behaviors strongly depend on the property of the $x(t)$ input. For a generic $x(t)$ input, the cross-correlation of (3) between two periodic sampling sequences, $x_a[k] = x(kt_c + t_0)$ and $x_b[k] = x(kt_c + t_s + t_0)$, can be expressed as $\rho(t_0, t_s, t_c)$. The t_c is the sampling interval for each of the sampling sequence, the t_s is the sampling time difference between the two sequences, and the t_0 is the initial sampling time for $x_a[0]$. Notably, the $\rho(t_0, t_s, t_c)$ is a periodic function of t_0 with a period of t_c. In the case of a time-interleaved ADC, we also have $t_s \leq t_c/2$. From (2), the corresponding zero-crossing probability between the two sampling sequences can be expressed as $P^z(t_0, t_s, t_c)$. Analogous to the probability density function, the zero-crossing density, defined as the zero-crossing probability per unit t_s time, can be expressed as

$$Z_R(t_0, t_c) \equiv \lim_{t_s \to 0} \frac{P^z(t_0, t_s, t_c)}{t_s} = \frac{1}{\pi} \times \left[-\frac{\partial^2 \rho(t_0, t_s, t_c)}{\partial t_s^2} \right]^{1/2} \Bigg|_{t_s = 0}. \quad (7)$$

For a M-channel time-interleaved ADC with T_s sampling interval between the adjacent channels, the single-channel sampling interval is $T_c = M \times T_s$. Assume the timing skew between the ADC_j and the ADC_{j+1} is small, i.e., $\Delta\tau_j \equiv \tau_j - \tau_{j+1} \ll T_s$, the probability difference, $\Delta P^z_{j,j+1}$, can then be approximated by

$$\Delta P^z_{j,j+1} = [Z_R(t_0, T_c) + Z_R(t_0 + T_s, T_c)] \times \Delta\tau_j. \quad (8)$$

From (7), it can be shown that $Z_R(t_0, t_c) \geq 0$. Thus, $\Delta P^z_{j,j+1}$ has the same polarity as $\Delta\tau_j$. Furthermore, the zero-crossing probability can be expressed as

$$P^z_{j,j+1} = \int_{t_0}^{t_0 + T_s} Z_R(t, T_c) dt. \quad (9)$$

Both $P^z_{j,j+1}$ and $\Delta P^z_{j,j+1}$ are required in estimating the converging speed and timing jitter of the calibration process [7].

Consider the the system shown in Fig. 2. If $\Delta P^z_{j,j+1}/\Delta\tau_j = Z_R(t_0, T_c) + Z_R(t_0 + T_s, T_c)$ is a constant, then the system's transient behavior can be modeled as a single-pole system with a time constant expressed as [7]

$$\tau_c = \frac{N_C}{\mu_t} \times \frac{2}{Z_R(t_0, T_c) + Z_R(t_0 + T_s, T_c)}. \quad (10)$$

As an example, let $x(t)$ be a single-tone sine wave, i.e., $x(t) = A\sin(2\pi f_i t)$, which has a frequency of f_i and a constant amplitude of A. Its corresponding $\rho(t_0, t_s, t_c)$ is $\cos(2\pi f_i t_s)$, and the corresponding $Z_R(t_0, t_c)$ can be expressed as

$$Z_R(t_0, t_c) = \begin{cases} 2f_i, & \frac{f_i}{f_c} \neq \frac{a}{b} \\ \sum_{n=0}^{a-1} \frac{2}{b} \delta\left(t_0 - n \cdot \frac{t_c}{a}\right), & \frac{f_i}{f_c} = \frac{a}{b}\ b \text{ is even} \\ \sum_{n=0}^{2a-1} \frac{1}{b} \delta\left(t_0 - n \cdot \frac{t_c}{2a}\right), & \frac{f_i}{f_c} = \frac{a}{b}\ b \text{ is odd} \end{cases} \quad (11)$$

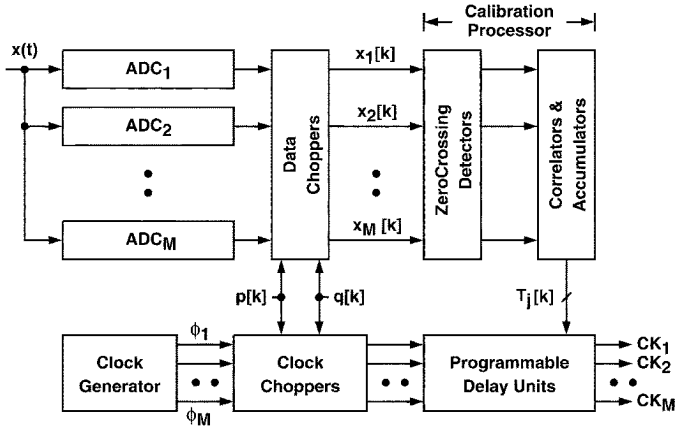

Fig. 3. Full-system timing-skew calibration.

where $f_c = 1/T_c$ is the sampling rate for a single channel, and a and b are two mutually prime positive integers. If the f_i/f_c ratio is irrational, i.e., $f_i/f_c \neq a/b$, the zero-crossing density, Z_R, is equal to $2f_i$, and independent of t_0 and t_c. If $f_i/f_c = a/b$, the input sine wave synchronizes with the f_c sampling clock. Thus, within any time period of the f_c clock, there are only a finite number of instants at which the zero-crossings can occur. If b is even, there are a possible uniformly spaced zero-crossing instants. On the other hand, if b is odd, there are $2a$ possible uniformly spaced zero-crossing instants. The proposed timing-skew calibration scheme cannot function properly with a synchronous input, unless the coressponding a is sufficiently large so that the time interval between the zero-crossings is smaller than the required timing resolution.

IV. Multi-Channel Timing-Skew Calibration

Fig. 3 shows the calibration scheme for the entire M-channel time-interleaved ADC. The clock generator produces M clocks with an identical frequency of f_c and equally spaced phases. The clocks pass through the clock choppers and the digitally controlled delay units to generate $\mathrm{CK}_1, \mathrm{CK}_2, \ldots, \mathrm{CK}_M$ which control the sampling timing of $\mathrm{ADC}_1, \mathrm{ADC}_2, \ldots, \mathrm{ADC}_M$ repectively. The calibration processor (CP) adjusts the digitally controlled delay units to minimize the timing skews among the A/D channels. The timing skews are caused by mismatches among the clock routes from the outputs of clock choppers to the sample-to-hold amplifiers in the A/D channels. The CP is pure digital and operate at a clock rate of f_c. It consists of only comparators, adders and registers, and requires no multi-bit multiplier.

A pairing scheme is proposed so that 1) the two-channel timing-skew calibration can be executed simultaneously on the selected pairs of A/D channels; 2) each clock chopper only swaps the sampling clocks of adjacent A/D channels; and 3) timing skews of all A/D channels are minimized relative to a single reference channel. As shown in Fig. 3, there are two independent random sequences, $p[k] \in \{-1, +1\}$ and $q[k] \in \{-1, +1\}$ for the control of the clock choppers and the data choppers. Fig. 4 illustrates the proposed pairing scheme

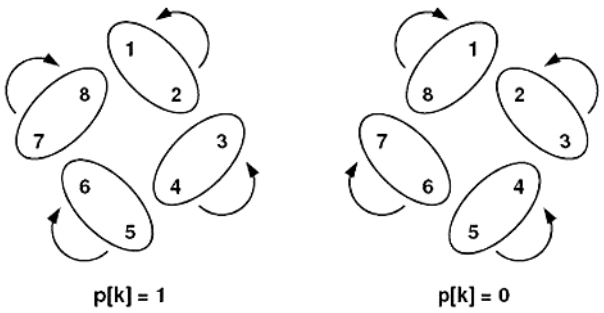

Fig. 4. Proposed pairing scheme for an 8-channel system.

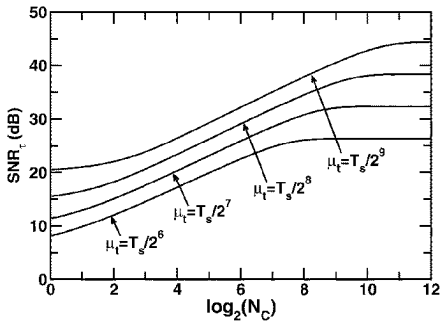

Fig. 5. SNR_τ versus N_C and μ_t for the 6-bit 16-channel ADC example.

for an 8-channel time-interleaved ADC. When $p[k] = +1$, the following calibration pairs are selected for simultaneous calibration: (1, 2), (3, 4), (8, 7), (6, 5). For each calibration pair, (a, b), the $q[k]$ sequence toggles the corresponding choppers to altenerate the sampling sequence of ADC_a and ADC_b. The CP then adjusts the bth delay unit to minimized the timing skew between the two channels. When $p[k] = -1$, the following calibration pairs are selected for simultaneous calibration: (2, 3), (4, 5), (1, 8), (7, 6). This pairing scheme assigns ADC_1 as the reference channel. For other A/D channel, its corresponding delay unit is ajusted so that its timing skew with the reference channel is eventually minimized.

In the above pairing scheme, the sampling interval of each individual A/D channel is no longer a constant MT_s, due to the reordering of the sampling sequence. The two random sequences, $p[k]$ and $q[k]$, are operated at the f_c clock, and they can change state only after the present state has been applied to all A/D channels. If $p[k]$ is restricted to change only during $q[k] = +1$, the sampling interval for each A/D channel can be confined to vary between $(M-1)T_s$ and $(M+1)T_s$.

Consider only the timing jitter caused by the calibration process using the pairing scheme just described. Let ADC_1 be the reference channel in a M-channel ADC, and all calibration pairs employ identical μ_t and N_C parameters. Since ADC_1 is the reference channel, the corresponding τ_1 is not adjusted, thus its jitter standard deviation $\sigma(\tau_1) = 0$. For ADC_2, the corresponding τ_2 is adjusted toward τ_1, resulting in a jitter standard deviation of $\sigma(\tau_2)$. For ADC_3, the corresponding τ_3 is adjusted toward τ_2, resulting in a jitter standard deviation of $\sqrt{2}\sigma(\tau_2)$. In general, for ADC_{j+1} where $j \geq 2$, the corresponding τ_{j+1} is adjusted toward τ_j, and its jitter standard deviation can be expressed as

$$\sigma(\tau_{j+1}) = \sqrt{j} \times \sigma(\tau_2). \tag{12}$$

On the other side of ADC_1, ADC_M has the same jitter standard deviation as ADC_2, ADC_{M-1} has the same jitter standard deviation as ADC_3, and etc. In the 8-channel example, the ADC_5 has largest timing jitter. To reduce $\sigma(\tau_{j+1})$, the CP can use larger N_C value when calibrating the timing skew of the ADC_{j+1}.

In the proposed pairing sheme for multichannel calibration, the use of the p random sequence increases the response time of the system by a factor of two. If $\Delta P^z_{j,j+1}/\Delta\tau_j = Z_R(t_0, T_c) + Z_R(t_0 + T_s, T_c)$ is a constant, then the system's transient behavior can also be modeled as a single-pole system with a time constant expressed as

$$\tau_s = 2\tau_c \tag{13}$$

where τ_c is defined in (10).

It is imperative to carefully choose the timing of $p[k]$ and $q[k]$ for controlling the clock choppers, so that undesirable glitches are not generated in the clocks when the choppers are toggled.

V. 6-Bit 16-Channel Design Example

A 6-bit 16-channel ADC, i.e., $M = 16$, is used as a design example. The sampling interval between the adjacent channels is T_s, and the sampling period for each channel is $T_c = M \times T_s = 16T_s$. The single-channel sampling rate is $f_c = 1/T_c$ and the effective sampling rate for the entire ADC is $f_s = 1/T_s$. The ADC is similiar to the system illustrated in Fig. 4 and employs the pairing scheme described in Section IV. Identical μ_t and N_C parameters are used in all calibration procedures. The input is assumed to be an asynchronous sine wave, i.e., $x(t) = A\sin(2\pi f_i t)$ and the f_i/f_c ratio is irrational. From (11), the corresponding zero-crossing density is $Z_R = 2f_i$.

Consider the timing jitter caused by the CP. Besides μ_t and N_C, the jitter standard deviations depend only on the $\Delta P^z_{j,j+1}/P^z_{j,j+1}$ ratio [7]; thus, it is not a function of the f_i input frequency for the single-tone input case. The ADC_1 is assigned as the reference channel, thus $\sigma(\tau_1) = 0$. Both the ADC_2 and ADC_{16} have the same jitter standard deviation, i.e., $\sigma(\tau_2) = \sigma(\tau_{16})$. The value of $\sigma(\tau_2)$ can be calculated from μ_t and N_C [7]. For other A/D channels, their corresponding jitter standard deviation can be calculated using (12). The ADC_9 is the most remote A/D channel away from the ADC_1; it has the worst-case jitter of $\sigma(\tau_9) = \sqrt{8} \times \sigma(\tau_2)$.

Assume the ADC's output contains only noises caused by sampling timing skew. Then, the output's signal-to-noise ratio can be expressed as

$$\mathrm{SNR}_\tau = \frac{1}{4\pi^2 f_i^2 \sigma^2(\tau)} \tag{14}$$

where $\sigma^2(\tau)$ is the timing-skew standard deviation. Fig. 5 shows the calculated SNR_τ against different values of N_C and μ_t for the 16-channel ADC example. The input frequency is assumed

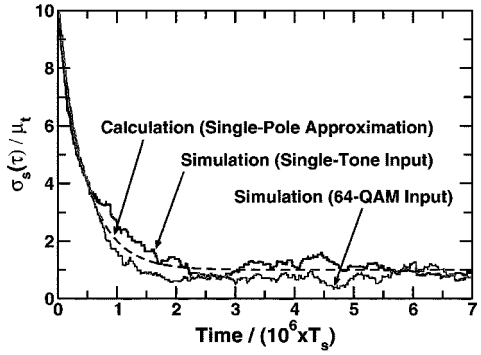

Fig. 6. Timing-skew settling behavior for the 6-bit 16-channel ADC example.

to be close to the Nyquist frequency, i.e., $f_i \approx f_s/2$. For this ADC example, the $\sigma^2(\tau)$ in (14) can be expressed as

$$\sigma^2(\tau) = \sum_{j=1}^{16} \sigma^2(\tau_j) = \sigma^2(\tau_2) \times \frac{1}{16} \sum_{j=-7}^{8} |j| = 4\sigma^2(\tau_2). \quad (15)$$

As N_C increases, SNR_τ is saturated to a value determined by the μ_t. To achieve 6-bit resolution, $N_C = 2^9$ and $\mu_t = T_s/2^8$ are chosen in this design example, In such case, $\sigma(\tau) \approx \mu_t$ and $\mathrm{SNR}_\tau \approx 37$ dB.

For the case of an asynchronous single-tone input with $Z_R = 2f_i$, the ADCs transient behavior can be modeled as a single-pole system with a time constant of $\tau_s = N_C/(f_i \times \mu_t)$, which is obtained using (13) and (10). Fig. 6 shows the settling behavior of the timing-skew spatial standard deviation, $\sigma_s(\tau)$ for this ADC example. The spatial standard deviation is collected by recording τ_j for $j = 1, 2, \ldots, 16$ at a given time. Calibration parameters are $N_C = 2^9$ and $\mu_t = T_s/2^8$. Results from both simulations and calculations using the single-pole model are shown in Fig. 6. For the single-tone simulation case, the input is a sine wave with a frequency of $(2345/8192)f_s \approx 0.29f_s$. The initial value for $\sigma_s(\tau)$ is set to $10\mu_t$. When settled, the steady-state $\sigma_s(\tau)$ is close to $1\mu_t$. For the broad-band simulation case, the input is a 64-QAM signal. Its carrier has a frequency of $(2345/8192)f_s$. The symbols are a random sequence, and the symbol rate is $(1739/8192)f_s$. The settling behavior of the broad-band case is similar to that of the simulation case with a single-tone input at the carrier frequency.

In the single-tone simulation case, the ADC's output spectrum exhibits visible spurious tones before calibration, and the signal-to-noise-and-distortion ratio (SNDR) is calculated to be 23.1 dB. When the calibration is turned on, all the visible tones are suppressed and the SNDR is improved to 37.0 dB, as predicted in Fig. 5. For the broad-band simulation case, the SNDR of the ADCs output is 22.4 dB before calibration, and is improved to 36.1 dB when the calibration is turned on.

VI. Effects of Gain/Offset Mismatches

Since only the zero crossings are collected in the the proposed timing-skew calibration scheme, the inter-channel gain mismatches do not affect the calibration behaviors. However, depending on the input condition, the calibration effectiveness may be sensitive to the offset mismatches. Consider two adjacent A/D channels, ADC_j and ADC_{j+1}. If the ADC_j has an input offset of 0 while the ADC_{j+1} has an input offset of O_{j+1}, the zero-crossing probability between the two channels, $P^z_{j,j+1}$, is deviated from (2) by an amount of $\delta P^z_{j,j+1}$. The $\delta P^z_{j,j+1}$ can be approximated by

$$\delta P^z_{j,j+1} \approx \frac{\rho_{j,j+1}}{2\pi\sqrt{1-\rho^2_{j,j+1}}} \times \frac{O^2_{j+1}}{E\left[x^2_{j+1}\right]}. \quad (16)$$

If the input exhibits large $\rho_{j,j+1}$ cross-correlation property, the $P^z_{j,j+1}$ is more sensitive to the offset mismatch. The offset sensitivity is reduced when large-power input is applied, since large-power input leads to large $E\left[x^2_{j+1}\right]$ value.

It is necessary to keep $\delta P^z_{j,j+1}$ of (16) much smaller than $\Delta P^z_{j,j+1}$ of (5), so that the analyzes of the previous sections can remain valid. There are calibration techniques that can minimize the offset mismatches [1], [8].

VII. Conclusion

The probability of input's zero crossing between two sampling channels is related to the cross-correlation of the sampled data, and can be expressed as a bivariate normal distribution. Theoretical analyzes can be carried out to estimate the converging speed and jitter behavior of the proposed calibration scheme, as well as its sensitivity to the inter-channel offset mismatch. The analyzes are valid even for wide-band input that causes aliasing in each A/D channel, as long as the zero-crossing density $Z_R(t_0, t_c)$ of (7) can be found.

The clock choppers and the digitally controlled delay units are crucial in this calibration scheme. The clock choppers must not cause additional timing skew and unwanted glitches in the clock signals. The delay units must provide the μ_t step size for digital control; and its adjustable range must cover all possible timing skew variations.

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