# A Bidirectional DC–DC Converter Topology for Low Power Application

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***Abstract*—This paper presents a bidirectional dc–dc converter for use in low power applications. The proposed topology is based on a half-bridge on the primary and a current-fed push-pull on the secondary side of a high frequency isolation transformer. Achieving bidirectional flow of power using the same power components provides a simple, efficient and galvanically isolated topology that is specially attractive for use in battery charge/discharge circuits in dc UPS. The dc mains (provided by the ac mains), when presented, powers the down stream load converters and the bidirectional converter which essentially operates in the buck mode to charge the battery to a nominal value of 48 V. On failure of the dc mains (derived from the ac mains), the converter operation is comparable to that of a boost and the battery regulates the bus voltage and thereby provides power to the downstream converters. Small signal and steady state analyzes are presented for this specific application. The design of a laboratory prototype is included. Experimental results from the prototype, under different operating conditions, validate and evaluate the proposed topology. An efficiency of 86.6% is achieved in the battery charging mode and 90% when the battery provides load power. The converter exhibits good transient response under load variations and switchover from one mode of operation to another.**

***Index Terms*—Bidirectional power flow, currend fed push-pull, dc UPS.**

## I. Introduction

BI-DIRECTIONAL dc–dc converters allow transfer of power between two dc sources, in either direction [1]–[4]. Due to their ability to reverse the direction of flow of current, and thereby power, while maintaining the voltage polarity at either end unchanged, they are being increasingly used in applications like dc uninterruptable power supplies, battery charger circuits, telecom power supplies and computer power systems.

Possible implementation of bidirectional converters using resonant [4], soft switching [5]–[7] and hard switching PWM [8] has been reported in literature. But, these topologies may often lead to an increase in component ratings, circuit complexity and conduction losses in resonant mode implementations, high output current ripple and loss of soft switching at light loads for soft switched circuits, and lack of galvanic isolation in integrated topologies.

This paper presents a bidirectional dc–dc converter topology for application as battery charger/discharger. The proposed converter, Fig. 1, is a combination of two well-known topologies, namely half-bridge and current-fed push-pull. The proposed converter provides the desired bidirectional flow of power for battery charging and discharging using only one transformer, as opposed to two in conventional schemes. It utilizes the bidirectional power transfer property of MOSFET's. Other advantages of the proposed topology include (a) reduced part count due to use of the same components in both directions of power flow, (b) low stresses on the switches, (c) galvanic isolation, (d) low ripple in the battery charging current, (e) fast switchover on failure and reappearance of dc mains, and (f) minimal number of active switches.

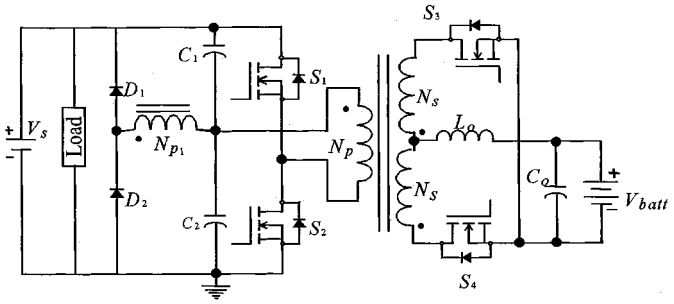


Fig. 1. Basic power topology for proposed bidirectional dc–dc converter.

The paper also provides detailed steady state and small signal analyzes for both topological modes. A generalized design procedure is given that facilitates design of the converter by making use of design curves.

The paper is organized as follows: Section II presents the description, operating modes and the control principle of the converter. Steady state analysis for a normalized converter and important design guidelines are discussed in Section III. The small signal analysis is provided in Section IV. A design example using the design curves and the design procedure outlined in Sections III and IV is presented in Section V. Key experimental results in Section VI provide verification of the proposed topology.

## II. Topology, Modes of Operation and Control Principle

### A. Power Topology

The basic power circuit topology is shown in Fig. 1. The transformer provides galvanic isolation between the dc mains and the battery. The primary side of the converter is a half bridge and is connected to the dc mains. The secondary side, connected to the battery, forms a current-fed push-pull.

The converter has two modes of operation. In the *forward/charging mode* the energy from the dc mains charges the

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battery over a specified input voltage range while powering the down stream load converters. In this mode of operation only the switches $S_1$ and $S_2$ are gated and the body diodes of the switches $S_3$ and $S_4$ provide battery side rectification. On failure of the dc mains, reversal of power flow occurs resulting from a switchover to the battery. Now, the battery supplies the load power at the dc bus voltage. In this *backup/current-fed mode*, the switches $S_3$ and $S_4$ are gated and the body diodes of the switches $S_1$ and $S_2$ provide rectification at the load side.

The use of the half-bridge and current-fed topologies over other possible configurations can be justified as follows. Switches in the off state in half and full-bridge topologies are subject to a voltage stress equal to the dc input voltage and not twice that as in the push-pull and single ended forward converters. In low power applications the two-switch half-bridge is preferred over the four-switch full-bridge topology. A two-switch double ended forward with voltage stress across the switches equal to the dc input voltage, provides a half wave output at its secondary, compared to a full wave in the half-bridge converter. Thus, the square wave frequency in the half-bridge secondary winding is twice that in the forward, thereby allowing a smaller output LC filter. The primary winding of the transformer in a half-bridge sustains half the supply voltage compared to the full dc voltage for the forward converter, implying half the number of turns on the primary. This allows full copper utilization of the half-bridge transformer, low number of primary winding turns, and reduction in its size and cost. For the secondary side converter, the current-fed push-pull is the most suitable topology that utilizes the presence of the output filter inductor of the half-bridge converter. Equal division of inductor current between switches during their overlap period reduces the average and rms values of the current flowing through them and also the rms current in the transformer secondary. A current-fed push-pull reduces the possibility of flux imbalance. It allows a wider range of input voltages, which is well suited for this specific case.

### B. Description of Operating Principle

*Forward/Charging Mode*: In this mode, Fig. 2, the dc mains, $V_s$, powering the load converters, provides the battery charging current, $i_{L_o}$. This charges the battery of the bidirectional converter at the nominal voltage. The switches $S_1$ and $S_2$ on the primary side are gated at duty ratios less than 0.5, while $S_3$ and $S_4$ are not switched at all. Operation of the bidirectional converter during this mode is comparable to that of a buck converter. Intervals $t_0$ to $t_4$, in the idealized waveforms of Fig. 4, describe the various stages of operation during one switching time period, $T_s$. The converter operation is repetitive in the switching cycle.

*Interval* $t_0$–$t_1$: Switch $S_2$ is OFF and $S_1$ is turned ON at time $t_0$. A voltage $V_s/2$ appears across the primary winding. The body diode of switch $S_4$, $D_{S_4}$, is forward biased and provides rectification on the secondary side. It also carries the battery charging current, $i_{\text{batt}}$. The primary current, $i_{S_1}$, builds up as it consists of the linearly increasing inductor current, $i_{L_o}$, reflected from the secondary, and the transformer primary magnetizing current.

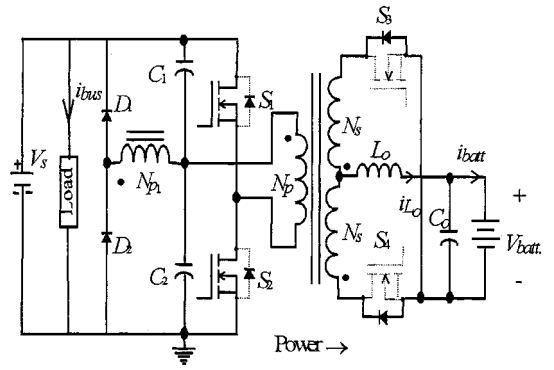



Fig. 2. Forward/charging mode ($V_S = 300$–$400$ V, $V_{\text{batt}} = 48$ V nominal).

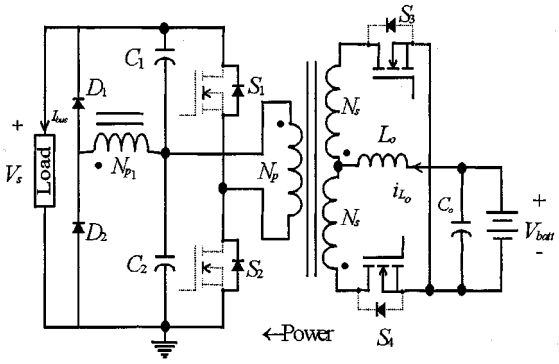



Fig. 3. Current-fed/backup mode ($V_{\text{batt}} = 48$ V nominal, $V_S = 350$ V).

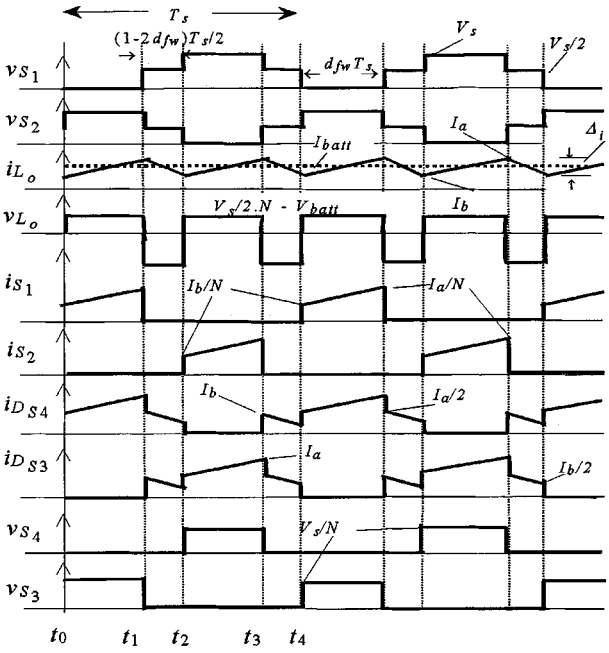



Fig. 4. Waveforms during the forward/charging mode.

*Interval* $t_1$–$t_2$: Switch $S_1$ is turned OFF at $t_1$ while $S_2$ continues to remain OFF. During this dead time interval there is zero voltage across the primary, and therefore secondary windings, and no power is transferred to the secondary side. The energy stored in $L_o$ results in the freewheeling of the current $i_{L_o}$, equally through the body diodes $D_{S_3}$ and $D_{S_4}$ to charge the

battery. Only half the supply voltage, $V_s$, appears across each switch $S_1$ and $S_2$ during this interval.

*Interval* $t_2$–$t_3$: Switch $S_2$ is turned ON at $t_2$ while $S_1$ continues to be in the OFF state. The operation is similar to that during interval $t_0$–$t_1$, but now the body diode of switch $S_3, D_{S_3}$, conducts and provides secondary side rectification. Inductor current, $i_{L_o}$, rises linearly again as the voltage across the inductor, $v_{L_o}$, increases. The switch body diode, $D_{S_3}$, carries the total battery charging current.

*Interval* $t_3$–$t_4$: The converter operation during this interval is similar to that in the interval $t_1$–$t_2$. No primary side switch is conducting and the battery charging current, is provided by the energy stored in the inductor. The body diodes of both the switches on the secondary side, $D_{S_3}$ and $D_{S_4}$, conduct simultaneously and equally.

Fig. 2 shows a balancing winding $N_{p_1}$ and two catching diodes $D_1$ and $D_2$ on the primary side of the half bridge. They maintain the centerpoint voltage at the junction of $C_1$ and $C_2$ to one half of the input voltage, $V_s$, and prevent a 'runaway' condition of staircase saturation of the transformer core. Such a condition may occur in current mode control when different amounts of charge are removed from the capacitors, $C_1$ and $C_2$, due to mismatches between the MOSFET's $S_1$ and $S_2$. Should the midpoint of $C_1$ and $C_2$ begin to drift, a small current, in mA, flows through $N_{p_1}$ and $D_1$ and $D_2$ to compensate for the drift. $N_{p_1}$ has the same number of turns as the winding $N_p$ and is phased in series with it through the ON time of $S_1$ and $S_2$.

*Backup/Current-fed Mode*: The converter operates in this mode, Fig. 3, on failure of the dc mains. The battery discharges to supply the load power. The switches $S_3$ and $S_4$ of the current-fed push-pull topology are driven at duty ratios greater than 0.5. The converter operation during this mode is described with reference to the waveforms presented in Fig. 5. As in the *charging mode*, inductor current is assumed to be continuous. The time intervals between $t_0$ to $t_4$ describe the converter operation, which is repetitive over a switching cycle, $T_s$.

*Interval* $t_0$–$t_1$: Switch $S_3$ is turned ON at time $t_0$ while $S_4$ remains in the ON state from the previous interval. The transformer secondary, $N_S$, is subject to an effective short circuit, which causes the inductor, $L_o$, to store energy as the total battery voltage appears across it. The inductor current, $i_{L_o}$, ramps up linearly and is shared equally by both $S_3$ and $S_4$. During this interval, the bulk capacitors, $C_1$ and $C_2$ provide the output load power load.

*Interval* $t_1$–$t_2$: $S_4$ is turned OFF at instant $t_1$ while $S_3$ continues to remain ON. The energy stored in the inductor, $L_o$, during the previous interval is now transferred to the load through the body diode $D_{S_2}$ and the diode $D_1$. Voltage across the auxiliary winding $N_{p_1}$ and the primary winding $N_p$ is identical due to their series phasing and equal number of turns. This allows simultaneous and equal charging of both $C_1$ and $C_2$ through $D_1$ and $D_{S_2}$, respectively.

*Interval* $t_2$–$t_3$: This interval is similar to interval $t_0$–$t_1$. Switch $S_3$ remains ON and $S_4$ is also turned ON at time $t_2$. The duty ratio for $S_3$ is therefore greater than 0.5. With both $S_3$ and $S_4$ turned ON, the transformer secondary is effectively shorted and the inductor stores energy, resulting in a linear rise in its current, $i_{L_o}$. Voltage across both $N_p$ and $N_{p_1}$ is zero, so load power is supplied by the discharge of the bulk capacitors.

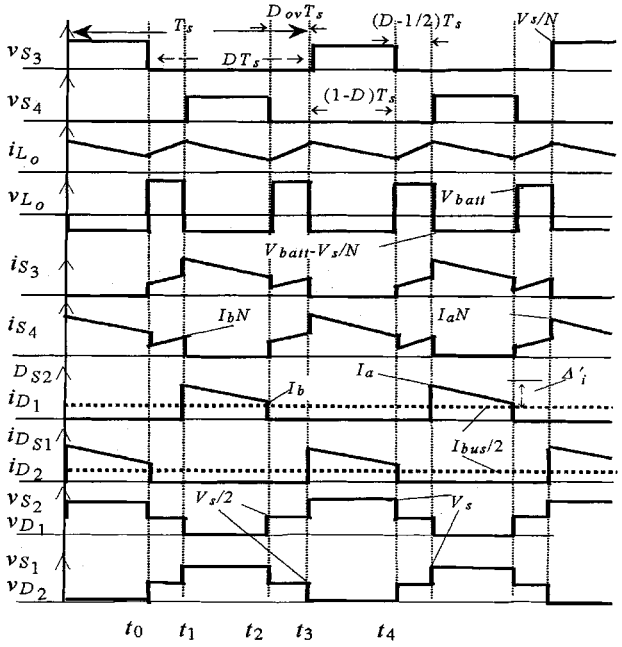



Fig. 5. Waveforms during the backup/current-fed mode.

*Interval* $t_3$–$t_4$: Converter operation during this interval resembles that during the interval $t_1$–$t_2$. $S_4$ remains ON and $S_3$ is turned OFF at $t_3$. The stored energy of $L_o$ is transferred to the primary side of the converter through the switch conducting on the secondary side, $S_4$, and the primary diodes $D_{S_1}$ and $D_2$. The conduction of $D_{S_1}$ and $D_2$ again results in equal charging of $C_1$ and $C_2$, respectively.

### C. Control Principle

Current mode control is used for both modes of converter operation. This allows

1) a pulse by pulse monitoring and limiting of current, thus avoiding flux imbalance in the transformer;
2) fast regulation to input voltage variation;
3) enhanced load regulation due to greater error amplifier bandwidth;
4) minimal external parts.

## III. Steady State Analysis and Design Guidelines

The steady state operation of the converter in both modes is analyzed to enable selection of the components. This analysis is based on the idealized waveforms shown in Figs. 4 and 5 and provides the basic design equations. The design equations correspond to the worst case operating conditions to ensure suitable operation of the converter over the desired operating range. The variables used in the analysis are defined in the idealized waveforms. The circuit parameters are normalized so that the results are valid over a wide range of operating conditions. Design curves that allow selection of components are presented in Figs. 6–15. Some practical considerations that must be accounted for while selecting components for the prototype setup

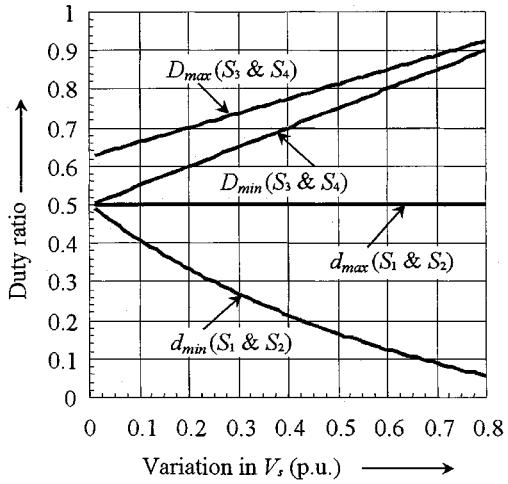



Fig. 6. Duty ratios for switches $S_1$ to $S_4$.

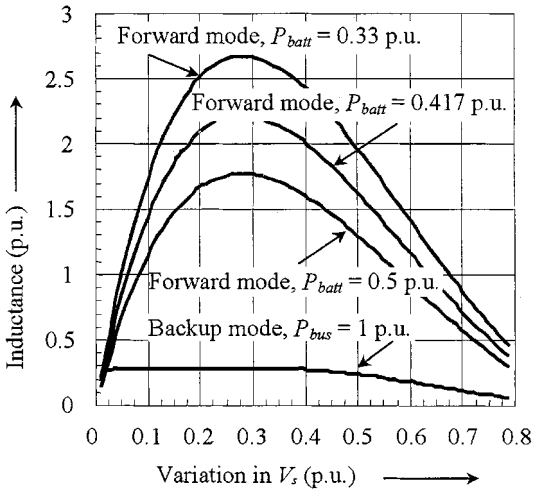



Fig. 7. Minimum inductance, $L'_{o_{\min}}$, at minimum load.

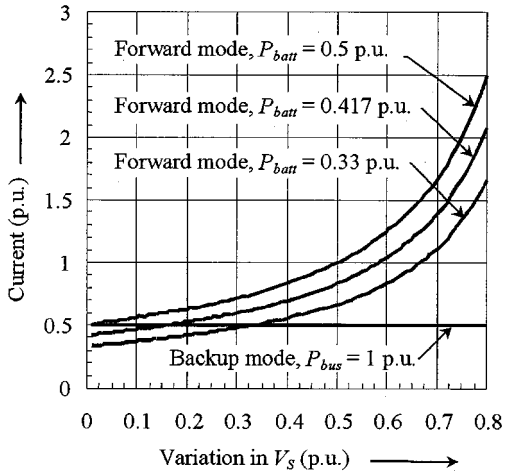



Fig. 8. Average current through $S_1$ and $S_2$.

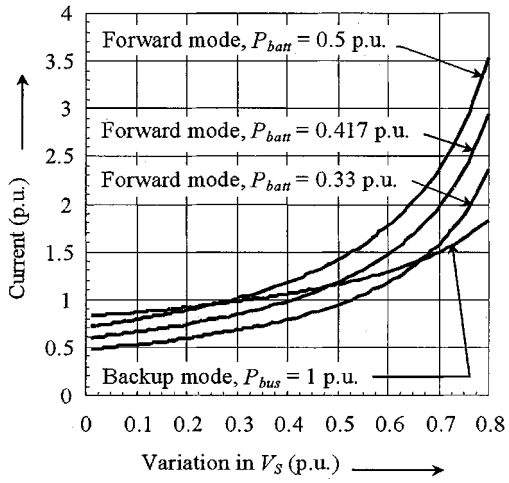



Fig. 9. RMS currents through $S_1$ and $S_2$.

are also presented. For the final selection, one must bear in mind the dual set of constraints arising from use of the same power circuit for both the operating modes and therefore choose the components accordingly.

The following assumptions are made to aid the analysis:

1) the circuit is operating in steady state, implying that all voltages and currents are periodic;
2) the switches and diodes are ideal;
3) the transformer is ideal with unity turns ratio;
4) all parameters are normalized and referred to the primary side and the reflected secondary side parameters are denoted with a prime "*′*;"
5) suitable approximations are made for the converter efficiency in both operating modes for the preliminary analysis.

The output power of the converter during battery charging mode is usually between one-third to one-half the power delivered in the *backup mode*.

The base quantities to obtain the normalized expressions are defined as follows:

1 p.u. voltage, $V_{\text{base}} = V_S$ volts (output voltage at the dc bus in the *backup mode*)

1 p.u. power, $P_{\text{base}} = P_{\text{bus}}$ watts (output power to the dc bus in the *backup mode*)

1 p.u. frequency, $f_{\text{base}} = f_s$ Hz (converter operating frequency in the *backup mode*).

The other base quantities like those for impedance and current are derived from the ones defined above.

1 p.u. current, $I_{\text{base}} = P_{\text{bus}}/V_S$ amps (base value for current)

1 p.u. inductance, $L_{\text{base}} = P_{\text{bus}}/2\pi f_s$ henries (base value for inductance)

1 p.u. capacitance, $C_{\text{base}} = 1/2\pi f_s P_{\text{bus}}$ farads (base value for capacitance).

The duty ratios of all four switches must be determined in order to calculate other circuit parameters. The constraints to be borne in mind are that the output (battery) voltage in the *forward mode* can at most be equal to half the input dc bus voltage and in the *backup mode* the output voltage (at the dc bus) must be atleast equal to the input (battery) voltage. Also, the maximum theoretical duty ratio of $S_1$ and $S_2$ in the *forward mode* must be less than 0.5 while the minimum theoretical duty ratio of $S_3$ and $S_4$ in the *backup mode* must be greater than 0.5. The duty ratios are dependant on the voltages at the input and the output in both operating modes.

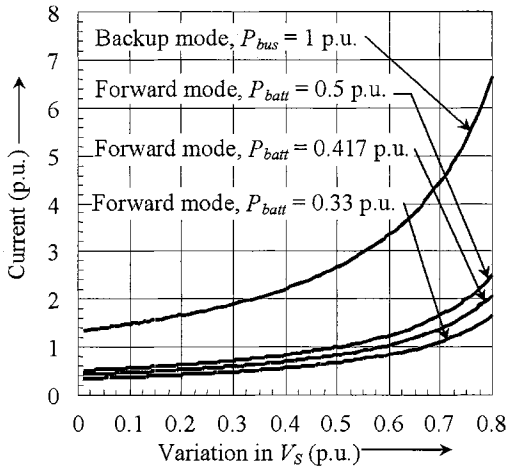



Fig. 10. Average currents through $S_3$ and $S_4$.

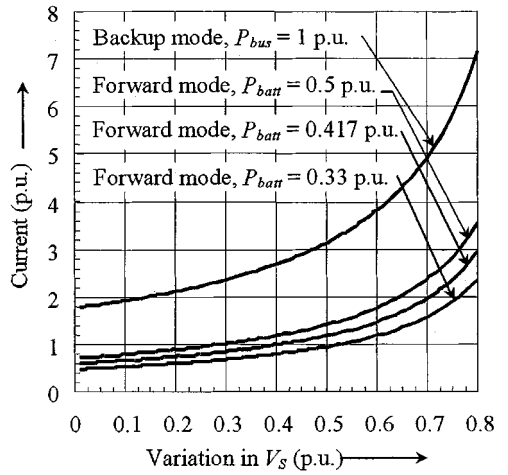



Fig. 11. RMS currents through $S_3$ and $S_4$.

The maximum and minimum duty ratios for $S_1$ and $S_2$ in the *forward mode* are defined by

$$d_{\max} = \frac{V'_{\text{batt}_{\max}}}{V_{S_{\min}}} \quad \text{and} \quad d_{\min} = \frac{V'_{\text{batt}_{\max}}}{V_{S_{\max}}}. \tag{1}$$

And the duty ratios for $S_3$ and $S_4$ in the *backup mode* are defined by

$$D_{\max} = \frac{V_S - V'_{\text{batt}_{\min}}}{V_S} \quad \text{and} \quad D_{\min} = \frac{1 - 2V_{S_{\min}}}{V_S}. \tag{2}$$

Fig. 6 shows the variation in the switch duty ratios as a function of the input dc bus voltage.

### A. Forward/Charging Mode

The minimum value of the output inductor, $L'_{o_{\min}}$, to maintain continuous inductor current under minimum load conditions is given by

$$L'_{o_{\min}} = \frac{V'_{\text{batt}_{\max}}}{4 \cdot f_s \cdot I'_{\text{batt}_{\min}}} \cdot (1 - 2d_{\min}) \quad \text{p.u} \tag{3}$$

where, $I'_{\text{batt}_{\min}}$ is the minimum p.u. battery charging current and $V'_{\text{batt}_{\max}}$ the maximum p.u. battery voltage. Fig. 7 shows the variation of $L'_{o_{\min}}$ as a function of the p.u. variation in the dc bus for the typical values of battery charging power. The actual value of $L'_o$ used in the circuit depends on the battery current ripple specifications and is larger than $L'_{o_{\min}}$. A suitable tradeoff must be made between the allowable output current ripple, $\Delta' i$, and the inductor size.

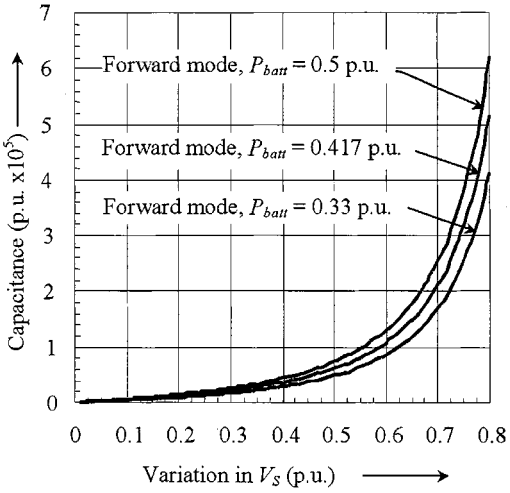



Fig. 12. Normalized value of input capacitor.

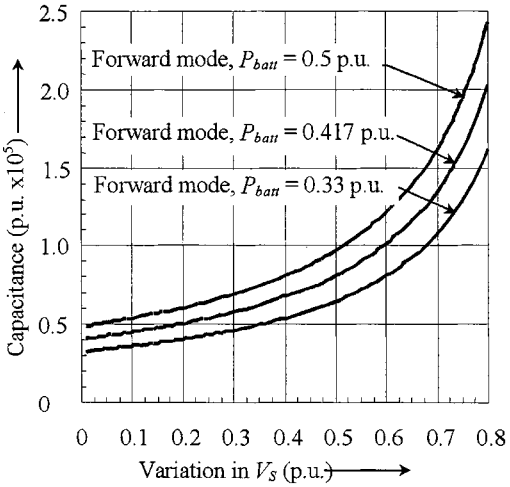



Fig. 13. Normalized value of output capacitor.

The selection of both the primary and secondary switches, depends primarily on the voltage stresses across and the current through them. The maximum reverse voltage across the primary side switches, $S_1$ and $S_2$, is equal to the maximum p.u. line voltage, is expressed as

$$V_{S_{1\max}} = V_{S_{2\max}} = V_{S_{\max}} \quad \text{p.u.} \tag{4}$$

The maximum rms current through the switches, $I_{S_{1\text{rms}}}$ and $I_{S_{2\text{rms}}}$, under maximum p.u. battery charging current, $I'_{\text{batt}_{\max}}$, and minimum p.u. line input voltage is shown in Fig. 9 and is given by,

$$\begin{aligned} I_{S_{1\text{rms}}} &= I_{S_{2\text{rms}}} \\ &= \frac{1}{2\sqrt{3}} \sqrt{\left(12 I'^2_{\text{batt}_{\max}} + \Delta i'^2\right) \cdot d_{\max}} \quad \text{p.u.} \end{aligned} \tag{5}$$

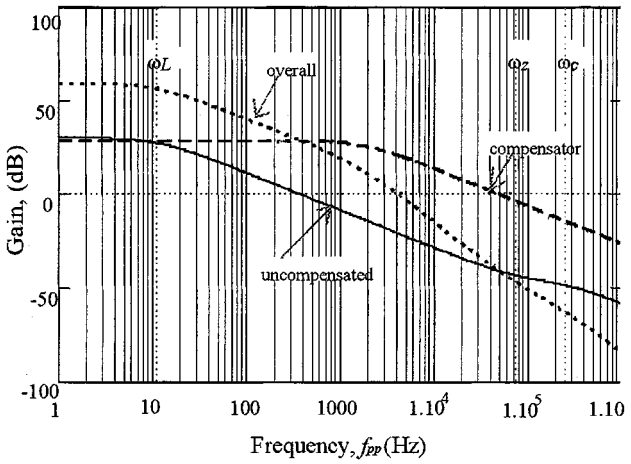



Fig. 14. Open loop gain response—forward/charging mode.

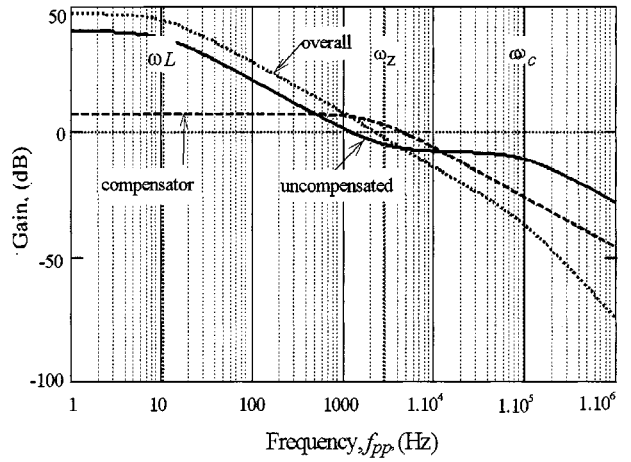



Fig. 15. Open loop gain response—backup/current-fed mode.

Maximum voltage stress across the body diodes of the secondary side switches, $S_3$ and $S_4$, is given by

$$V'_{S_{3\max}} = V'_{S_{4\max}} = V_{S_{\max}} \quad \text{p.u.} \tag{6}$$

The maximum average current through the body diodes of the secondary switches, $D_{S_3}$ and $D_{S_4}$, expressed by

$$I'_{D_{S_{3\text{avg}}}} = I'_{D_{S_{4\text{avg}}}} = \frac{I'_{\text{batt}_{\max}}}{2} \quad \text{p.u.} \tag{7}$$

is calculated for minimum input voltage and maximum load conditions and shown in Fig. 10.

During *forward mode* operation, if the battery is suddenly removed the energy stored in the inductor $L'_o$ is discharged into the output filter capacitor $C'_o$. This constraint and the maximum allowable value of output voltage ripple on $V'_{\text{batt}}$ based on the equivalent series resistance (*esr*) of the capacitor, define the choice of the filter capacitor $C'_o$. The first, and the dominant, constraint gives the minimum value of capacitor to be used as

$$C'_o = \frac{L'_o \cdot I'^2_{\text{batt}_{\max}}}{V'^2_{\text{batt}_{\text{peak}}} - V'^2_{\text{batt}}} \quad \text{p.u.} \tag{8}$$

where, $V'^2_{\text{batt}_{\text{peak}}}$ is the maximum allowable battery voltage when the load is removed. Fig. 13 shows the normalized values of the capacitance for different power at the battery end in the charging mode.

The input bulk capacitors, $C_1$ and $C_2$, are equal in value. The allowable input voltage ripple, $V'_{\text{ripple}}$, is a constraint for their selection, Fig. 12. The capacitors must also be large enough to provide sufficient hold up time at the dc bus voltage under dc mains failure, before the converter begins operation in the *backup mode*.

$$C_1 = C_2 = \frac{2 \cdot I_{\text{pri}}}{V'_{\text{ripple}}} \cdot t_{\text{diss}} \quad \text{p.u.} \tag{9}$$

where, $t_{\text{dis}}$ is the capacitor discharge period and $I_{\text{pri}}$ is the primary current at maximum duty ratio at an expected converter efficiency, $\eta$, of 80% given by

$$I_{\text{pri}} = \frac{P_{\text{batt}} \cdot d_{\max}}{V'_{\text{batt}}} \cdot \frac{100}{\eta}. \tag{10}$$

As mentioned in Section II, the balancing winding $N_{p_1}$ must have the same number of turns as the primary winding $N_p$ to ensure equal voltage across it to prevent staircase saturation of the core. As switch mismatches are very small, the average current in the winding is a few milliamps so a smaller diameter wire can be used for $N_{p_1}$. The diodes $D_1$ and $D_2$ carry only minimal current and can be suitably rated.

### *B. Backup/Current-Fed Mode*

The minimum value of $L'_o$, $L'_{o_{\min}}$, is computed to maintain continuous inductor current under minimum load by

$$L'_{o_{\min}} = \frac{1.25 \cdot V_S}{f_s \cdot I_{\text{bus}}} \cdot (2D_L - 1) \cdot D'^2_L \quad \text{p.u.} \tag{11}$$

where, the duty ratio $D_L$ is defined for the boundary of continuous inductor current at a minimum load of 0.1 p.u at the bus. Fig. 7 shows $L'_{o_{\min}}$ as a function of the specified p.u. variation in $V_s$. The minimum inductor current under boundary conditions, referred to the primary is expressed as

$$I'_{L_{\text{boundary}}} = \frac{V_S D'_L}{2 \cdot f_s \cdot L'_{o_{\min}}} \cdot (2D_L - 1) \quad \text{p.u.} \tag{12}$$

and, $D'_L = 1 - D_L$.

The actual value of the inductor is chosen to be as large as physically possible while using a specific core. Also, a larger inductor results in lower ripple component in the inductor current, which in turn implies a lower rms value of the current.

Current and voltage stresses across the switches $S_3$ and $S_4$ determine their ratings. The maximum voltage stress across the secondary side switches, $S_3$ and $S_4$, is

$$V'_{S_{3\,\max}} = V'_{S_{4\,\max}} = V_{S_{\max}} \quad \text{p.u..} \tag{13}$$

Fig. 11 shows the minimum rms current rating desired of these switches, which is given by

$$I'_{S_{3\text{rms}}} = I'_{S_{4\text{rms}}} = \frac{\sqrt{3}}{6}\sqrt{\left(\frac{3 \cdot I^2_{\text{bus}}}{D'^2_{\max}} + \Delta' i^2\right) \cdot (3 - 2D_{\max})} \quad \text{p.u.} \tag{14}$$

where, $\Delta' i$ is the ripple in the inductor current reflected to the primary and $D_{\max}$ is the maximum duty ratio and $D'_{\max} = 1 - D_{\max}$.

The maximum voltage and current stresses, for the rectifying body diodes, $D_{S_1}$ and $D_{S_2}$, of the primary switches are found to be

$$V_{S_{1\max}} = V_{S_{2\max}} = V_{S\max} \quad \text{p.u.} \tag{15}$$

$$I_{D_{S_{1\text{avg}}}} = I_{D_{S_{2\text{avg}}}} = \frac{I_{\text{bus}}}{2} \quad \text{p.u..} \tag{16}$$

The balancing winding, $N_{p_1}$, and the diodes $D_1$ and $D_2$ enable simultaneous and equal charging of the capacitors $C_1$ and $C_2$ during intervals $t_1$–$t_2$ and $t_3$–$t_4$. As $N_{p_1}$ and $N_p$ carry equal currents the wire diameter for both windings must be equal. The diodes $D_1$ and $D_2$ are selected according to the maximum reverse voltage across them and the current flowing through them while charging $C_1$ and $C_2$. Their ratings are identical to those for the body diodes of the switches $S_1$ and $S_2$, due to presence of identical windings $N_p$ and $N_{p_1}$.

The capacitors $C_1$ and $C_2$ are selected according to the desired output ripple at the dc bus. They must also be large enough to hold the voltage at the dc bus when the switches $S_3$ and $S_4$ overlap, during intervals $t_0$–$t_1$ and $t_2$–$t_3$, under the worst possible case of minimum battery supply voltage and full load.

## IV. Small Signal Analysis

Small signal analysis for both modes of converter operation under current mode control is performed to generate the required transfer functions to design and evaluate the control loop. The information from these transfer functions, particularly the control-to-output transfer function, has been used to determine the error amplifier that allows the converter to meet load regulation and transient response specifications.

For both operating modes, transfer functions are derived for the gain and audio susceptibility, using the procedure outlined in [11]. These transfer functions and the parameters used therein are defined in the Appendix. The frequency response of the control-to-output transfer function provides information on the poles and zeros and the gain of the uncompensated converter. The transfer function for the compensator (error amplifier) gain is derived using the information provided by output-to-control transfer function. This is used to design the compensation network parameters for the compensator which are needed to achieve desired overall system stability and response to transients and load variations.

## V. Design Example

This section presents a design example for the proposed bidirectional converter. The design curves in Figs. 6–15 provide suitable normalized ratings of components in the power circuit, under worst case conditions to ensure proper operation of the converter. These curves are plotted as a function of the p.u. variation in the dc bus $V_s$; a parameter that is defined. The analysis presented in Section IV is used to select the components for the feedback loop. The ratings of the components from the design curves provide a good approximation for the final values used in an actual implementation which maybe a little different due to other practical considerations. The final values of the power components used in the prototype, chosen after considering converter operation in both modes, are summarized in Table I.

TABLE I
Components Used in the Experimental Setup

| Parameters | Value/ Rating | Parameters | Value/ Rating |
|---|---|---|---|
| $D_1, D_2$ | MUR 460 | $L_p, L_{p_1}$ | 2 mH |
| $C_1, C_2$ | 150 μF | $L_s, L_o$ | 360 μH |
| $S_1, S_2$ | IRF 840 | $N_p$ | 19 |
| $S_3, S_4$ | IRFP 250 | $N_s$ | 8 |
| $C_o$ | 470 μF | $d_{max}$ | 0.435 |
| $D_{max}$ | 0.725 | $d_{min}$ | 0.326 |
| $D_{min}$ | 0.642 | | |

The specifications for converter operation are as follows.

***Forward/Charging Mode***

Input voltage range $= 300$ V ($V_{s_{\min}}$)–400 V ($V_{s_{\max}}$).
Output Power $= 100$ W ($P_{\text{batt}}$).
Operating frequency $= 100$ kHz ($f_s$).

***Backup/Current-fed Mode***

Output power (on dc mains bus) $= 300$ W ($P_{\text{bus}}$).
Output voltage (on dc mains bus) $= 350$ V ($V_s$).
Operating frequency $= 100$ kHz ($f_s$).

Using the base quantities defined in Section III, the change in the dc bus voltage is 0.143 p.u, giving the quantities $V_{S_{\max}}$ and $V_{S_{\min}}$, the operating frequency in both modes is 1 p.u., and the power at the battery end in the charging mode is 0.33 p.u. For simplicity in calculations the variation in the dc bus is taken as 0.14 p.u.

The nominal battery voltage during converter operation in the *backup mode* is 0.368 p.u., corresponding to the real value of 128.9 V and is defined, for a lead acid battery [12], by

$$V'_{\text{batt}} = \frac{V'_{\text{batt}_{\max}}}{1.167} \quad \text{p.u.} \tag{17}$$

where, $V'_{\text{batt}_{\max}}$ is the maximum p.u. battery volatge expressed as

$$V'_{\text{batt}_{\max}} = \frac{V_{S_{\min}}}{2 \cdot N} \quad \text{p.u..} \tag{18}$$

A suitable nominal value of the battery voltage is chosen at 48 V and the corresponding value of transformer turns ratio, $N = 2.687$, is calculated from (17) and (18). As the design curves are normalized with the assumption of a unity turns ratio transformer, this implies that the values obtained from the design curves must be converted to their real values and then transformed accordingly using the new transformer turns ratio of 2.687.

The corresponding maximum and minimum duty ratios for the switches $S_1$ to $S_4$ obtained from Fig. 6 are: $d_{\min} = 0.377, d_{\max} = 0.5, D_{\min} = 0.57$ and $D_{\max} = 0.678$.

*A) Inductor,* $\mathbf{L_o}$*:* The minimum value of the inductor, $L'_{o_{\min}}$, to maintain continuous inductor current is obtained from Fig. 7. For the *forward mode* with $P_{\text{batt}} = 0.33$ p.u., $L'_{o_{\min}} = 2.14$ p.u. at the minimum battery load of 0.033 p.u. In the *backup mode*, $L'_{o_{\min}} = 0.291$ p.u. with a minimum load at the dc bus of 0.1 p.u. The p.u. values in the forwardand *backup modes* correspond to

192.67 $\mu$H and 31.43 $\mu$H after the suitable conversion into real values. Therefore, the worst case value of 192.67 $\mu$H from the *forward mode* is selected for the inductance $L'_{o_{\min}}$.

*B) Switches,* $\mathbf{S_1}$ *and* $\mathbf{S_2}$*:* Equations (4) and (15) indicate that the maximum voltage stress across the switches is 1.14 p.u. in the *forward mode* and 1 p.u. across their body diodes in the *backup mode*. The rms current through the switches in the *forward mode* is 0.549 p.u. and the average current through their body diodes is 0.5 p.u., obtained from Figs. 9 and 10, respectively. The maximui voltage stress corresponds to 400 V in the forward and 350 V in the *backup mode*, and the worst case rms (*forward mode*) and average (*backup mode*) current ratings are 0.47 A and 0.429 A.

*C) Switches,* $\mathbf{S_3}$ *and* $\mathbf{S_4}$*:* The body diodes of $S_3$ and $S_4$ are subject to a maximum voltage stress of 1.14 p.u. in the *forward mode* and the switches are subject to a voltage stress of 1 p.u. in the *backup mode*. The average current through $D_{S_3}$ and $D_{S_4}$ is 0.388 p.u., Fig. 10, and the rms current through the switches in the *backup mode* is 1.99 p.u, Fig. 11. Therefore, a maximum of 400 V is seen across the switches in the *forward mode*. The average current through their body diodes is 0.853 A and the rms current through $S_3$ and $S_4$ in the *backup mode* is 4.58 A.

*D) Output Filter capacitor,* $\mathbf{C_o}$*:* The output filter capacitor is determined by the energy that it will have to absorb from the inductor if the battery is suddenly removed. The design curve in Fig. 13 for $P_{\text{batt}} = 0.33$ p.u. gives the value of $C_o$ as $6.2 \cdot 10^3$ p.u. This corresponds to a real value of 174 $\mu$F.

*E) Capacitors* $\mathbf{C_1}$ *and* $\mathbf{C_2}$*:* $C_1$ and $C_2$ provide filtering action for the input voltage ripple in the *forward mode* and hold-up time during the switchover to the *backup mode*. Fig. 12 gives the capacitance for each capacitor as $3.7 \cdot 10^4$ p.u. at $P_{\text{batt}} = 0.33$ p.u. which is 147 $\mu$F when converted to the real value using the appropriate conversion.

*F) Transformer secondary winding,* $\mathbf{N_S}$*:* The number of turns, and therefore the magnetizing inductance, of the secondary windings is made as large as possible. Taking into account the previously determined transformer turns ratio $N$, the number of secondary turns is selected according to the chosen suitably sized core, to minimize both copper and core losses in the transformer. The magnetizing inductance for the chosen core was determined to be 360 $\mu$H using 8 turns on the secondary winding.

*G) Transformer primary winding,* $\mathbf{N_p}$*:* Using the selected value of the transformer turns ratio, $N$, and the secondary winding inductance, $N_S$, the magnetizing inductance of the primary winding is calculated to be 1.4 mH.

*H) Balancing winding,* $\mathbf{N_{p_1}}$*:* The *forward mode* operation dictates that the number of turns on $N_{p_1}$ be equal to $N_p$, thereby resulting in equal inductance, to prevent the saturation of the core. In the *backup mode*, it was determined that the wire diameter for both the windings should be equal as they carry equal current. Thus, the winding $N_{p_1}$ is identical to $N_p$ and has 1.4 mH inductance.

*I) Catching diodes,* $\mathbf{D_1}$ *and* $\mathbf{D_2}$*:* $D_1$ and $D_2$ have voltage and current stresses equal to those of the body diodes of $S_1$ and $S_2$ in the *backup mode* as they permit simultaneous charging of $C_1$ and $C_2$. In the *forward mode* they carry minimal current only when balancing the mid-point of $C_1$ and $C_2$ and are subject to a maximum voltage stress of 1 p.u. Thus, the maximum voltage stress across them is 400 V and the average current is 0.429 A.

The values generated by the design curves provide a theoretical basis for the component ratings and values. In the actual implementation in the prototype the values are somewhat different. The maximum duty ratio of $S_1$ and $S_2$ is 0.435 and not the theoretically ideal value of 0.5, to provide a dead time between them in the *forward mode*. The transformer turns ratio is chosen as 2.373 and the design equations are used once again to generate the ratings for the laboratory prototype with the given operating specifications. These values are detailed in Table I.

The design of the compensator depends on the actual values of the power components used in the prototype.

### *Compensator Design:*

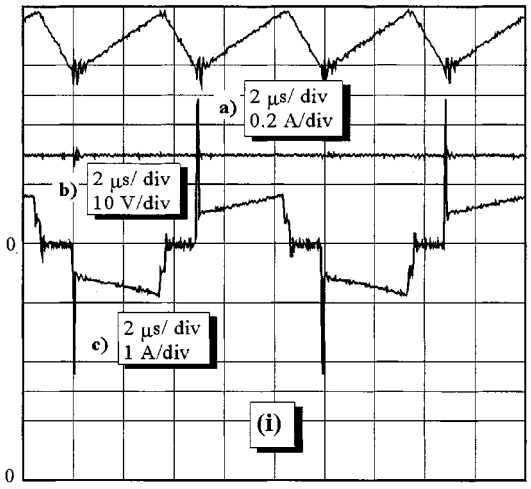
Once, the final selection of the power components is completed, the small signal analysis, presented in Section IV and the Appendix, determines the design of the control circuit parameters for both modes to achieve the desired bandwidth and meet stability requirements of the converter. Current mode control is implemented by UC 3846 and UCC 3804, for the forward and *backup mode*s, respectively.

For the *forward mode*, the output operating point, $R$, was chosen for $V_s = 350$ V, $P_{\text{batt}} = 100$ W and $V_{\text{batt}} = 54.65$ V. Output capacitor *esr*, $r = 5$ m$\Omega$, $R_s = 1$ and no slope compensation was used so, the slope of the compensating ramp, $M_c = 0$. The remaining parameters are calculated from the existing information of the power circuit components. Fig. 14 shows the gain transfer function of the uncompensated converter, the compensator, and the overall response of the system, for the calculated parameters. A high gain bandwidth of 59 dB and crossover frequency of about 4 kHz, is obtained by choosing $R_f = 270$ k$\Omega$, $R_{\text{in}} = 10$ k$\Omega$ and $C_f = 330$ pF.

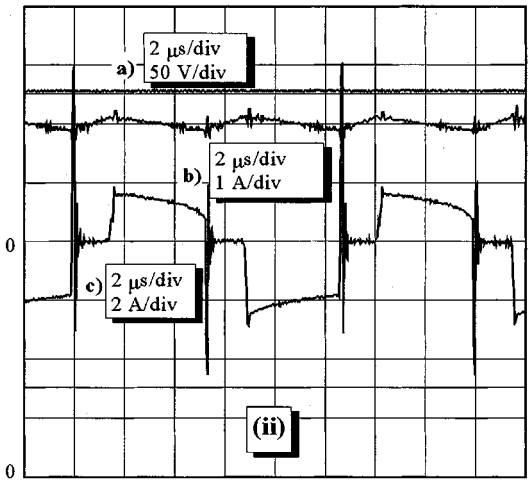
The parameters for the *backup mode* mode, defined in the Appendix, are calculated for the output operating point $R$ determined for $V_{\text{batt}} = 48$ V, $P_{\text{batt}} = 300$ W and $V_s = 350$ V. The combined effective *esr*, $r_e$, of the output capacitors, $C_1$ and $C_2$, is estimated to be 50 m$\Omega$, $R_s = 0.263$, and $M_c = 0$ as the ratio of compensating slope to the inductor current slope is zero. The other parameters are again determined by the component values selected the design of the power components. The frequency responses' of the uncompensated system, overall system and the compensator, which is designed to give the desired overall system response, are all shown in Fig. 15. The compensator, similar to that for the *forward mode*, has the following values to provide a gain bandwidth of 47.5 dB and a crossover frequency of 2.1 kHz: $R_f = 750$ k$\Omega$, $C_f = 100$ pF and $R_{\text{in}} = 330$ k$\Omega$.

## VI. Experimental Verification and Results

A prototype was built in the laboratory to evaluate the performance of the proposed topology. The static performance was studied and overall efficiency obtained experimentally, for both the *forward* and *backup modes*. The dynamic response of the converter under transient conditions of step changes in load and switchover from *charging* to *backup mode* is illustrated.




(a)




(b)

Fig. 16. Steady state operation (i). Forward mode. (a) Battery charging current, $i_{\rm batt}$. (b) Battery voltage, $V_{\rm batt}$. (c) Transformer primary current. (ii) Backup mode. (a) Load voltage, $V_S$. (b) Inductor Current, $i_{L_o}$. (c) Transformer primary current.

### A. Key Experimental Results in Steady State Operation

Fig. 16(a) shows the experimental waveforms for the *forward/charging mode*, at 75% load, with the converter operating at 100 kHz ($V_s = 360$ V, battery power $P_{\rm batt} = 85$ W). The dc mains supplies load power and charges the battery to $V_{\rm batt} = 54.5$ V, [Fig. 16(b)]. The battery charging current, $i_{\rm batt} = 1.55$ A, [Fig. 16(a)], is constant with relatively small ripple as desired.

Fig. 16(b) shows the relevant waveforms during steady state operation of the converter in the *backup/current-fed mode* at 75% rated load. The battery voltage, $V_{\rm batt} = 50$ V and load power, $P_{\rm bus} = 190$ W. The battery discharges to boost the voltage level of the dc bus to $V_s = 323$ V, Fig. 16(ii)a), thereby powering the load.

Current spikes are observed in the transformer primary current, in the *forward mode* and *backup modes*, Fig. 16. These are due to the reverse recovery of the diodes. Use of diodes with a softer reverse recovery, like Hexfreds, will reduce the current spikes. The higher voltage drop across them will not greatly effect the converter efficiency because of the low currents flowing through them in both operating modes when providing load rectification.

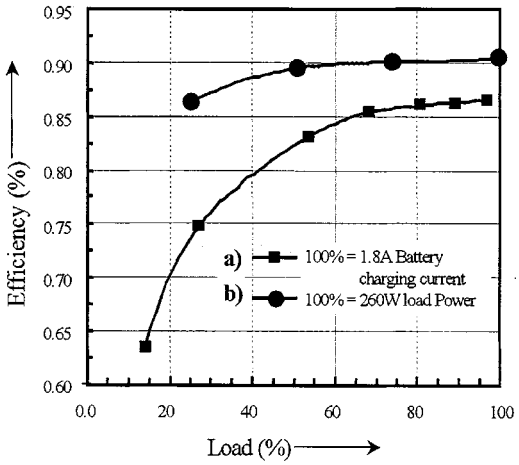



Fig. 17. Efficiency curves from experimental setup. (a) Forward mode. (b) Backup mode.

Certain applications may require the converter to start operating in the *backup mode* when the hold up capacitors $C_1$ and $C_2$ are not charged. Under such conditions, as the duty cycle of $S_3$ and $S_4$ is increased to build up the load (dc bus) voltage, current in the inductor continues to rise with the switches operating at maximum duty cycle. This continuous increase in the current results in a switch current that exceeds the rated value and can permanently damage the switch. This adverse situation can be avoided by adding a parallel combination of a relay and resistor, in series with the battery when starting up in the *backup mode*, with no output voltage. The series resistor limits the previously increasing inductor current. Once the output capacitors are charged the resistor is bypassed by the relay.

### B. Efficiency Evaluation

Fig. 17 shows the efficiency as a function of the percentage of battery charging (load) current for the forward mode ($V_s = 350$ V) obtained from the experimental setup. The battery charge voltage, $V_{\rm batt}$, is 54.1 V. The efficiency reaches a peak of 86.6% and is seen to decrease as the battery draws less charging current. The converter efficiency during the *backup mode* is also shown as a function of percentage load, with $V_{\rm batt} = 50$ V. The load voltage is maintained at 325 V. An efficiency of 90.5% is obtained for this mode. These results confirm a high efficiency for the converter topology in both operating modes.

### C. Transient Performance

Transient performance of the converter is evaluated under the following conditions: a) step change in load while operating in the *backup mode*, b) switchover from *forward* to *backup mode* at 75% load, when the battery is charged, and c) switchover from *forward* to *backup mode* when the battery is drawing a charging current of 1 A.

*1) Load Step Change:* The load transient condition is examined for a step change in load from 25% to 75% while operating in the *backup mode*. Fig. 18(b) shows the change in load current from 0.2 A to 0.59 A with the inductor current, $i_{L_o}$, Fig. 18(c), reaching a steady state value of 4.05 A at 75% load. There is an

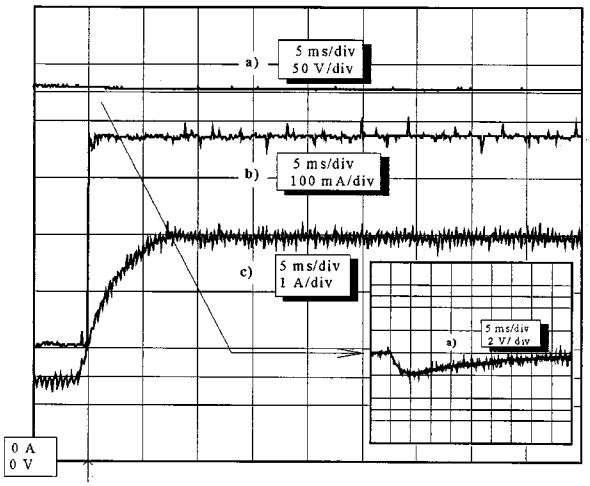



Fig. 18. Load transient (25 to 75%)—Backup mode. (a) Load voltage, $V_S$. (b) Load current, $i_{\rm bus}$. (c) Inductor current, $i_{L_o}$.

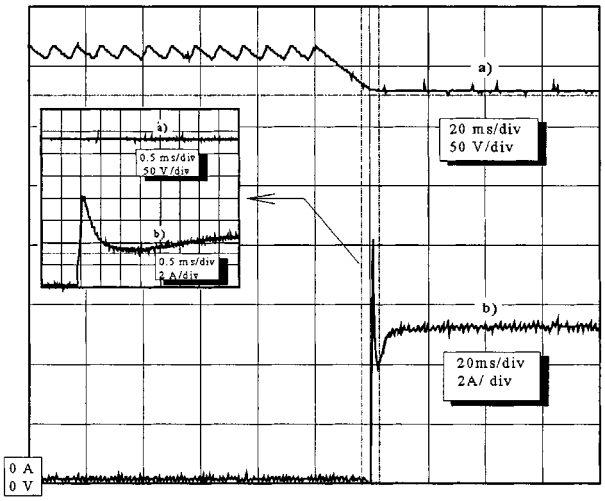



Fig. 19. Switchover—forward to backup mode (75% load) with battery charged. (a) Load voltage, $V_S$. (b) Inductor current, $i_{L_o}$.

imperceptible change in the dc bus voltage [Fig. 18(a)] for this step change in load, as seen in the zoom during that particular time interval. This indicates the excellent response of the converter to load transients.

*2) Switchover from Forward to Backup Mode When the Battery Is Charged:* Fig. 19 shows the switchover at 75% load, with the battery charged at 53 V and therefore drawing minimal current. The bus voltage [Fig. 19(a)] is 360 V in the *forward mode* and is regulated at 325 V in the *backup mode*, which is within the load converter's working input voltage range of 300–400 V. On ac mains failure, the voltage at the dc bus starts to drop. As soon as the bus voltage is detected below 325 V, the converter begins operation in *backup mode* and regulates the bus voltage at 325 V. Other values of the regulated bus voltage in the *backup mode* are possible by appropriate changes in the line and bulk detection circuitry. The zoom in Fig. 19 shows that inductor current, $i_{L_o}$, changes direction and reaches a steady state value in a very short duration. The converter thus provides seamless transition from *forward* to *backup mode*.

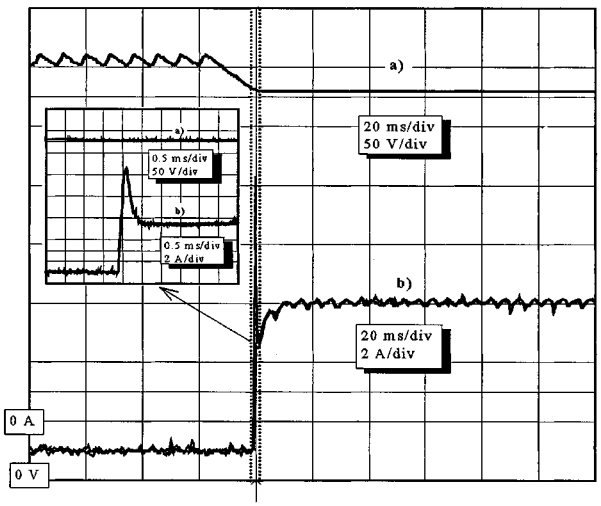



Fig. 20. Switchover—forward to backup mode with battery drawing charging current of 1 A (75% load). (a) Load voltage, $V_S$. (b) Inductor current, $i_{L_o}$.

*3) Switchover from Forward to Backup Mode When the Battery Draws Charging Current:* Fig. 20 shows the switchover to *backup mode* at 75% load, with the battery drawing 1 A charging current at 50 V. The inductor current [Fig. 20(b)] demonstrates a quick change in direction from a negative to a positive value. The load voltage [Fig. 20(a)] regulates at 324 V.

When the ac line comes back, the bus voltage rises and on crossing the 325 V threshold, begins to supply the load. The converter now operates in *forward mode*. The *backup mode* error amplifier reduces the inductor current resulting in a smooth transition from one mode to the other. A delay is allowed before the battery starts charging again to ensure the presence of the stable ac line and prevent sudden switchovers from one mode to the other.

## VII. Conclusion

A bidirectional converter topology has been presented and evaluated. Steady state analysis provides the normalized expressions and the design curves to select the power components. Small signal models are presented to determine the compensation network parameters. A design example has been included, using the design procedure outlined for the power components and the compensation network. The experimental setup for the proposed converter, based on the design example, validates the analysis and shows good steady state and transient (load transient and switchover from one mode to another) performance. The converter demonstrates high efficiency (86.6% in the *forward mode* and 90.5% in the *backup mode*), low part count due to its bidirectional feature and galvanic isolation.

## Appendix
## Parameters Used in Small Signal Transfer Functions

### A. Forward/Charging Mode

*Open Loop Audio Susceptibility*

$$\frac{\hat{v}_{\rm batt}}{\hat{v}_s} = A_{g_{vf}} \cdot \frac{1+\frac{s}{\omega_z}}{1+\frac{s}{\omega_L/C_1}+\frac{s^2}{\omega_L\omega_c/C_1}}$$

$$\omega_z = \frac{\omega_L R}{r}$$
$$\omega_L = \frac{1}{(R+r)\cdot C_o}$$
$$\omega_c = r\cdot\frac{nd'_{fw}-d_{fw}}{L_o d'_{fw} n} + \frac{2\omega_s}{\pi n d'_{fw}}.$$

*Control-to-Output*

$$\frac{\hat{v}_{\text{batt}}}{\hat{v}_c} = G_{vf}\cdot\frac{1+\frac{s}{\omega_z}}{1+\frac{s}{\omega_L/C_1}+\frac{s^2}{\omega_L\omega_c/C_1}}$$
$$C_1 = \frac{(nd'_{fw}-d_{fw})\cdot r + kR}{(nd'_{fw}-d_{fw}+k)R}$$
$$G_{vf} = \frac{kR}{nd'_{fw}-d_{fw}+k}\cdot\frac{1}{R_s}$$
$$A_{g_{vf}} = \frac{(nd'_{fw}-d_{fw})d_{fw}}{2N(nd'_{fw}-d_{fw}+k)}.$$

*Error amplifier Gain*

$$A_{\text{comp}_{vf}} = \frac{R_f}{R_{\text{in}}\cdot(1+sR_fC_f)}$$
$$n = 1+\frac{2M_c}{M_1}$$
$$\omega_s = \frac{2\pi}{T_s}$$
$$k = \frac{4L_o}{RT_s}$$

where

| | |
|---|---|
| $r$ | *esr* of the output filter capacitor $C_o$; |
| $R_f$ and $R_{\text{in}}$ | feedback and input resistors; |
| $L_o$ | output filter inductor; |
| $R$ | output operating point; |
| $R_s$ | ratio of voltage to comparator to switch current; |
| $d_{fw}$ | ON time duty ratio of switch $S_1$ (or $S_2$) in half a switching cycle; |
| $d'_{fw} =$ , | $1-d_{fw}$; |
| $C_f$ | feedback path capacitor; |
| $T_s$ | switching period; |
| $M_c$: | slope of stabilizing ramp; |
| $M_1$ | inductor current slope during switch ON time; |
| $N$ | transformer primary to secondary turns ratio. |

### B. For the Backup/Current-Fed Mode

*Open loop audio susceptibility*

$$\frac{\hat{v}_s}{\hat{v}_{\text{batt}}} = A_{g_{cf}}\cdot\frac{1+\frac{s}{\omega_{z_1}}}{1+\frac{s}{\omega_L/C_b}+\frac{s^2}{\omega_L\omega_c/C_b}}.$$

*Control-to-output*

$$\frac{\hat{v}_s}{\hat{v}_c} = G_{cf}\cdot\frac{1-\frac{s}{\omega_{z_2}}}{1+\frac{s}{\omega_L/C_a}+\frac{s^2}{\omega_L\omega_c/C_a}}$$
$$\omega_L = \frac{1}{(R+r_e)C_e}.$$

*Error Amplifier Gain*

$$A_{\text{comp}_{vf}} = \frac{R_f}{R_{\text{in}}\cdot(1+sR_fC_f)}$$
$$\omega_{z_1} = \frac{4L_o + r_eRC_eN'D'_{\text{ov}}}{N'D'_{\text{ov}}(2r_e - N'RD'_{\text{ov}})}$$
$$\omega_c = \frac{r_eN'^2D'_{\text{ov}}}{kRT_s} + \frac{2}{nD'_{\text{ov}}T_s}$$
$$C_b = \frac{4kR + r_enN'^2D'^2_{\text{ov}}}{2R(8k+nN'^2D'^3_{\text{ov}})}$$
$$A_{g_{cf}} = 2\cdot\frac{8kR + D'_{\text{ov}}N'^2\left\{2r_eD^2_{\text{ov}} + RD'_{\text{ov}}(nD'_{\text{ov}} - D_{\text{ov}})\right\}}{N'D'_{\text{ov}}R(16k+nN'^2D'^3_{\text{ov}})}$$
$$G_{cf} = \frac{4k(N'RD'_{\text{ov}} - 2r_e)}{R_s(16k+nN'^2D'^3_{\text{ov}})}$$
$$C_a = \frac{8Rk + r_enN'^2D'^2_{\text{ov}}}{R(16k+nN'^2D'^3_{\text{ov}})}$$
$$\omega_{z_2} = \frac{\left\{kD_{\text{ov}}T_s + 0.5r_eC_eD'^2_{\text{ov}}N'^2(nD_{\text{ov}} - D_{\text{ov}})\right\}R}{4kR + D'_{\text{ov}}N'^2\left\{RD'_{\text{ov}}(nD'_{\text{ov}} - D_{\text{ov}}) + 2r_eD^2_{\text{ov}}\right\}}$$
$$\omega_s = \frac{2\pi}{T_s}$$
$$k = \frac{4L_o}{RT_s}$$
$$n = 1+\frac{2M_c}{M_1}$$
$$N' = \frac{1}{N}$$

where

| | |
|---|---|
| $R_f$ and $R_{\text{in}}$ | feedback and input resistors; |
| $R$ | output operating point; |
| $R_s$ | ratio of voltage to comparator to switch current; |
| $D_{\text{ov}}$ | overlap interval in each half switching period; |
| $N'$ | transformer secondary to primary turns ratio; |
| $r_e$ | *esr* of equivalent capacitance $C_e$ (combination of $C_1$ and $C_2$); |
| $C_f$ | feedback path capacitor; |
| $T_s$ | switching frequency; |
| $D'_{\text{ov}} =$ , | $1-D_{\text{ov}}$; |
| $M_c$ | slope of compensating ramp; |
| $M_1$ | slope during overlap period. |

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