A Bidirectional Multi-Port DC-DC Converter with Reduced Filter Requirements

by

Yuanzheng Han

A thesis submitted in conformity with the requirements
for the degree of Master of Applied Science
Graduate Department of Electrical and Computer Engineering
University of Toronto

Abstract

A Bidirectional Multi-Port DC-DC Converter with Reduced Filter Requirements

Yuanzheng Han
Master of Applied Science
Graduate Department of Electrical and Computer Engineering
University of Toronto
2016

Practical challenges in distributed generation and electric vehicles have motivated the rapid development of bidirectional multi-port dc-dc converters. This paper proposes a converter that not only can perform fast battery voltage balancing and limit ground leakage current, it also features low switching ripple and component count, providing significant cost savings from reduced filter requirements and improved efficiency. Experimental testing of a 3.3 kW prototype confirms the bidirectional power transfer capability and demonstrates above 99% converter efficiency over a wide range of input power.

Contents

List of Tables

List of Figures

Chapter 1

Introduction

1.1 Research Challenge in DC-DC Converter

Commercialization of both distributed generation (DG) and electric vehicles (EV) has presented a unique set of practical challenges and motivated research into suitable power processing converters [10, 13, 21]. Typical applications in DG and EV require a dc-dc converter to integrate multiple lower voltage dc energy sources, such as photovoltaic (PV) panels or battery stacks, with a high voltage dc bus [3, 16, 20]. Particularly, the key functional and safety requirements for such a multi-port dc-dc topology include independent optimal loading of inputs, low ground leakage currents, and, in the case of energy storage applications, bidirectional power transfer capability [13, 18, 21].

The dc energy sources in DG or EV applications typically operate at a low dc voltage level, ranging from 3 to 4 V for a Li-ion battery cell to approximately 16-17 V for a "12-V" PV panel of 36 cells at maximum power point (MPP) [20]. Battery cells or low votlage PV panels are then packaged in modules with higher voltages and used in applications. For example, standard battery packs can be found with 12 V, 48 V, 96 V or 192 V [19]. However, voltages at this level still cannot meet the voltage requirements of existing higher power systems [20, 21]. For instance, the most common PV systems are designed for operation under 1000 V with dc bus limits ranging from 575 V to 850 V [15]. Consequently, energy sources such as battery packs or PV panels are usually connected in series to achieve the required dc voltage level. As the number of series connected sources increases, optimal loading of individual energy sources, both at the cell level and module level, is compromised. In the case of solar PV applications, sub-optimal loading results in reduced power harvesting, which is costly but not hazardous. In the case of energy storage applications where Li-ion batteries form the energy source, battery cells that are equally charged or discharged by the same current will still deviate

in their state of charge (SOC) over time because of the difference in electrochemical characteristics among battery cells [21]. Consequently, without charge equalization, the capacity for the entire battery string is limited by the battery cell that has the least capacity, and such limitation can eventually reduce the battery pack capacity by 25-30% [12]. Of even greater concern, a lack of charge equalization can lead to overcharging and over-discharging that not only greatly reduce battery cycle life, but, particularly for overcharging, may also cause battery heating, venting, or explosions [2].

While cost and efficiency constraints generally make energy balancing at the individual solar cell or battery cell level infeasible, module level energy balancing can substantially reduce the severity of the problem, increasing yield from solar PV arrays and improving SOC balance within battery systems. While Li-ion battery systems still require per-cell overcharge and over-discharge protection, such protection circuitry is greatly simplified if the battery pack voltage is reduced via string sub-division.

Power converters are usually used to connect battery packs or PV panels in series to form high voltage strings and bypass faulty units. Multi-port dc-dc converters are an cost-effective and efficient options to help mitigate energy imbalance amongst stacked dc energy sources. An important consideration in the selection of a suitable multi-port dc-dc converter is the ground leakage current. Challenges associated with ground leakage currents are well-documented in non-isolated dc-dc converters for PV applications. These currents are an unintentional capacitive current caused by high frequency fluctuating voltages across parasitic capacitances [4, 5, 9, 11]. The nature of non-isolated cascaded multi-port topologies dictates that some of the input dc energy sources will be necessarily ungrounded. Consequently, fluctuations of the potential between their input reference potential and ground may occur at either grid frequency or switching frequency [11]. This fluctuating potential will energize any parasitic capacitance, resulting in ground leakage current.

In the context of cascaded PV panels, the parasitic capacitance refers to the effective capacitance between the conducting surface of the PV array and the ground or grounded frame [5]. Experimental studies in [9] estimate that high frequency parasitic ground capacitance is approximately 7.08 nF/kW$_p$, while other studies in [5] and [11] report a range of parasitic capacitance from pF/kW up to μF/kW depending on topology, switching strategies, and environmental conditions. Because the ground leakage current flows in a resonant circuit that also includes the converter filter components, it can become very significant under certain operating conditions [9].

Ground leakage currents are highly undesirable as they both lower converter efficiency and post safety hazards to people and animals [7, 11, 17]. Consequently, it is important

for converters to limit and minimize the ground leakage current.

1.2 Existing Technology

Many multi-port dc-dc converters have been proposed over the years as possible solutions to the challenges in DG or EV applications. However, most of these converters address only some of the above mentioned research challenges and are often not satisfactory due to economics or performance concerns.

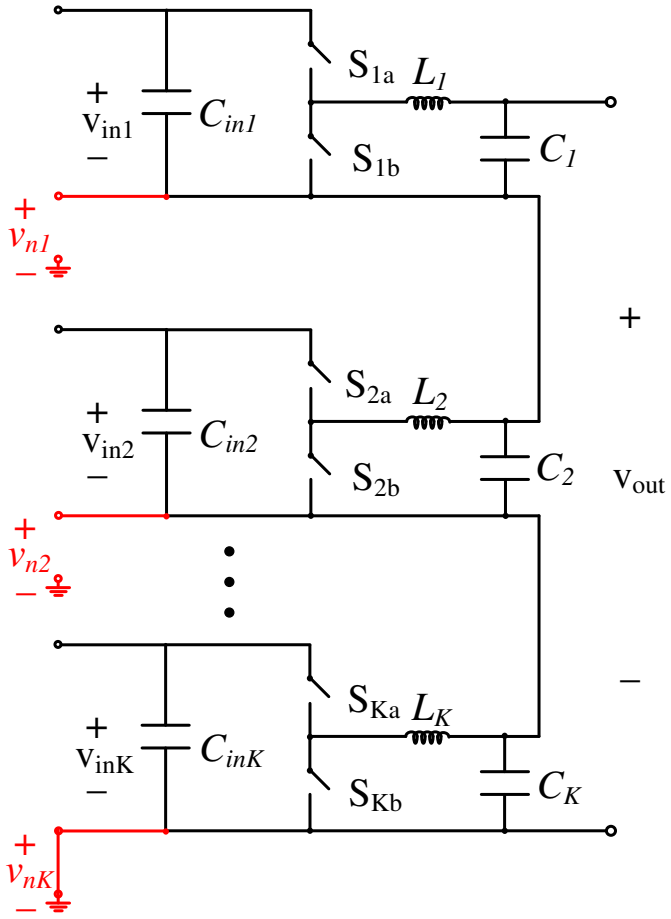


Figure 1.1: Classical cascaded buck converter.

Because a multi-port dc-dc converter application typically has indistinguishable input ports with identical input sources, one of the most straightforward approaches in deriving new multi-port topologies is to select a single-input single-output topology of desirable characteristics and connect multiple instances of it in series to form a multi-port converter.

Fig. 1.1 shows an example of this kind of multi-port dc-dc converter with a buck topology. This classical cascaded buck converter can satisfy most of the functional requirements of applications in DG and EV with independent optimal loading of inputs, low ground leakage currents, and bidirectional power transfer capability, and therefore will be used as a base case to compare and evaluate other multi-port dc-dc converters. The classical cascaded buck converter, however, does not utilize the possible component sharing among its modules and thus does not take any advantage of cost reduction and provides opportunity for further improvement.

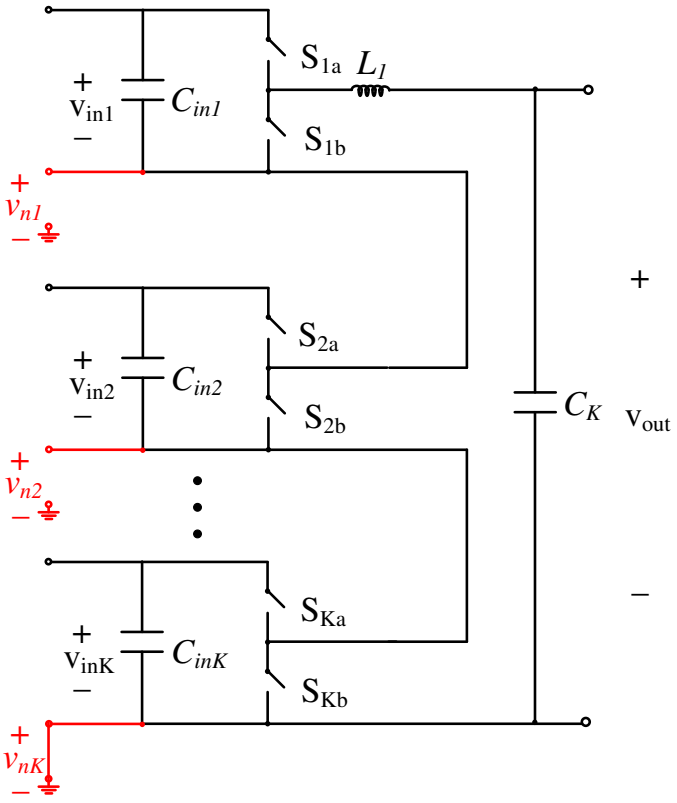


Figure 1.2: Two-part hybrid cascaded multi-level converter.

A two-part hybrid cascaded multi-level converter is proposed in [21] for the energy storage system in EV and DG. The dc-dc stage includes cascaded half-bridges with battery cells interfaced with a dc bus as shown in Fig. 1.2. The topology resembles the classical cascaded buck topology in Fig. 1.1 but has proposed to combine all individual inductive and capacitive filter components to a single output inductor and capacitor in an attempt to reduce the converter construction cost and enhance power density. However, such modification removes the direct capacitive path to ground from all ungrounded input

reference potentials, and as a result, baring a single grounded potential all other v_{nk}'s experience high frequency fluctuating voltage, which can lead to uncontrollable level of ground leakage currents.

A modular system that performs both battery cell-level balancing and dc-dc conversion to supply a low-voltage bus is proposed in [6]. The cascaded system shown in Fig. 1.3 is based on a series-input parallel-output architecture of low voltage, low power dc-dc converters. Battery cells are connected directly in series in this system, thus eliminating the problem of ground leakage current due to high frequency fluctuating potential. The inclusion of a low voltage dc bus allows the low power dc-dc converters to control power sharing between the cells and the bus to achieve battery balancing. However, this system does not perform load regulation of the high voltage dc bus, and therefore, is not intended to be utilized as a power processing converter for EV or DG applications.

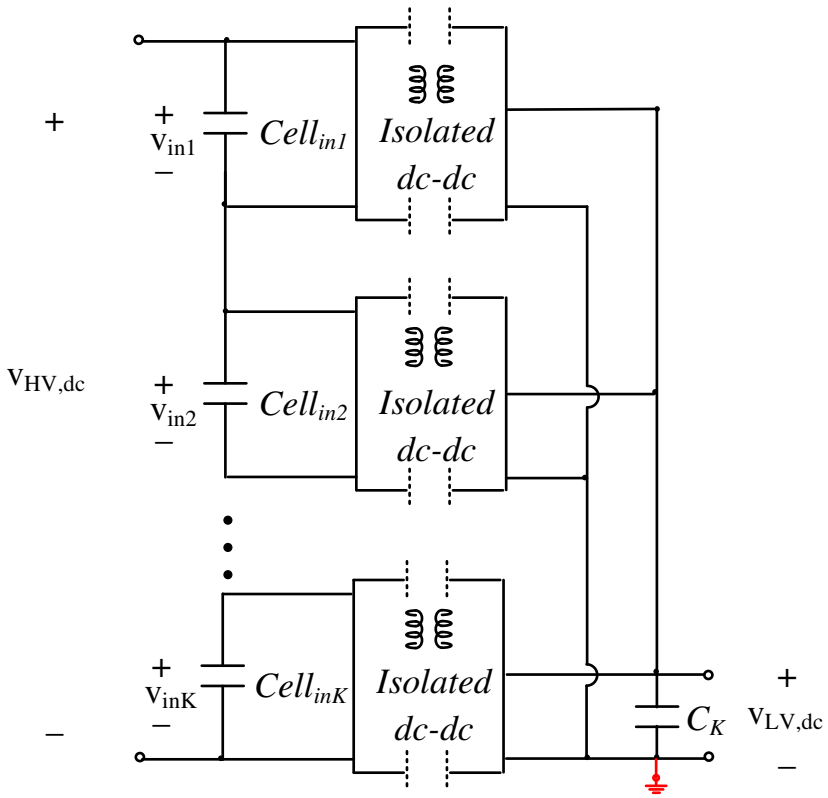


Figure 1.3: Active Balancing System for Electric Vehicles with Incorporated Low Voltage Bus.

It is evident from the above discussion that the existing multi-port dc-dc topologies are inadequate in addressing some of the most important open challenges in EV and DG applications. More specifically, there lacks an efficient and economical multi-port power

processing converter that is capable of interfacing energy storage with high voltage dc bus as well as performing key functional requirements such as battery cell balancing. The issue of ground leakage current in non-isolated multi-port topologies further complicates the converter design, making the research of suitable power processing converters in EV and DG a worthy challenge.

The objective of this thesis is to propose and experimentally verify a new bidirectional multi-port dc-dc converter with limited ground leakage current and low switching ripple that can be used as a power processing converter and perform fast battery voltage balancing in an energy storage system.

1.3 Thesis Outline

The thesis outline is as follows:

In Chapter 2, a modular converter topology along with its variants are proposed as solutions to a list of design objectives. The cascaded configuration is discussed in Chapter 6 as a separate topic.

In Chapter 3, after obtaining the converter steady state input-output relationship, an interleaved switching strategy is proposed to enhance the switching ripple reduction characteristics of the proposed converter.

In Chapter 4, the dynamic model of the converter is derived, and a control algorithm is proposed to achieve key functional objectives as well as to address some practical control challenges.

In Chapter 5, a case study of the proposed converter compared with the classical cascaded buck converter is conducted and supported with both simulation and experimental results.

In Chapter 6, several cascaded configurations are proposed, and one of which is selected for control design. The control algorithm is further verified with simulation results.

Chapter 2

Proposed Converter Topology

2.1 Design Objectives

It is recognized that there are many open challenges in multi-port dc-dc converter research that require attention while many requirements cannot be satisfied simultaneously. This research will focus on bringing a solution to some of the practical challenges in DG and EV applications discussed in the introductory chapter. It is decided in the early stages of the research that the proposed converter topology should be:

- Modular and can be extended to a multi-input single-output converter;
- Capable of managing power sharing independently among input ports;
- Capable of bidirectional power transfer from input ports to the output port;
- Capable of limiting high frequency ground leakage current; and
- Highly efficient with reduced filter requirement, compared to the cascaded buck converter of Fig. 1.1.

The above five design objectives are especially important for a battery management system. More specifically, a modular structure allows flexibility in designing total input battery voltage level while independent power sharing management can satisfy functional requirements such as battery voltage balancing or fault bypassing. Bidirectional power transfer is essential to charge and discharge the batteries. Limiting ground leakage current not only reduces safety hazards such as electric shock but also reduces power loss. Finally, a highly efficient converter with reduced filter requirement helps reduce the cost and size of the converter and improves the life and ecomony of a battery system.

2.2 Proposed Topology

To conceive a highly efficient modular converter with reduced filter requirement, it is important to utilize the idea of filter component sharing among the input and output ports. A double-input single-output general structure is one of the simplest structures that allows for filter sharing design and is therefore chosen as the base structure to design the multi-port modular converter.

The proposed non-isolated multi-port dc-dc converter is shown in Fig. 2.1. The converter has two input ports v_1 and v_2, and one output port v_3. Two pairs of complementary switches are employed: 1) S_{1a}, S_{1b} and 2) S_{2a}, S_{2b}, connected via a single interface inductor. Switches S_{1b} and S_{2a} are active switches. Switches S_{1a} and S_{2b} may be implemented using diodes if only unidirectional power conversion is required, or using active switches to enable bidirectional power conversion. An interleaved pair of capacitors, C_{3a} and C_{3b}, as shown in Fig. 2.1, simultaneously provide output filtering and filtering of the reference voltage v_{n1} to ground. Hence, the sizing of capacitors C_{3a} and C_{3b} provides a direct mechanism for mitigating high frequency ground currents that might otherwise flow through parasitic capacitances that exist between the floating dc energy sources and ground.

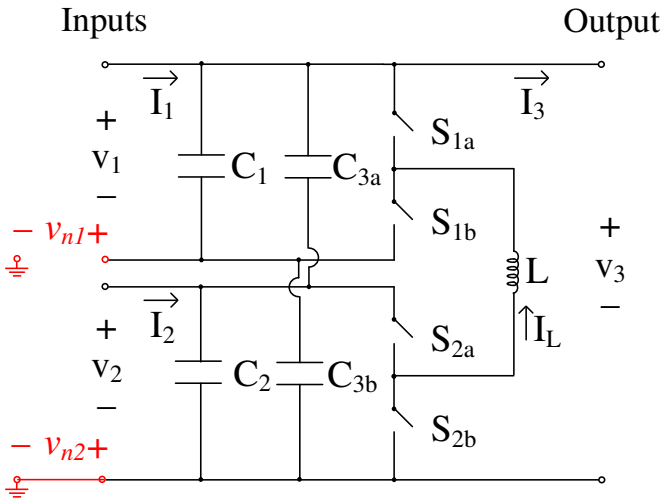


Figure 2.1: Proposed bidirectional multi-port dc-dc converter.

One of the key features of the proposed topology is the interfacing inductor L flanked by the two pairs of complementary switches. It is shared among all switching states and provides energy transfer and current filtering simultaneously. On the other hand, the placement of capacitors C_{3a} and C_{3b} provides enhanced filtering of both output voltage

v_3 and the reference voltage v_{n1} to ground for a given capacitor size and voltage rating. Due to the interleaved placement of capacitors, the equivalent output capacitor C_{out} can be calculated from (2.1). (2.2) and (2.3) show the dc voltage rating for C_{3a} and C_{3b} in the proposed converter.

$$C_{out} = (C_{3a}//C_2) + (C_{3b}//C_1) \tag{2.1}$$

$$V_{C3a} = V_3 - V_2 \tag{2.2}$$

$$V_{C3b} = V_3 - V_1 \tag{2.3}$$

The proposed converter has reduced energy storage requirements when compared to the majority of other double-input single-output topologies in [8]. It should be noted that the proposed converter module can be expanded to a $(2K+1)$-port converter by cascading with itself. The cascaded configuration will be discussed in Chapter 6.

2.3 Variants and Comparison

The placement of the capacitors C_{3a} and C_{3b} can be changed to derive topological variants of the proposed converter module. For example, C_{3a} and C_{3b} can be moved to the output port V_3 to form a single output capacitor C_3 as shown in Fig. 2.2.

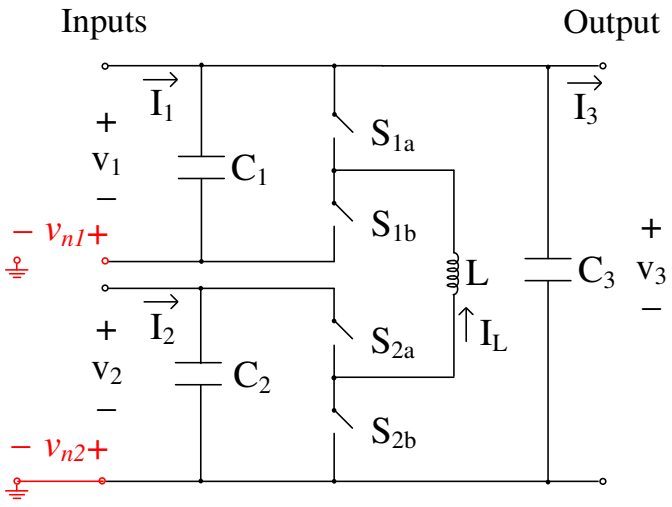


Figure 2.2: Variant 1 of the proposed converter with a single output capacitor.

Similarly, another variant of the proposed converter can be found by combining the capacitors C_{3a} and C_{3b} to a single capacitor C_3 and placed between the input ports as

shown in Fig. 2.3. In this case, the equivalent output capacitor C_{out} can be calculated from (2.4). The dc voltage rating for C_3 is shown in (2.5).

$$C_{out} = C_3//C_2//C_1 \tag{2.4}$$

$$V_{C3} = V_3 - V_1 - V_2 \tag{2.5}$$

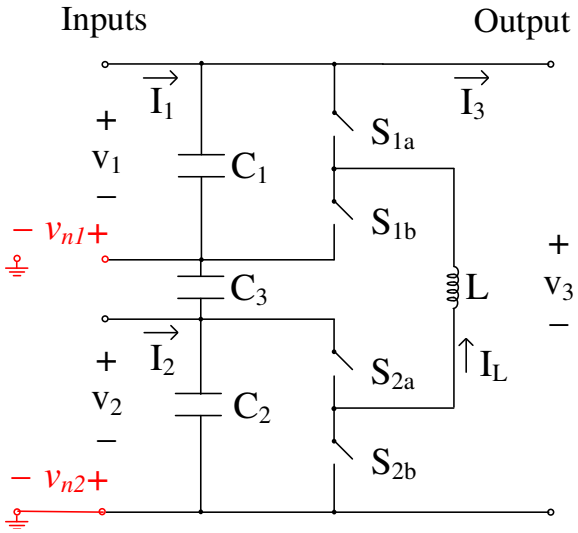


Figure 2.3: Variant 2 of the proposed converter with a centrally placed single output capacitor.

In the proposed converter and its variants, input ports V_1 and V_2 are typically connected to batteries. Consequently, C_1 and C_2 are dominated by the battery capacitance, which is significantly larger than the filter capacitor. As a result, equivalent output capacitors for the proposed converter and the variant 2 shown before can be approximated as (2.6) and (2.7), respectively.

$$C_{out,proposed} = C_{3a} + C_{3b} \tag{2.6}$$

$$C_{out,variant\ 2} = C_3 \tag{2.7}$$

If we can assume both inputs have voltage V, it is evident that the output port voltage V_3 has the range shown in (2.8).

$$V_3 = [0, 2V] \tag{2.8}$$

Table 2.1 compares the capacitor placements between the proposed converter and its

variants. It can be seen the proposed capacitor configuration has the lowest capacitor voltage rating when compared to its variants. On the other hand, the proposed configuration provides a direct capacitive path from the reference node v_{n1} to ground and is not limited by the input capacitance. This results in better filtering performance and design flexibility.

	Variant 1	Variant 2	Proposed
Capacitor rating	2V	2V	V
Equivalent *Cout*	C_3	C_3	C_{3a}+C_{3b}
Direct filter v_{n1} to gnd			✓

Table 2.1: Comparison of various capacitor configurations.

Chapter 3

Principle of Operation

3.1 Input Output Relationship

The proposed switch mode converter consists of one inductor and four capacitors and is controlled by two pairs of complementary switches, which can also be designed to have arbitray phase shift in their respective carriers. Consequently, the order and duration of the switching states for the proposed converter depend on the switching strategy, making finding the dc input-output relationship a challenge using the conventional inductor voltage second balancing (IVSB) method and the capacitor charge balancing (CCB) equations. However, a closer examination of the variant 1 of the proposed converter in a different perspective reveals that the structure resembles two buck switching cells with their outputs connected together as shown in Fig. 3.1.

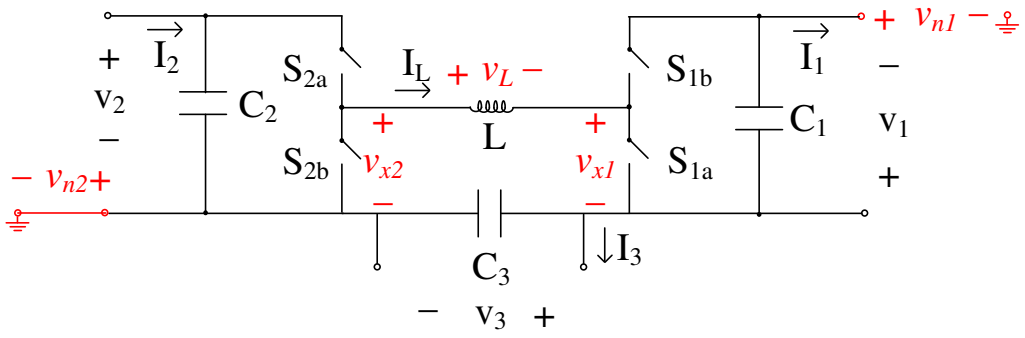


Figure 3.1: Variant 1 of the proposed converter with a single output capacitor shown in a different perspective.

Consequently, the output port voltage V_3 can be found with (3.1).

$$V_3 = \frac{1}{T_s}\int_{T_s} v_{x2} - v_{x1} - v_L \tag{3.1}$$

where

$$\frac{1}{T_s}\int_{T_s} v_{x2} = D_2 V_2 \tag{3.2}$$

$$\frac{1}{T_s}\int_{T_s} -v_{x1} = D_1 V_1 \tag{3.3}$$

$$\frac{1}{T_s}\int_{T_s} -v_L = 0 \tag{3.4}$$

Duty cycle D_1 controls the percentage on-time of switch S_{1b}, and D_2 controls switch S_{2a}. Similarly, the current relationship can be found using (3.5) and (3.6), where the average capacitor currents are all zero.

$$I_3 = \frac{1}{T_s}\int_{T_s} i_L \tag{3.5}$$

$$\frac{1}{T_s}\int_{T_s} i_L = \frac{I_1}{D_1} = \frac{I_2}{D_2} \tag{3.6}$$

Together with the simplified voltage equation, the converter dc input output relationship is shown in (3.7) and (3.8).

$$V_3 = D_1 V_1 + D_2 V_2 \tag{3.7}$$

$$I_3 = \frac{I_1}{D_1} = \frac{I_2}{D_2} \tag{3.8}$$

It has been shown in Chapter 2 that equivalent output capacitors can be found for the proposed converter and its variant 2. Consequently, the same dc input-output relationship can be found using the above analysis.

To simplify the discussion, variant 1 of the proposed converter with a single output capacitor is used for the following analysis of interleaved control. IVSB analysis of the proposed converter will be shown at the end of this chapter.

3.2 Interleaved Control

Fig. 3.2 to 3.5 illustrate all four possible switching states due to the switching sequence of the two pairs of complementary switches.

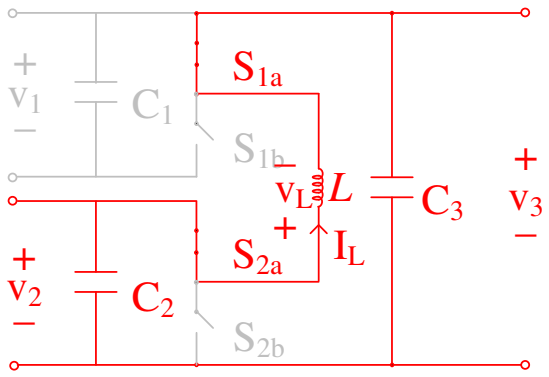


Figure 3.2: Switching state 1 of variant 1 of the proposed converter.

The order and appearance of the switching states are affected by the relative phase shift of the carrier signals for the two pairs of complementary switches. Consequently, it is possible to manipulate the order of switching states with an appropriate interleaved control to reduce inductor switching ripple.

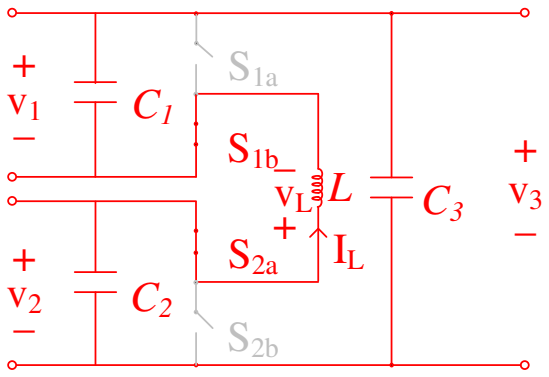


Figure 3.3: Switching state 2 of variant 1 of the proposed converter.

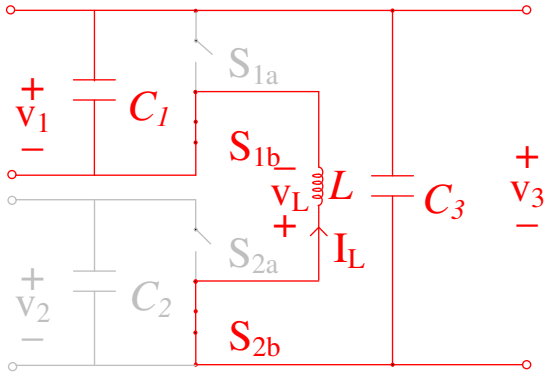


Figure 3.4: Switching state 3 of variant 1 of the proposed converter.

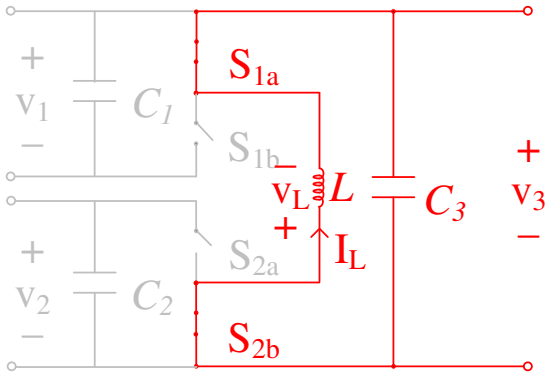


Figure 3.5: Switching state 4 variant 1 of the proposed converter.

$$State\ 1: \ v_L = v_2 - v_3 \tag{3.9}$$

$$State\ 2: \ v_L = v_1 + v_2 - v_3 \tag{3.10}$$

$$State\ 3: \ v_L = v_1 - v_3 \tag{3.11}$$

$$State\ 4: \ v_L = -v_3 \tag{3.12}$$

In order to find the appropriate interleaved switching strategy, it is important to review the intended converter operation. The converter is intended to be used in a battery management system to regulate dc power transfer from battery sources to high

voltage dc bus as described in the Design Objectives in 2.1. Because battery voltage balancing is an important requirement of such a system, it is reasonable to assume that the desired voltage and power transfer for both the input ports will be identical during steady state operations. Consequently, (3.13) and (3.14) can be assumed in designing the switching strategy.

$$V_1 = V_2 = V_{in} \tag{3.13}$$

$$D_1 = D_2 = D \tag{3.14}$$

Therefore, the inductor current rate of change will be the same for both switching states 1 and 3 in the steady state operation according to (3.9) and (3.11). In consequence, in order to reduce the inductor current ripple, the switching strategy should allow states 1 and state 3 to have the same duration and be separated by other switching states to ensure that the peak inductor current ripple at the beginning of states 1 and 3 is the same. Effectively, this causes the inductor current ripple to appear at doubling of the physical switching frequency as shown in Fig. 3.6.

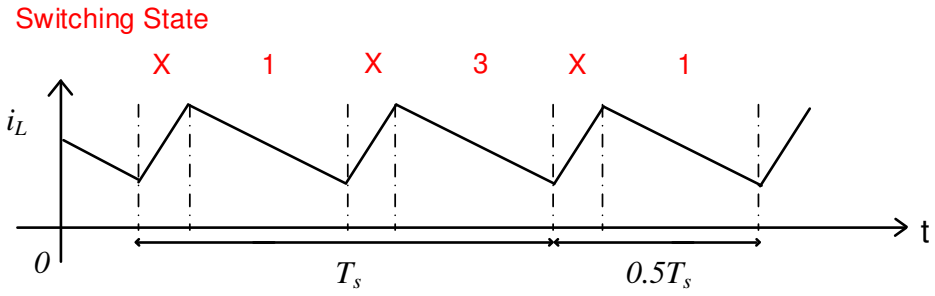


Figure 3.6: The inductor current waveform for the interleaved control of the two pairs of complementary switches.

Because each switching state corresponds to a specific set of switch ON/OFF status, the desired duty cycle waveforms for D_1 and D_2 can be deducted from Fig. 3.6. The desired duty cycle waveforms along with the PWM implementation are shown in Fig. 3.7.

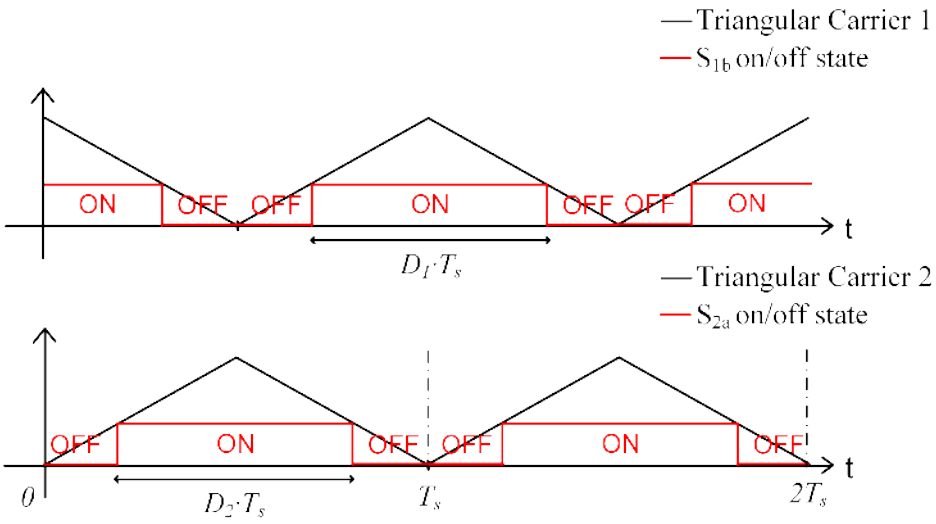


Figure 3.7: Interleaved control of the two pairs of complementary switches.

Two triangular carrier signals with 180° phase shift are used to control and synchronize switches S_{1b} and S_{2a}. The symmetrical carrier ensures that the switching states 1 and 3 have the same duration in the steady state operation. On the other hand, state 2 appears in the switching sequence when D is greater than 0.5 while state 4 appears when the duty cycle is less than 0.5. (3.15) confirms with the IVSB analysis that the voltage conversion ratio for the interleaved switching strategy agrees with the input output relationship found in (3.7).

$$< V_L >_{T_s} = \frac{1}{T_s}\left(\int_{T_2}(v_1+v_2-v_3)+\int_{T_1}(v_2-v_3)+\int_{T_2}(v_1+v_2-v_3)+\int_{T_3}(v_1-v_3)\right) \tag{3.15}$$

$$\begin{aligned} &= \left(\frac{D}{2}-\frac{1-D}{2}\right)(V_1+V_2-V_3)+(1-D)(V_1-V_3) \\ &\quad +\left(\frac{D}{2}-\frac{1-D}{2}\right)(V_1+V_2-V_3)+(1-D)(V_2-V_3) \\ &= DV_1+DV_2-V_3 \end{aligned}$$

3.3 IVSB Analysis of the Proposed Configuration

With the interleaved control and D is greater than 0.5, the proposed converter configuration has the following three switching states:

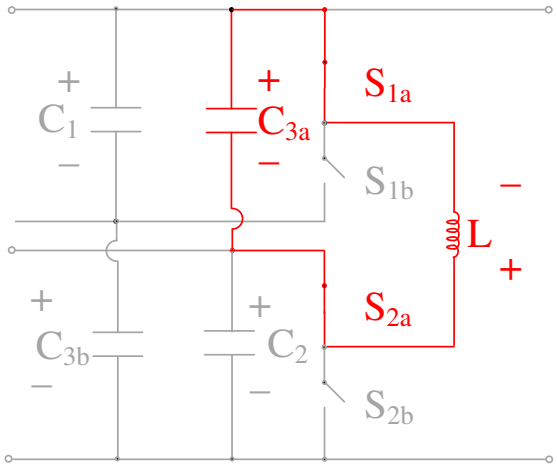


Figure 3.8: Switching state 1 of the proposed converter.

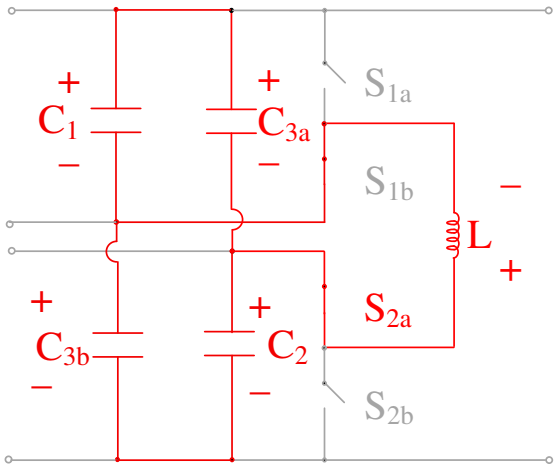


Figure 3.9: Switching state 2 of the proposed converter.

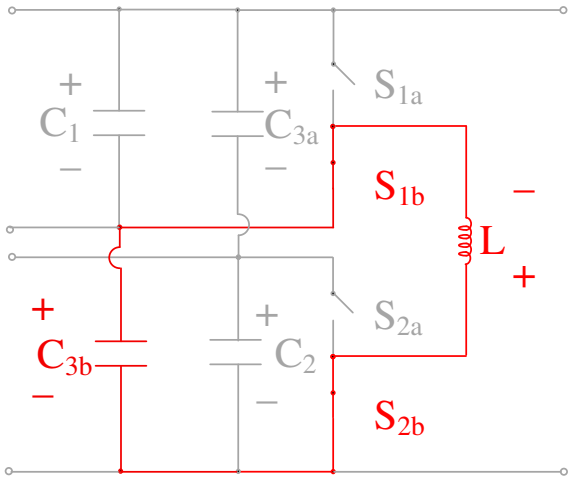


Figure 3.10: Switching state 3 of the proposed converter.

$$State\ 1: \ v_L = -v_{3a} \tag{3.16}$$

$$State\ 2: \ v_L = v_1 - v_{3a} = v_2 - v_{3b} \tag{3.17}$$

$$State\ 3: \ v_L = -v_{3b} \tag{3.18}$$

IVSB analysis (3.19) of the proposed converter with interleaved capacitor configuration also confirms the dc relationship.

$$\begin{aligned} < V_L >_{T_s} &= \frac{1}{T_s}\left(\int_{T_2}(v_1 - v_{3a}) + \int_{T_1}(-v_{3a}) + \int_{T_2}(v_2 - v_{3b}) + \int_{T_3}(-v_{3b})\right) \\ &= \left(\frac{D}{2} - \frac{1-D}{2}\right)(V_1 - V_{3a}) + (1-D)(-V_{3a}) \\ &\quad + \left(\frac{D}{2} - \frac{1-D}{2}\right)(V_2 - V_{3b}) + (1-D)(-V_{3b}) \\ &= DV_1 + DV_2 - \frac{1}{2}(V_1 + V_2 + V_{3a} + V_{3b}) \\ &= DV_1 + DV_2 - V_{out} \end{aligned} \tag{3.19}$$

Chapter 4

Control Strategy

4.1 Theoretical Control Design

To better understand the dynamic behaviour and control for the proposed converter, the lossless dynamic model is first derived using the state-space averaging technique shown in (4.1) to (4.3) for the variant 1 with a single output capacitor.

$$L\frac{di_L}{dt} = (d_1 v_1 + d_2 v_2) - v_{out} \tag{4.1}$$

$$C_1\frac{dv_1}{dt} = -d_1 i_L \tag{4.2}$$

$$C_2\frac{dv_2}{dt} = -d_2 i_L \tag{4.3}$$

The output dynamics are treated as a disturbance v_{out} to the control system because the output port voltage is typically regulated by connected sources or separate converters. Considering the converter intended application in battery management systems, there are two main control objectives for the typical operation of this converter:

- Regulating output current; and
- Balancing input port voltages.

It is not immediately obvious how to achieve these two goals simultaneously using the control variables d_1 and d_2 because controlling the two input port voltages independently while regulating the output current seems to require three control variables. However, because the output voltage is regulated by an external system, the action of controlling output current or the inductor current is related to the sum of the input voltages as shown in (4.1). On the other hand, the second objective of balancing the input port

voltages means that it is desired to regulate the voltage difference between the input ports. In other words, to achieve the control objectives it is required to control the sum and difference of the input voltages. Consequently, it could be more intuitive for the control design to use the sum and difference variables of the original control variables as shown in (4.4) to (4.7).

$$v_\Sigma = v_1 + v_2 \tag{4.4}$$

$$v_\Delta = v_1 - v_2 \tag{4.5}$$

$$d_\Sigma = \frac{d_1 + d_2}{2} \tag{4.6}$$

$$d_\Delta = \frac{d_1 - d_2}{2} \tag{4.7}$$

To simplify the dynamic model, it is assumed that the input filter capacitance C_1 and C_2 are the same and equal to C. This is a reasonable assumption as batteries of the same type are often connected to the input ports and consequently, the filters are also chosen to be the same. The transformed dynamic model using the sum and difference variables is shown in (4.8) to (4.10).

$$L\frac{di_L}{dt} = d_\Sigma v_\Sigma + d_\Delta v_\Delta - v_{out} \tag{4.8}$$

$$C\frac{dv_\Delta}{dt} = -2i_L d_\Delta \tag{4.9}$$

$$C\frac{dv_\Sigma}{dt} = -2i_L d_\Sigma \tag{4.10}$$

Because v_Σ is related to the output port voltage through the duty cyle command d_Σ, there are only two states of interest for this control system, namingly the inductor current i_L and the input voltage difference v_Δ. Fig. 4.1 shows the controller block diagrams of (4.8) and (4.9) with the inclusion of parasidic resistance R_{esr}. The current controller regulates the inductor current to i_L^{ref}, and the delta controller regulates the input voltage difference to zero. Because the voltage diference between input ports is small during steady state operation, $d_\Delta v_\Delta$ is small and treated as a disturbance to the system together with v_{out}. Physically speaking, while the current controller outputs the desired voltage level to achieve the load current reference, the delta controller divides the current to charge or discharge the input ports at different rates to achieve voltage balancing.

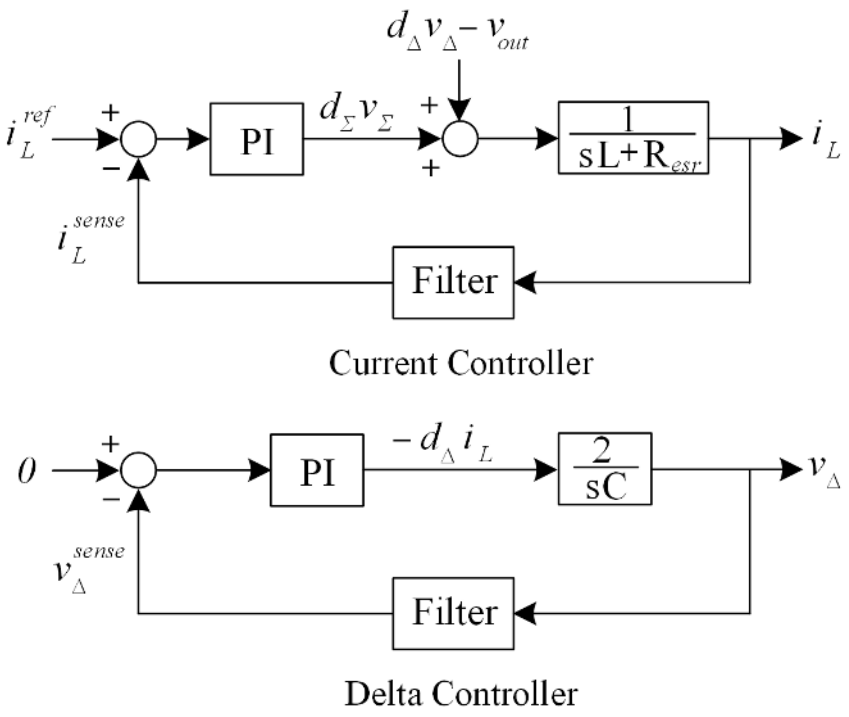


Figure 4.1: Block diagrams of the current and delta controllers

Theoretical design for both the current controller and delta controller can be achieved with a conventional PI controller for the first order system. The controller output can be reconstructed to the usable form of d_1 and d_2 with (4.11) and (4.12).

$$d_1 = \frac{d_\Sigma v_\Sigma}{v_1^{sense} + v_2^{sense}} + \frac{-d_\Delta i_L}{-i_L^{ref}} \tag{4.11}$$

$$d_2 = \frac{d_\Sigma v_\Sigma}{v_1^{sense} + v_2^{sense}} - \frac{-d_\Delta i_L}{-i_L^{ref}} \tag{4.12}$$

i_L^{ref} is used in calculating d_Δ to reduce the effect of current sensing noise in computing the duty cycle. However, such approximation is valid for a relatively fast controller, and appropriate logic should be implemented such that when i_L^{ref} changes signs the delta controller is not driving d_Δ to the wrong direction due to the response time of the inductor current.

The same control scheme can also be derived for the proposed converter configuration. The state space equations are shown in (4.13) to (4.15).

$$L\frac{di_L}{dt} = (d_1 v_1 + d_2 v_2) - \frac{1}{2}(v_1 + v_2 + v_{3a} + v_{3b}) \tag{4.13}$$

$$C_1 \frac{dv_1}{dt} = -d_1 i_L + C_{3b} \frac{dv_{3b}}{dt} \tag{4.14}$$

$$C_2 \frac{dv_2}{dt} = -d_2 i_L + C_{3a} \frac{dv_{3a}}{dt} \tag{4.15}$$

Applying the same sum and difference variable transformation in (4.4) to (4.7), the transformed dynamic model for the proposed configuration is shown in (4.16) and (4.17), where the same controls structure can be used.

$$L \frac{di_L}{dt} = d_\Sigma v_\Sigma + d_\Delta v_\Delta - v_{out} \tag{4.16}$$

$$(C + C_f) \frac{dv_\Delta}{dt} = -2 i_L d_\Delta \tag{4.17}$$

4.2 Practical Control Challenge

4.2.1 Predict-Reset Control

One practical challenge in designing the delta controller is that the input port capacitance is greatly influenced by the connected source, and consequently, the stability and dynamic response in practice can be very different from the control design. Fig. 4.2 compares loop gain and phase margin variations due to different input port capacitances. It can be seen that for a specific PI controller the delta control loop remains stable but the phase margin becomes very small for large input capacitance. The magnitude plot shows that the input capacitance alters the loop gain and causes the dynamic performance to vary. In other words, if a user connects high capacitance energy sources to the input ports, this specific delta controller might cause highly oscillatory input voltage variations during the process of voltage balancing.

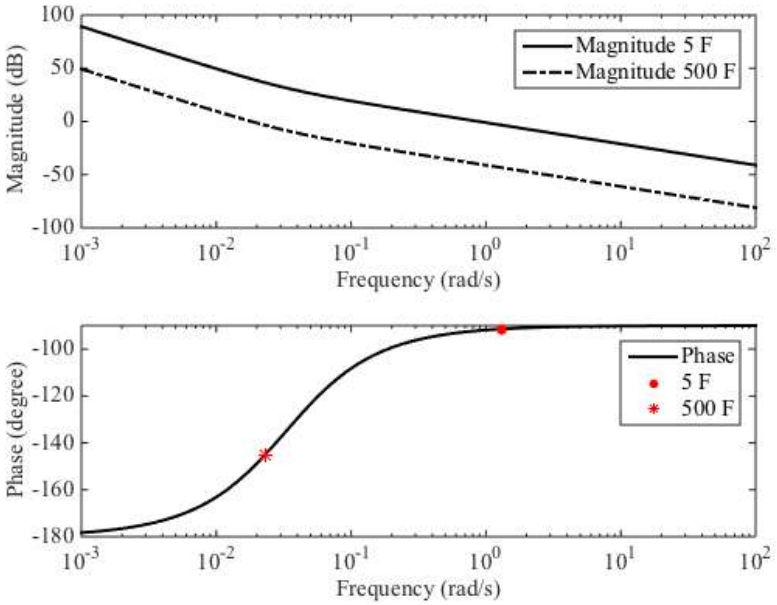


Figure 4.2: Low frequency bode plots comparing gain and phase margin variations due to different battery capacitance of the input ports.

To prevent such undesired dynamic behaviour, a predict-reset PI controller, shown in Fig. 4.3, is designed and implemented in the delta control loop. An examination of the control objectives reveals that the reference to the delta controller needs to be constant and zero for proper voltage balancing. Consequently, the controller error-output product threshold, M, can be used as a reliable indicator to reset the accumulated control errors, as shown in Fig 4.3. In practical implementations, it is possible that the system settles to a steady state with d_Δ not equal to zero due to different leakage current of the batteries. Therefore, M is set to a small negative number to relax integrator reset criteria.

The reset threshold M is a small but negative quantity with sufficient amplitude to ensure that accumulator reset does not occur under steadystate conditions due to leakage currents. Fig. 4.4 compares the dynamic response of both the conventional and predict-reset PI controllers for different input capacitance. It can be seen that the predict-reset PI controller prevents voltage overshoot and achieves balancing approximately 10 times faster than the conventional PI controller.

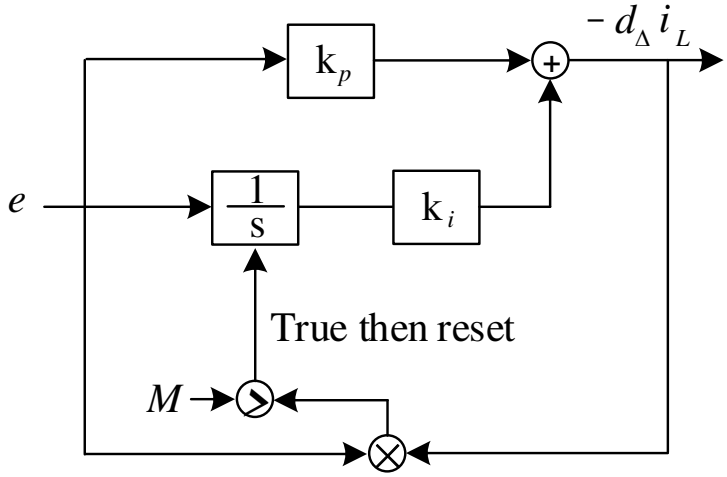


Figure 4.3: The predict-reset PI control logic used in the practical implementation of the delta controller.

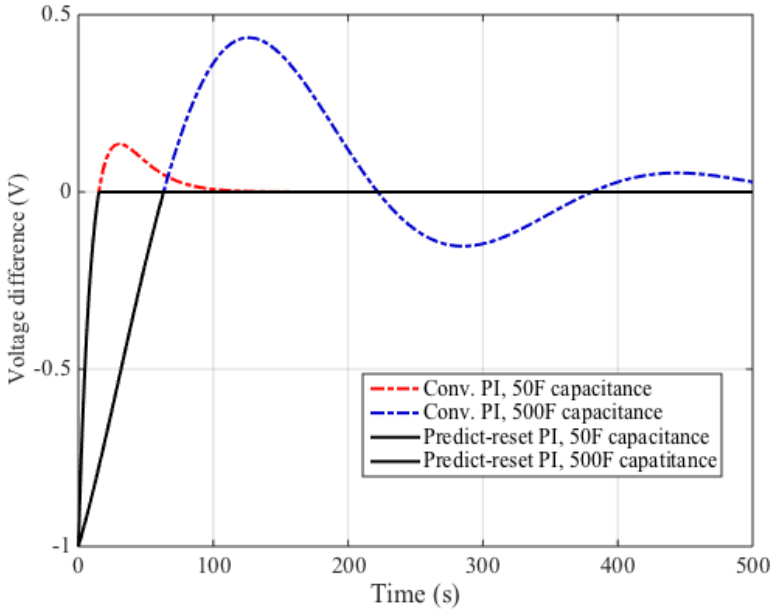


Figure 4.4: Comparison of the dynamic response of both the conventional and predict-reset delta controllers for different input port capacitance.

4.2.2 Integrator Anti-Windup

Another practical concern in the controller implementation is the integrator saturation. Many factors, including battery capacity, load current, bidirectional power transfer and difference voltage level, can affect the integrator saturation. Consequently, an effective integrator anti-windup method is required. In the proposed control strategy, a variation of the integrator clamping method is implemented for the current controller as shown in Fig. 4.5. Integrator clamping or conditonal integration is a method to avoid integrator windup where the integration is suspended when a certain condition is met [14]. In this case, the condition used is shown in (4.18) where it is found to provide the best result [14].

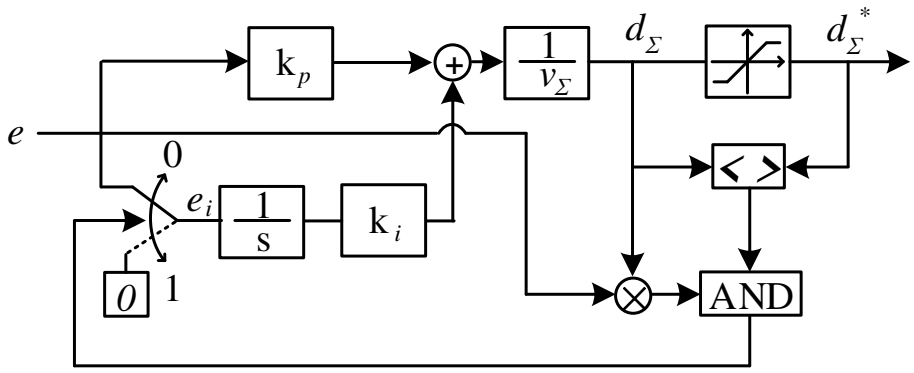


Figure 4.5: Anti-windup method used for the current control loop.

$$e_i = \begin{cases} 0, & if\ e \cdot d_\Sigma > 0\ and\ d_\Sigma \neq d_\Sigma^* \\ e, & else \end{cases} \tag{4.18}$$

Fig. 4.6 shows that the integrator clamping method returns the output to the linear region immediately after saturation and thus can be used as an effective anti-windup scheme.

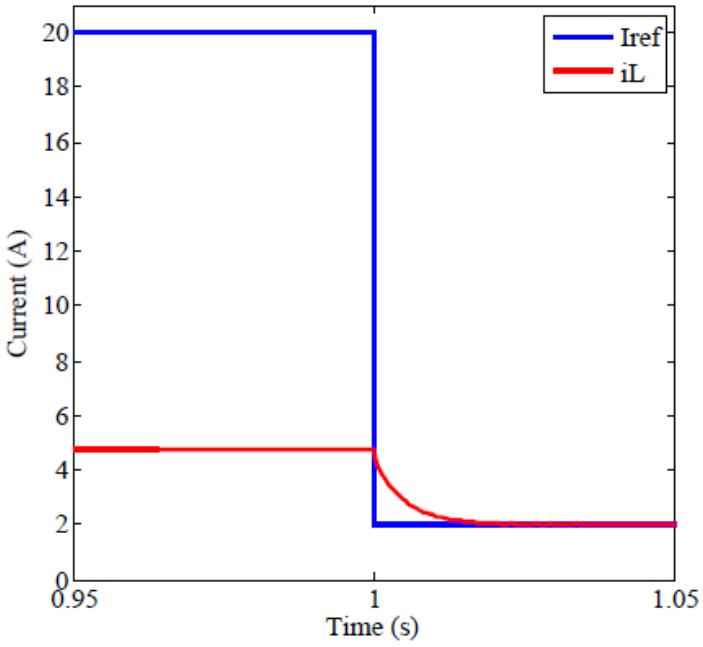


Figure 4.6: Response of the current controller with anti-windup.

Similarly, the integrator clamping method can also be used in the delta controller. However, a slight modification of the saturation logic is required to consider the sign of the inductor current as shown in (4.19).

$$e_i = \begin{cases} 0, & if\ e \cdot (d_\Delta - d_\Delta^*) \cdot i_{ref} < 0 \\ e, & else \end{cases} \tag{4.19}$$

Chapter 5

Case Studies

5.1 Simulation Analysis

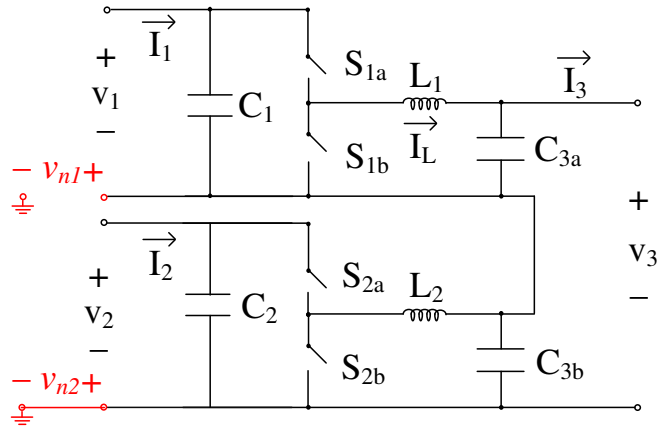
To compare and quantify the reduction in switching ripple of the proposed converter, a simulation study and comparison with a typical double-input single-output classical cascaded buck converter (Fig. 5.1 (a)) is conducted in PLECS. Equivalent energy storage requirements (of inductors and capacitors) are implemented in both converters as shown in Table 5.1.

Symbol	Definition	Value
f_s	Switching frequency	60 kHz
C_{3a}, C_{3b}	Filter capacitor	68 μF
L_1, L_2	Inductors	13.1 μH
L	Equivalent single inductor	26.2 μH

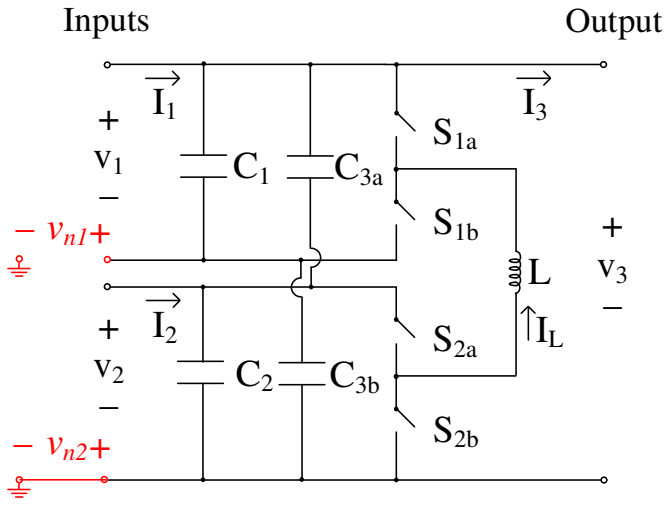
Table 5.1: Components used in the simulation and experiment.

5.1.1 Switching Performance

Both converters are operated with interleaving to minimize switching ripple. Fig. 5.2 shows simulated waveforms of i_L, v_{out}, and $\Delta v_{n1,pp}$ for both converters at input voltages of 50 V and output voltage of 70 V. The proposed converter has lower switching ripple for equivalent energy storage. Summaries in Table 5.2 show that when compared to the classical cascaded buck converter, the proposed converter inductor current ripple is reduced by 3.6 times while the output voltage and input reference node voltage ripple are



(a)



(b)

Figure 5.1: (a) The double-input single-output classical cascaded buck converter used in the simulation as a comparison to show the ripple reduction characteristics of the proposed converter. (b) The proposed converter configuration.

reduced by 3.7 and 12.8 times, respectively. The reduction in switching ripple leads to significant cost savings in the form of reduced filter requirements and improved efficiency.

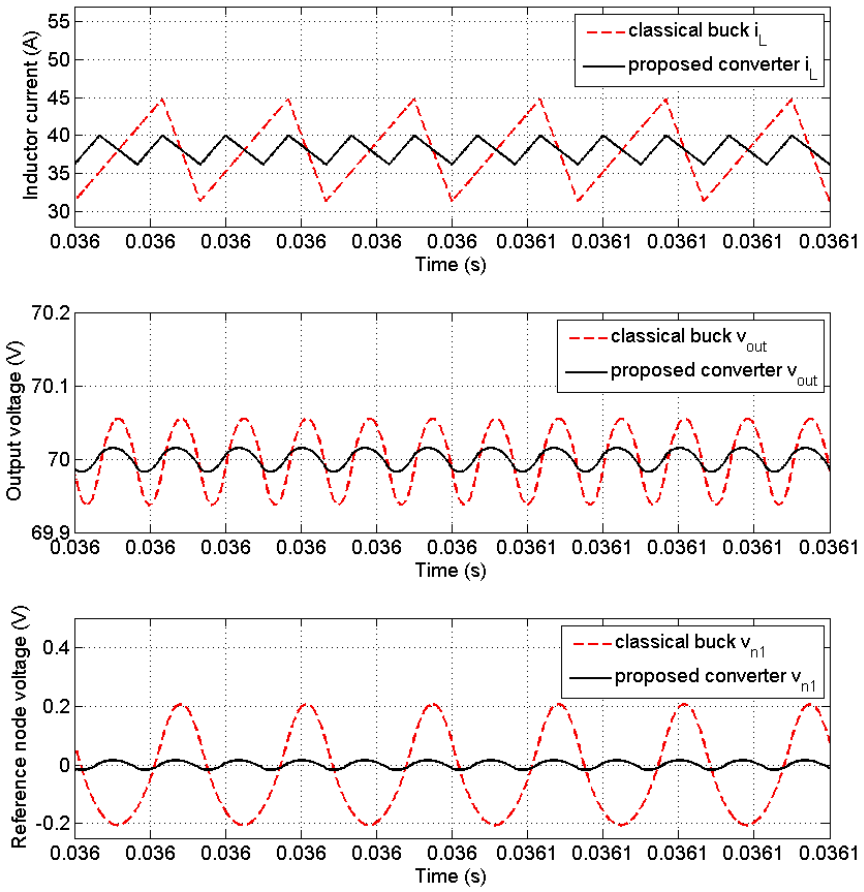


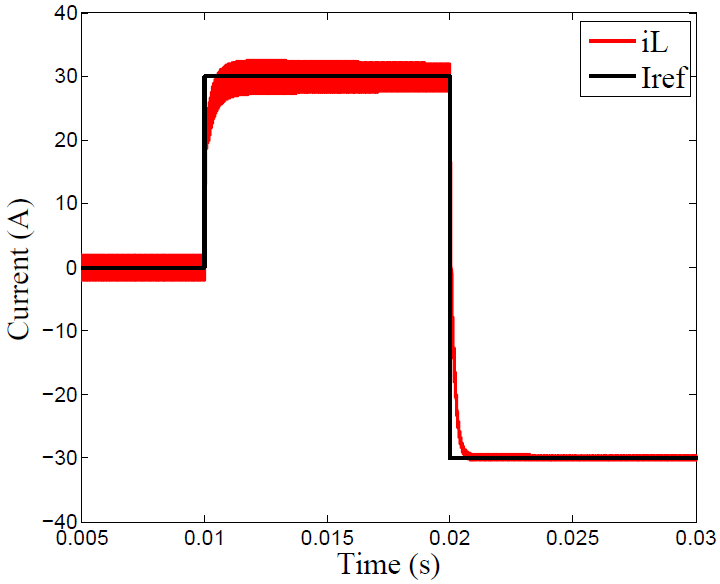
Figure 5.2: PLECS simulation and comparison between the proposed converter and the double-input single-output classical cascaded buck converter.

Variable	Classical Cascaded Buck	Proposed Converter
$\Delta i_{L,pp}$	13.43 A	3.78 A
$\Delta v_{out,pp}$	117 mV	32 mV
$\Delta v_{n1,pp}$	410 mV	32 mV

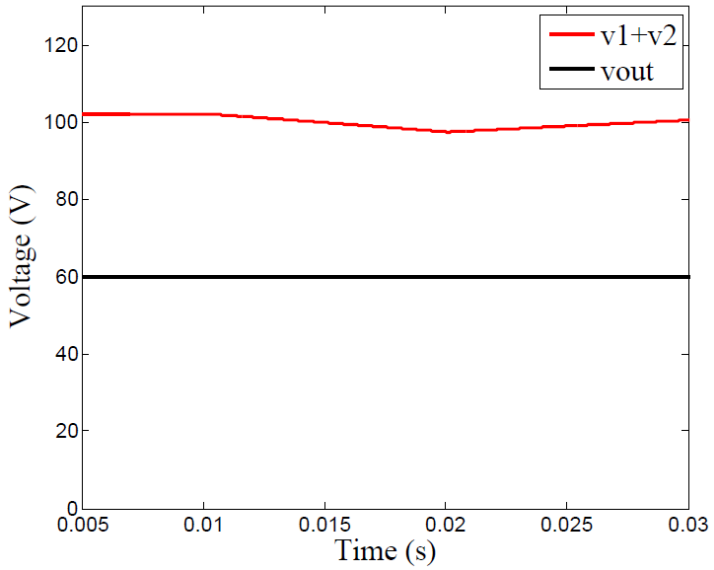
Table 5.2: Simulation comparison between the proposed converter and the double-input single-output classical cascaded buck converter.

5.1.2 Bidirectional Power Transfer

A closed loop simulation of the proposed converter is developed in Simulink. The circuit setup includes capacitors of 0.1F at the input ports to represent battery capacitance with initial voltages of 52 V and 50 V, respectively. The output port is connected to a dc voltage source of 60 V.



(a)



(b)

Figure 5.3: (a) Inductor current step response to both positive and negative current commands. (b) $v_1 + v_2$ compared to the output port voltage.

Fig. 5.3 (a) shows that the simulated converter is capable of bidirectional power transfer following both positive and negative I_{ref}. Fig. 5.3 (b) shows the corresponding voltage response to the current step. It can be seen that the sum of the input voltages decreases when the converter is discharging current to the output, and the sum of the input voltages increases when the converter is sinking current from the output.

5.1.3 Voltage Balancing

Fig. 5.4 shows the voltage balancing simulation results for the proposed converter in the same simulation setup in Fig. ??. It can be seen that the two input ports had an initial voltage difference of 2 V, and the voltage difference remained at 2 V when I_L is zero. During the nominal bidirectional operation of the proposed converter of non-zero reference current, the voltage difference between the input ports reduces, and the input voltages become balanced.

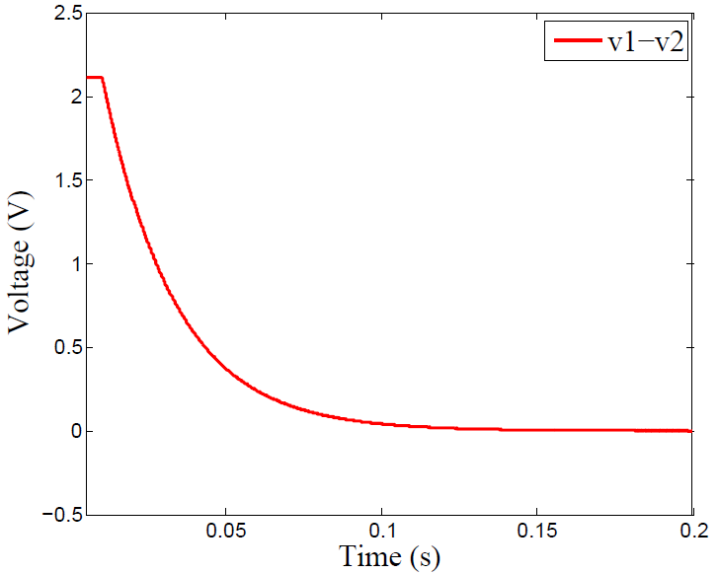
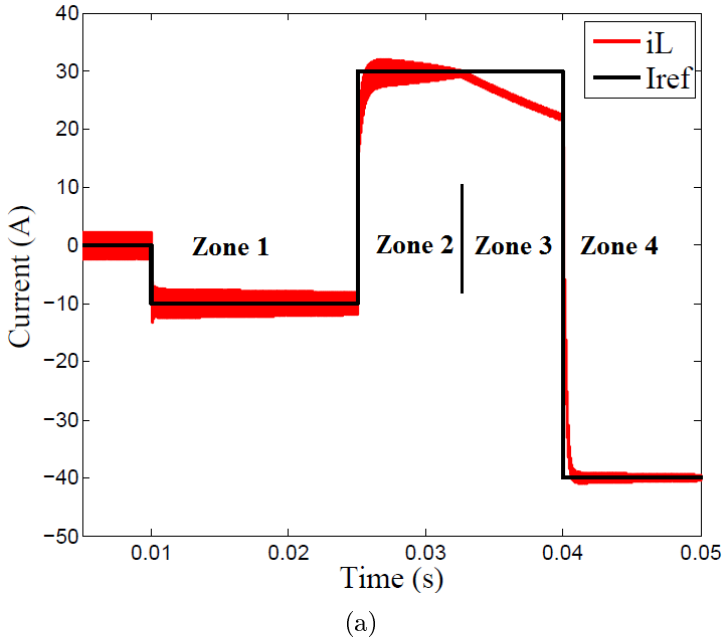


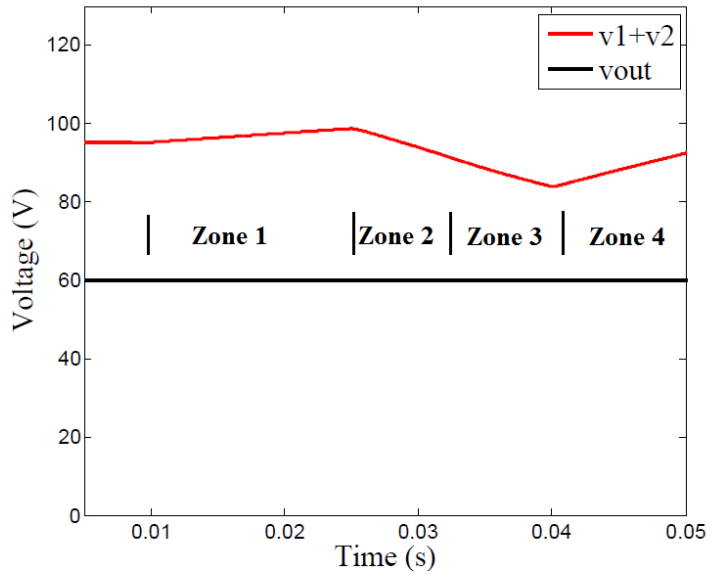
Figure 5.4: Voltage balancing simulation results for the proposed converter with initial input port voltages of 52 V and 50 V, respectively.

5.1.4 Controller Saturation

Controller saturation is an important concern in the control design as discussed in chapter 4.2. When the inputs of the converter are connected to batteries of different initial voltage and capacitance, either or both of the current controller and the delta controller can enter into saturation and affect the bidirectional power transfer and voltage balancing.



(a)



(b)

Figure 5.5: (a) Inductor current step response to both positive and negative current commands. (b) $v_1 + v_2$ compared to the output port voltage.

Consider a set of new simulation conditions where the battery capacitance for the input ports is reduced to 0.05 F, and the initial voltages are set to 50 V and 45 V, respectively. Fig. 5.5 (a) shows the inductor current response to I_{ref} with the new set of simulation conditions, and Fig. 5.6 shows the corresponding voltage balancing results. Both Fig. 5.5 and Fig. 5.6 are divided into zones 1 to 4 where different controller

saturation situations occur. Examining the controller saturation status in Fig. 5.7 reveals that the delta controller saturates in zones 1, 2, and 3 and the current controller saturates in zone 3. The following will analyze the effect of saturation on power transfer and voltage balancing in different zones.

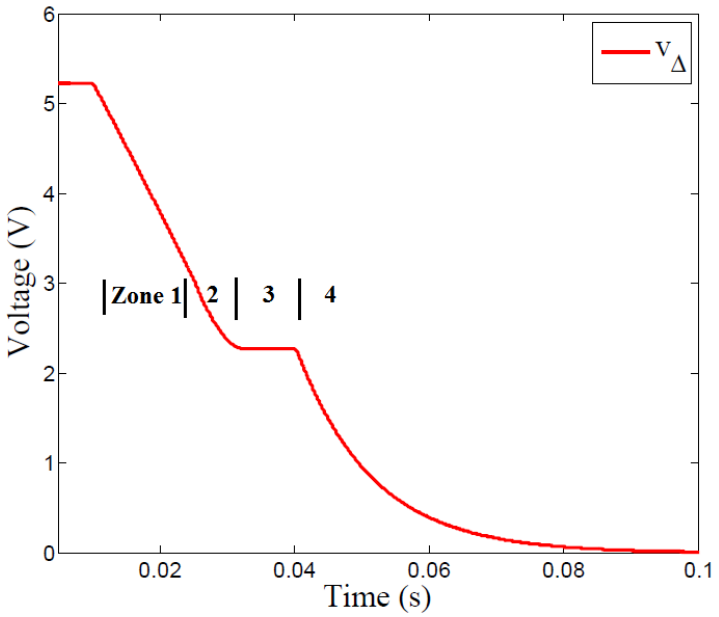


Figure 5.6: Voltage balancing simulation results for the proposed converter with initial input port voltages of 50 V and 45 V, respectively.

In zone 1, only the delta controller becomes saturated. Duty cyle values plotted in Fig. 5.8 show that d_Σ is approximately 0.6 and d_Δ is -0.35. The delta controller becomes saturated whenever untransformed duty command d_1 or d_2 becomes saturated according to (4.11) and (4.12). In this case, d_2 becomes saturated, and the inductor current is divided according to the saturation limit 0.05:0.95, where a majority of the current is channeled into input port V_2. As a result, v_Δ is reduced as shown in Fig. 5.6. It should be noted that as long as d_Δ is saturated and I_{ref} remains unchanged, I_1 and I_2 will also be constant, and consequently, v_Δ will change linearly as shown in zone 1 in Fig. 5.6. On the other hand, i_L is unaffected by the delta controller saturation shown in zone 1 in Fig. 5.5 (a). This is expected because $d_\Delta v_\Delta$ only appears as a disturbance in the current control loop as shown in Fig. 4.1, and its value is small compared to the control output $d_\Sigma v_\Sigma$.

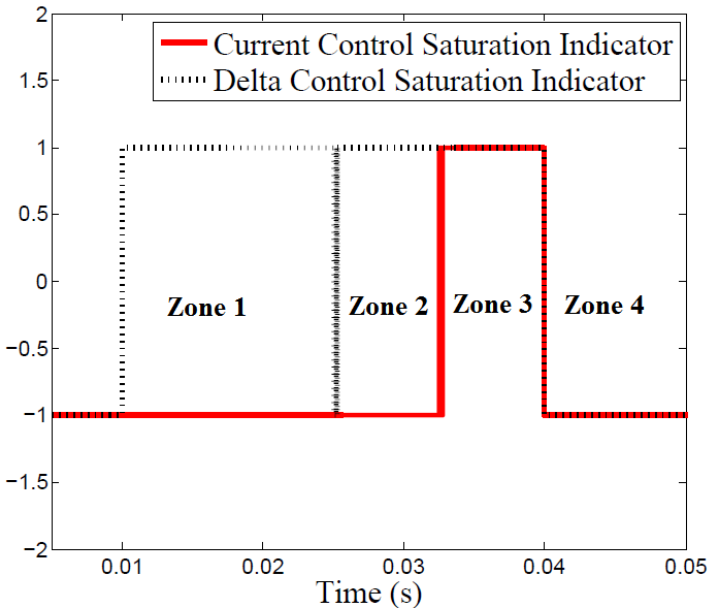


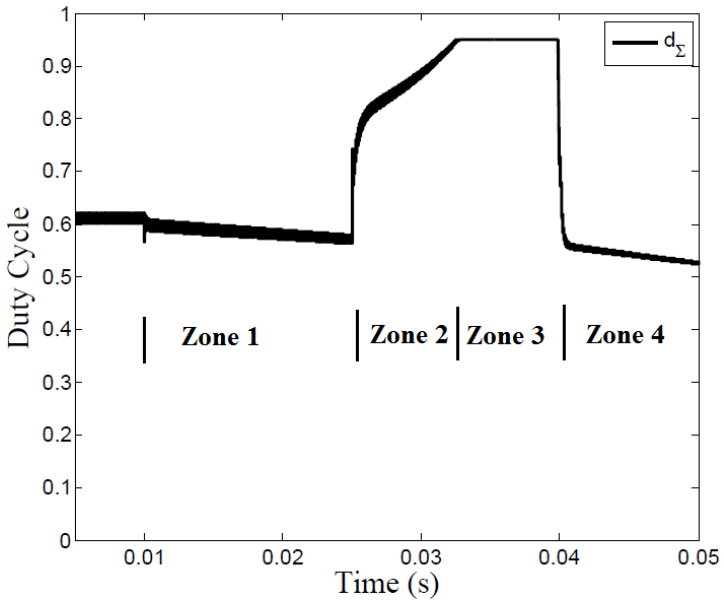
Figure 5.7: Current and delta controller saturation graph where a value of "1" indicates saturation.

In zone 2, I_{ref} changes sign, and the delta controller resets and becomes saturated again while the current controller remains unsaturated as shown in Fig. 5.7. Because the converter is discharging current to the output port, the sum of input port voltages drops as shown in Fig. 5.5 (b). The rest of the analysis is the same as in zone 1.

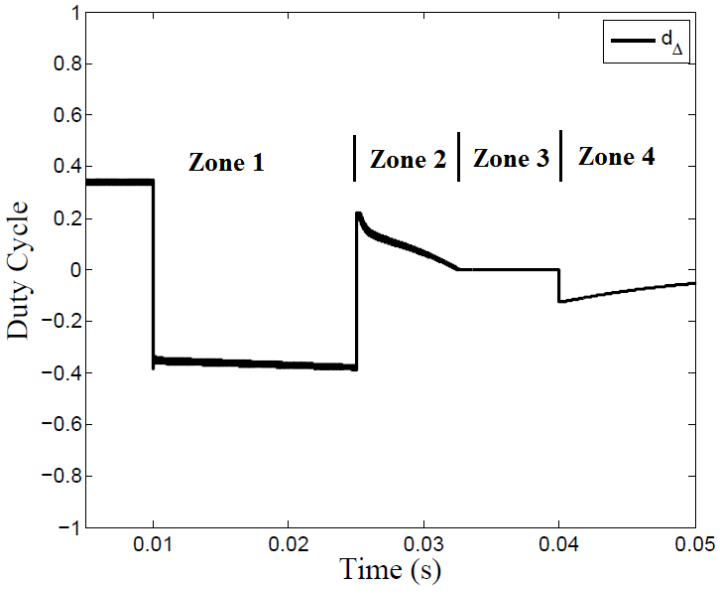
In zone 3, both the current and delta controllers are saturated as shown in Fig. 5.7. The saturation of the current controller in this zone is due to insufficient input battery voltage to support the required power transfer to the output. As we can see from Fig. 5.5 (b), the decrease of sum of input voltages starts in zone 2 and continues throughout zone 3 due to current discharge. As a result, d_Σ starts to increase in zone 2 and reaches its upper saturation limit in zone 3 as shown in Fig. 5.8 (a). Because the saturated current controller can no longer regulate i_L, i_L starts decreasing with a large time constant due to the battery capacitance and the inductor. The converter would either shut down when the input voltages reach their lower limits or in this case, a subsequent negative reference current command allows the batteries to be charged, and the current controller comes out of saturation due to its anti-windup mechanism. On the other hand, v_Δ remains constant in zone 3 as shown in Fig. 5.6. This is expected because when d_Σ becomes saturated, any non-zero d_Δ will cause d_1 or d_2 to be saturated according to (4.11) and (4.12). Consequently, the inductor current is drawn evenly from the input ports, and v_Δ remains unchanged in this case.

In zone 4, I_{ref} changes its sign again, and both controllers become unsaturated. The

converter resumes normal operation.



(a)



(b)

Figure 5.8: (a) Current controller duty cycle command d_Σ (b) Delta controller duty cycle command d_Δ.

5.2 Experimental Results

A 3.3 kW converter prototype rated at 40 A with component values shown in Table 5.1 is tested to verify converter switching ripple, bidirectional power transfer capability, and input voltage balancing performance. The experimental setup shown in Fig. 5.9 uses two stacks of 30 supercapacitors for energy storage. A Regatron TopCon Quadro bidirectional power supply is connected to the output port to regulate the output port voltage for closed loop operation. The following three subsections analyze and compare the experimental results with simulation to quantify the converter performance.

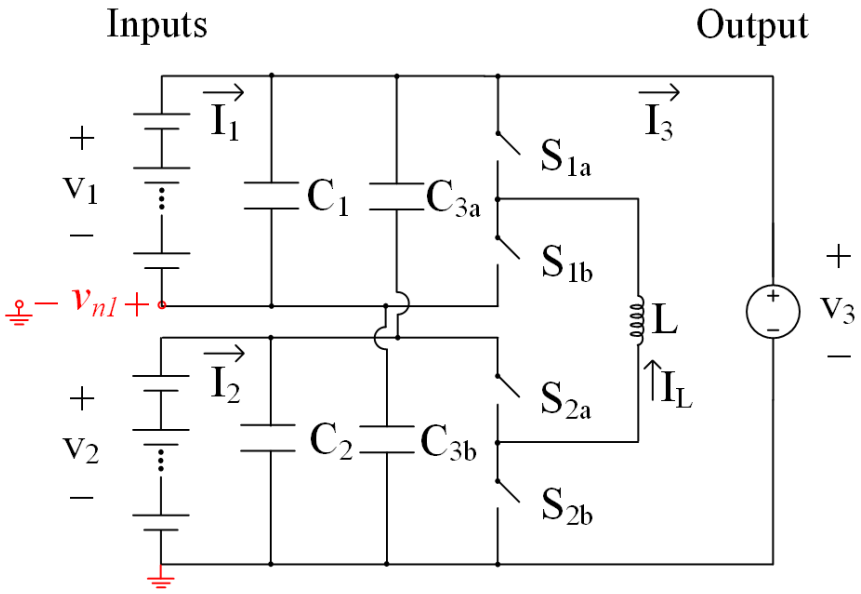


Figure 5.9: Experimental setup for closed loop operation of the proposed converter. A resistive load is replaced at the output for switching measurements.

5.2.1 Switching Performance

Fig. 5.10 shows the inductor current, output voltage, and input reference node voltage ripple at input voltages of 50 V and output voltage of 70 V. The average inductor current is 35 A. Table 5.3 compares the 120 kHz component of the experimental and simulation results. It can be seen that both the inductor current and output voltage ripple in the experiment closely match the simulation results.

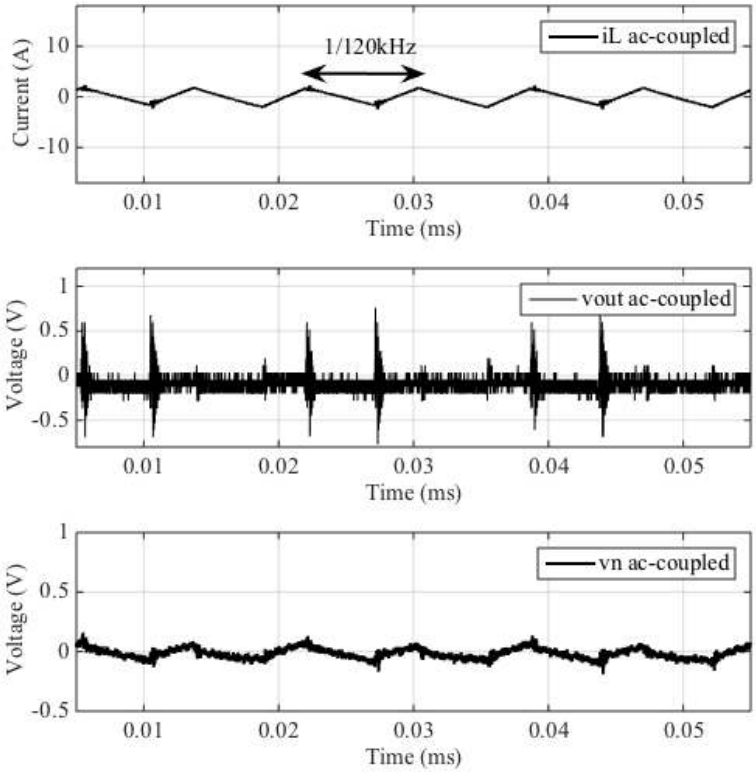


Figure 5.10: Inductor current, output voltage, and input reference node voltage ripple at input voltages of 50 V, output voltage of 70 V, and average inductor current of 35 A.

	Simulation	Experiment
$\Delta i_{L,pp}$	3.06 A	2.88 A
$\Delta v_{out,pp}$	33.6 mV	41.4 mV
$\Delta v_{n,pp}$	33.6 mV	99.2 mV

Table 5.3: Comparison of the experimental and simulated switching ripple of the proposed converter

The experimental input reference node ripple is higher than the simulation result due to input parasitic inductance and series resistance in the capacitors. In the experimental setup, the input sources are located away from the experimenter and the converter input ports due to safety precautions. Consequently, the introduction of parasitic inductance in the long connecting cables is unavoidable, and such parasitic inductance, while not modeled in the simulation, will cause voltage ripple to increase in the experiment. This

parasitic inductance will be reduced when the input sources are connected directly to the input ports in an industrial setup. On the other hand, soldering of through hole capacitors in the construction of the prototype adds parasitic series resistance. Such series resistance causes a voltage drop that increases the ripple during the interleaved switching and can be observed in the input reference node voltage ripple in Fig. 5.10. Nevertheless, the experimental input reference node ripple of the proposed converter with the input parasitic inductance and capacitor series resistance is still approximately 4 times better than the classical cascaded buck converter. It should be noted that the peak-to-peak value of the input reference node voltage ripple is about 0.1 V. For conservative estimates of human impedance of 1000 to 2000 Ω in dry conditions [7], the resulting current of the proposed converter is well below the 0.5 mA startle reaction current limit as recommended by UL [1].

5.2.2 Bidirectional Power Transfer

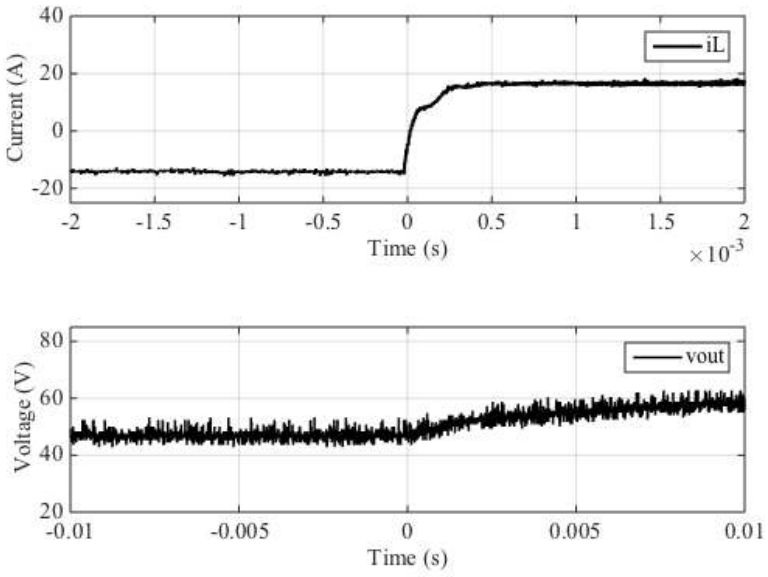
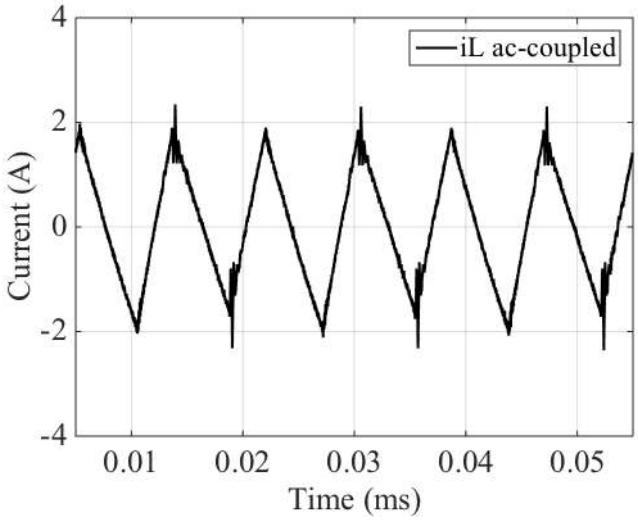


Figure 5.11: Inductor current and output voltage dynamic response due to a step change in the reference current of the current controller. The output voltage is regulated by an external power supply.

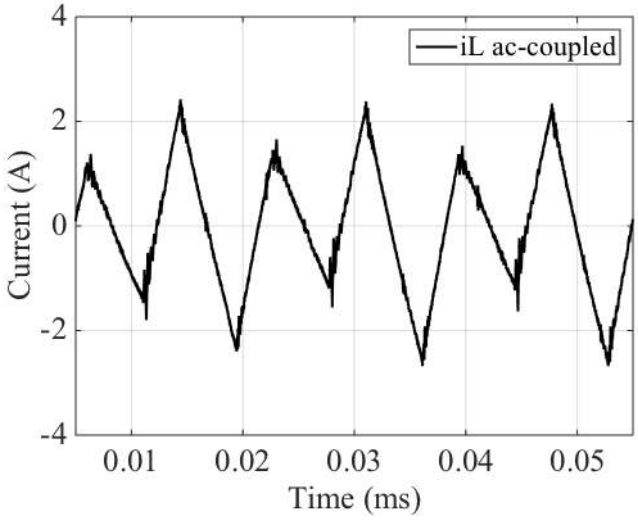
Fig. 5.11 shows the step response for a transition between positive and negative i_L^{ref} command. It should be noted that the output voltage dynamics are due to the limited response time of the V_3 voltage regulator within the Regatron power supply combined

with the line inductance between the power supply and the test setup. Because the output voltage is held positive, it is clear that bidirectional current flow constitutes bidirectional power transfer between the input ports and the output port.

5.2.3 Voltage Balancing



(a)



(b)

Figure 5.12: (a) Inductor current (ac-coupled) at input voltages of 50 V and output voltage of 70 V. (b) Inductor current (ac-coupled) at input voltages of 55 V and 45 V and output voltage of 70 V.

Unbalanced input voltages can lead to dangerous overcharge conditions and can affect the switching performance of a converter, causing increased switching ripple and somewhat reduced efficiency.

Fig. 5.12 compares the inductor current ripple due to balanced and unbalanced input voltages for a given v_{Σ}. It can be seen that unbalanced voltages can cause $\Delta i_{L,pp}$ to be 25% higher when the voltage deviation from the mean is approximately $\pm$ 10%.

The proposed converter can perform input voltage balancing for positive and negative power flows. Fig. 5.13 shows the voltage balancing results for two different initial charging states, one in the charging mode, and the other in the discharging mode. In both cases, the difference voltage is regulated to zero and the supercapacitor voltages become, and remain, balanced.

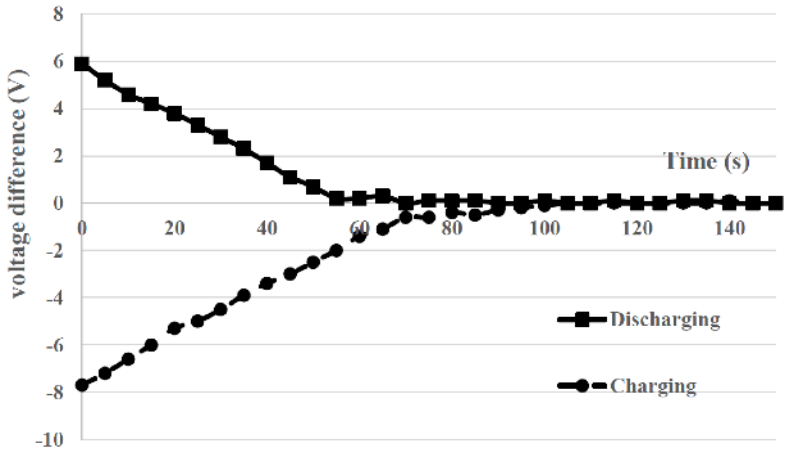


Figure 5.13: Voltage balancing results for both charging and discharging operations. Zero voltage difference indicates balanced battery voltages at the input ports.

5.2.4 Efficiency

The switching ripple suppression characteristics of the proposed converter contributes to reduced filter requirements and improved efficiency. Fig. 5.14 shows the efficiency data calculated and recorded from measurements with Yokogawa WT3000 high-precision power analyzer at rated input voltages of 60 V and upto rated output current of 40 A. It should be noted that Yokogawa WT3000 has four measuring terminals, and each terminal has a current limit of 30 A. In order to measure upto the rated output current, two terminals are dedicated to the output port. It can be seen in Fig. 5.14 that the converter can operate at above 99% efficiency over a wide range of duty cycles and input powers due to the significant reduction in switching ripple and reduced component count.

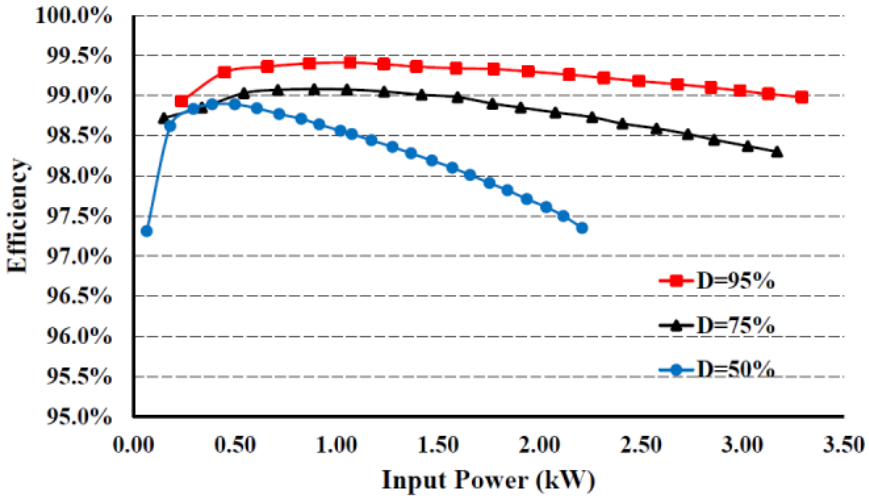


Figure 5.14: Converter efficiency measurements for various open loop duty cycle values at rated input port voltages of 60 V and upto rated output current of 40 A.

To further validate the efficiency measurements, an efficiency analysis is conducted on a buck converter using the same experimental components and PCB board with available datasheet information and measurements. This analysis in included in Appendix A.

Chapter 6

Cascaded Configuration

6.1 Topology and Variations

The proposed converter is modular and can be extended to a $(2K+1)$-port converter by cascading with itself or its variations. The proposed cascaded converter in Fig. 6.1 has $(2K+1)$-port with a single output port capacitor. This cascaded configuration will be used for control analysis and simulation to demonstrate bidirectional power transfer and voltage balancing capability. Other variations of the cascaded configuration are shown in Fig. 6.2 to 6.4.

6.2 Control Strategy

The control objectives of the cascaded configuration are the same as the proposed single module converter albeit the increased control complexity. The principles of the sum and difference control can be extended to include intra-module as well as inter-module voltage balancing for a system of K cascaded modules. (6.1) and (6.2) show the transformed variable of module voltage sum and intra-module voltage difference of the two input ports similar to the transformation shown in (4.4) and (4.5) for the single module case with the addition of a subscript i to identify the specific module in this cascaded system.

$$v_{i,\Sigma} = v_{i,1} + v_{i,2} \tag{6.1}$$

$$v_{i,\Delta} = v_{i,1} - v_{i,2} \tag{6.2}$$

(6.3) and (6.4) introduce two new variables for the control. v^* is the average module sum voltage of all K modules in the cascaded system, and $\tilde{v}_i$ is the inter-module difference voltage between the actual module sum voltage $v_{i,\Sigma}$ and the system average module sum

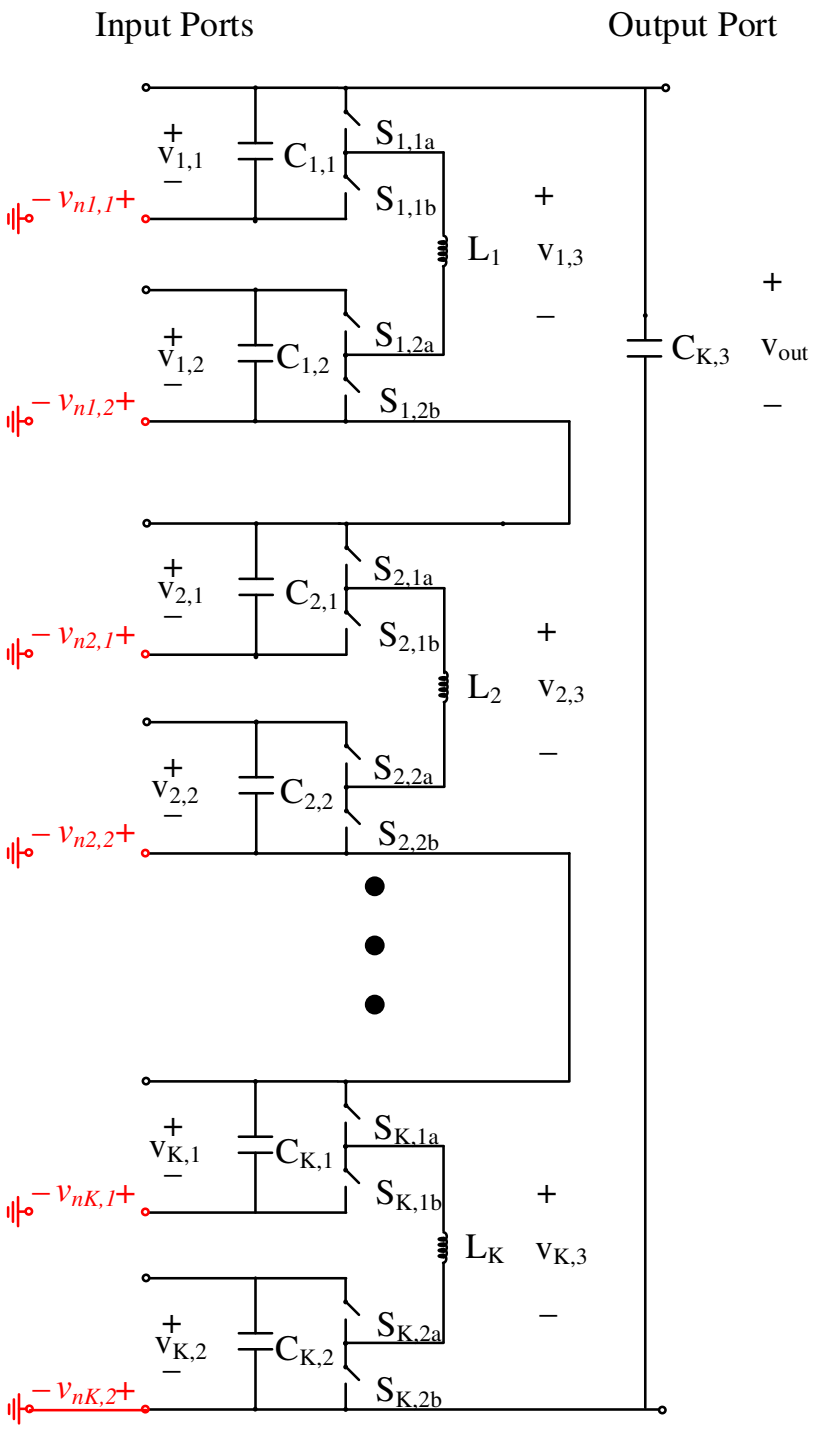


Figure 6.1: Proposed cascaded bidirectional multi-port dc-dc converter.

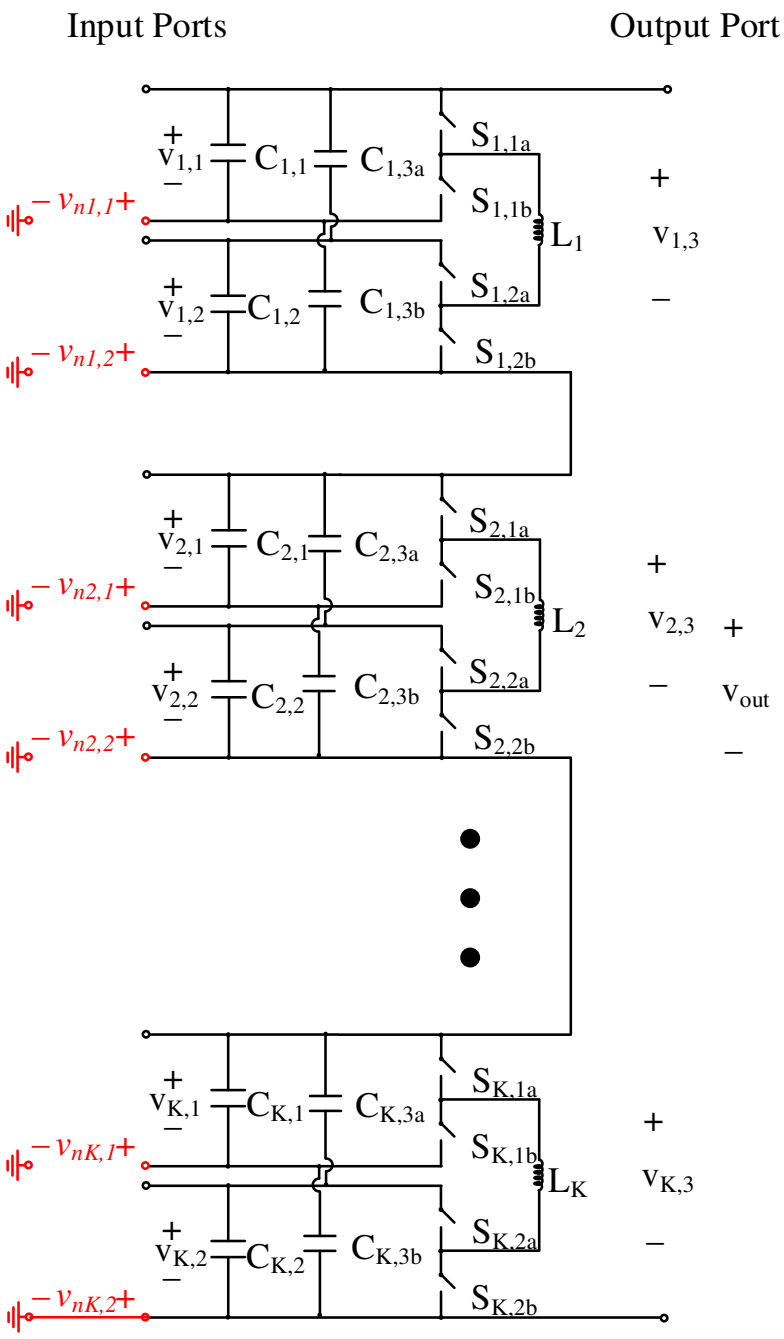


Figure 6.2: Proposed cascaded bidirectional multi-port dc-dc converter variant 1.

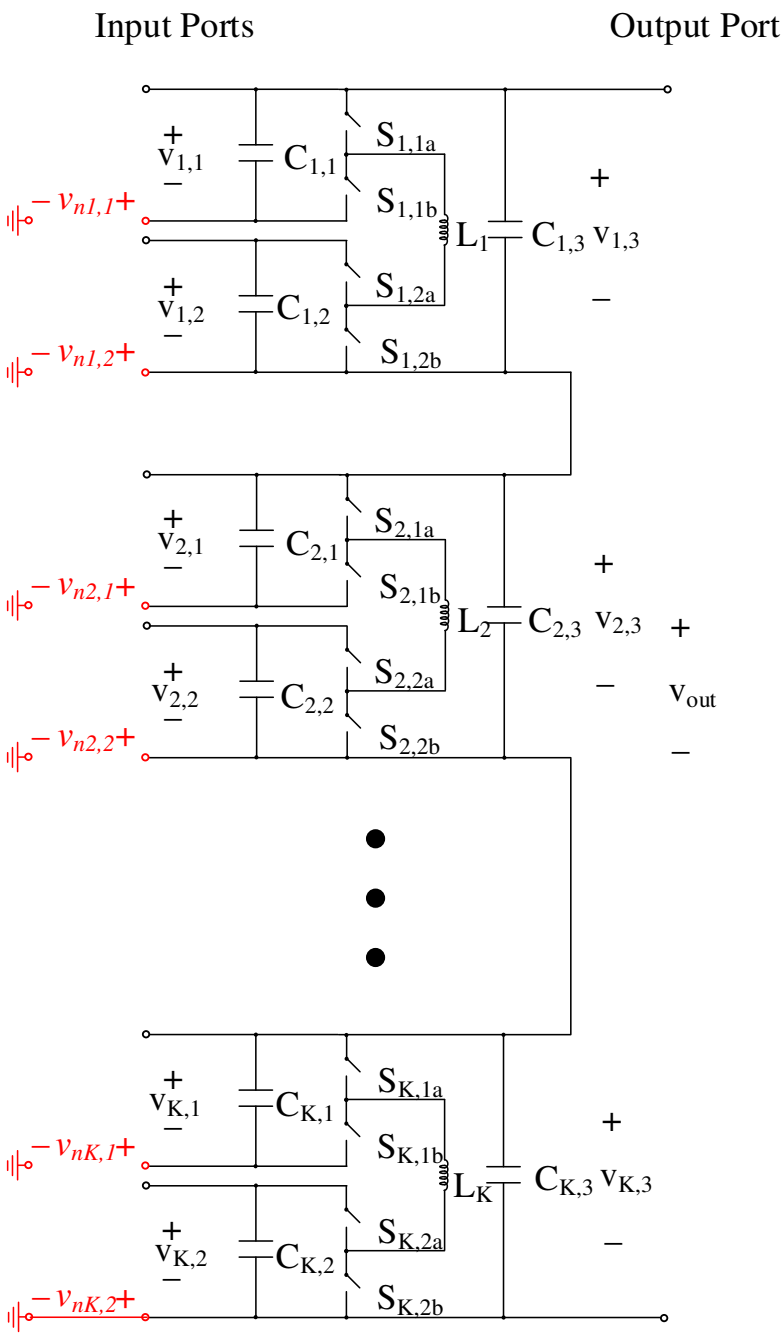


Figure 6.3: Proposed cascaded bidirectional multi-port dc-dc converter variant 2.

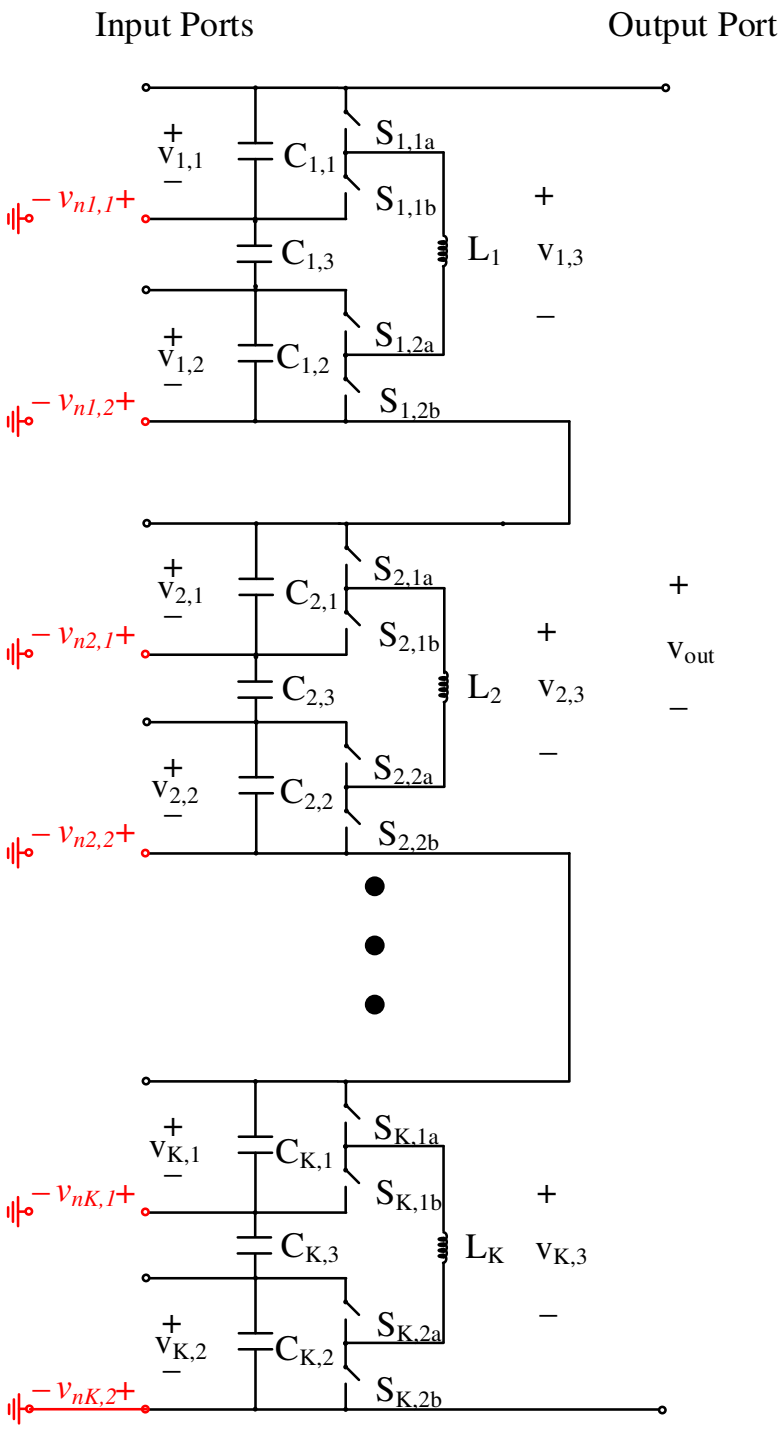


Figure 6.4: Proposed cascaded bidirectional multi-port dc-dc converter variant 3.

voltage v^*. Consequently, v^* will serve as a moving target where all module voltages in the system will converge to achieve inter-module voltage balancing.

$$v^* = \frac{1}{K}\sum_{i=1}^{K} v_{i,\Sigma} \tag{6.3}$$

$$\tilde{v}_i = v_{i,\Sigma} - v^* \tag{6.4}$$

Similar to the transformed voltage variables, transformed duty cycle variables are defined in (6.5) to (6.8), where the actual duty command to every pair of complementary switches can be calculated using (6.9) and (6.10).

$$d_{i,\Sigma} = \frac{d_{i,1} + d_{i,2}}{2} \tag{6.5}$$

$$d_{i,\Delta} = \frac{d_{i,1} - d_{i,2}}{2} \tag{6.6}$$

$$d^* = \frac{1}{K}\sum_{i=1}^{K} d_{i,\Sigma} \tag{6.7}$$

$$\tilde{d}_i = d_{i,\Sigma} - d^* \tag{6.8}$$

$$d_{i,1} = d^* + \tilde{d}_i + d_{i,\Delta} \tag{6.9}$$

$$d_{i,2} = d^* + \tilde{d}_i - d_{i,\Delta} \tag{6.10}$$

The transformation of variables will lead to a control system similar to the single model case. (6.11) to (6.13) show the system of equations with the transformed variables for the proposed cascaded structure. The K inductors connected in series form an equivalent single inductance of KL. The simplified current equation in (6.11) has three disturbance terms that resembles the current equation in the single module case with the addition of a sum of products that includes intra-module voltage differences $\tilde{v}_i$. The inter-module voltage difference equation shown in (6.12) is the same as in the single module control. However, because the system contains K modules, there are K equations of (6.12). Similarly, there are also K equations of (6.13) that represents the voltage sum of each module in the form of $(v^* + \tilde{v}_i)$ derived from (6.4). There are a total of $(2K + 1)$ equations in the system, however, they are not all independent. (6.14) shows that the

sum of all intra-module voltage difference is zero, and consequently, only $(K-1)$ of the K equations of (6.4) are independent.

$$\begin{aligned} KL\frac{di_L}{dt} &= \sum_{i=1}^{K}(d_{i,1}v_{i,1} + d_{i,2}v_{i,2}) - v_{out} \\ &= \sum_{i=1}^{K} d_{i,\Sigma}v_{i,\Sigma} + \sum_{i=1}^{K} d_{i,\Delta}v_{i,\Delta} - v_{out} \\ &= Kd^*v^* + \sum_{i=1}^{K}\tilde{d}_i\tilde{v}_i + \sum_{i=1}^{K} d_{i,\Delta}v_{i,\Delta} - v_{out} \end{aligned} \tag{6.11}$$

$$\left.\begin{aligned} C\frac{dv_{i,\Delta}}{dt} &= C\frac{dv_{i,2}}{dt} - C\frac{dv_{i,1}}{dt} \\ &= -d_{i,2}i_L - (-d_{i,1}i_L) \\ &= -2i_L d_{i,\Delta} \end{aligned}\right\} \quad i = 1, ..., K \tag{6.12}$$

$$\left.\begin{aligned} C\frac{d(v^* + \tilde{v}_i)}{dt} &= C\frac{dv_{i,2}}{dt} + C\frac{dv_{i,1}}{dt} \\ &= -d_{i,2}i_L + (-d_{i,1}i_L) \\ &= -2i_L(d^* + \tilde{d}_i) \end{aligned}\right\} \quad i = 1, ..., K \tag{6.13}$$

$$\begin{aligned} \sum_{i=1}^{K}\tilde{v}_i &= \sum_{i=1}^{K}(v_{i,\Sigma} - v^*) \\ &= \sum_{i=1}^{K} v_{i,\Sigma} - Kv^* \\ &= 0 \end{aligned} \tag{6.14}$$

Fig. 6.5 shows the proposed control block diagrams. There are: one current controller, K delta controllers to regulate different battery voltages $v_{i,\Delta}$ of each module to zero, and $(K-1)$ tilde controllers to regulate different voltage sum $v_{i,\Sigma}$ of each module to the average module voltage sum v^* of the cascaded structure. The current controller follows i_L^{ref} command and ensures system-level bidirectional power transfer between the output and input ports. The K delta controller works in parallel to perform intra-module balancing and ensures the voltages of the two input ports in the same module are the same. The tilde controllers have system module average voltage v^* as the reference, which will cause all module sum voltages to converge to v^*, resulting in zero $\tilde{v}_i$ or in other

words, achieving desired inter-module voltage balancing. The $(K-1)$ tilde controllers will compute $(K-1)$ $\tilde{d}_i$'s where $\tilde{d}_K$ is computed by (6.15) due to the relationship found in (6.16).

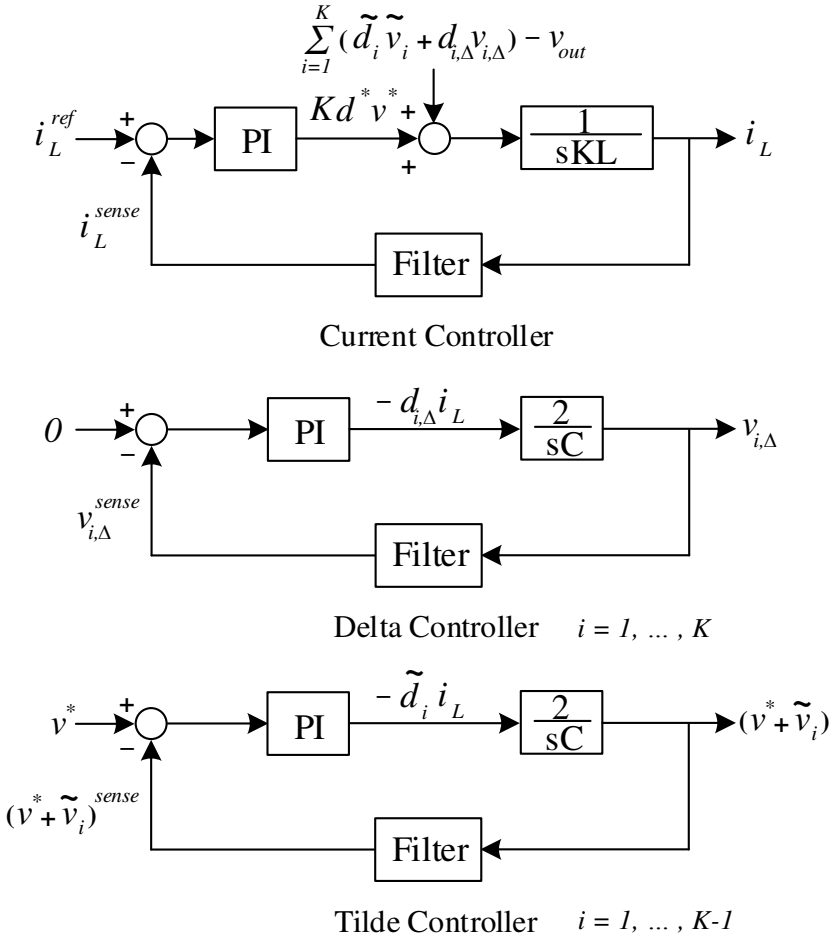


Figure 6.5: Block diagrams of the controllers for the cascaded converter.

$$\tilde{d}_K = -\sum_{i=1}^{K-1} \tilde{d}_i \tag{6.15}$$

$$\begin{aligned}\sum_{i=1}^{K}\tilde{d}_i &= \sum_{i=1}^{K}(d_{i,\Sigma}-d^*)\\ &= \sum_{i=1}^{K}d_{i,\Sigma}-Kd^*\\ &= 0\end{aligned} \tag{6.16}$$

6.3 Simulation Results

To validate the control strategy for the cascaded configuration, a three module model is developed in Simulink.

In this simulation system, the battery capacitance for each input port is 0.1 F, and the total inductance of the cascaded structure is 26.2 μH. The initial input voltage for each port is shown in Table 6.1. The output port is connected to a dc voltage source of 150 V via a line inductance of 50 μH.

Fig. 6.6 shows the converter current step response to both positive and negative I_{ref}. Fig. 6.7 shows the voltage balancing results of the proposed cascaded converter. It can be seen that all input port voltages converge to the global moving average v^* and consequently achieves voltage balancing. In summary, the cascaded configuration is capable of bidirectional power transfer as well as battery voltage balancing.

	$v_{i,1}$	$v_{i,2}$
Module 1	55 V	53 V
Module 2	51 V	49 V
Module 3	47 V	45 V

Table 6.1: Initial input voltage for each port for the cascaded converter.

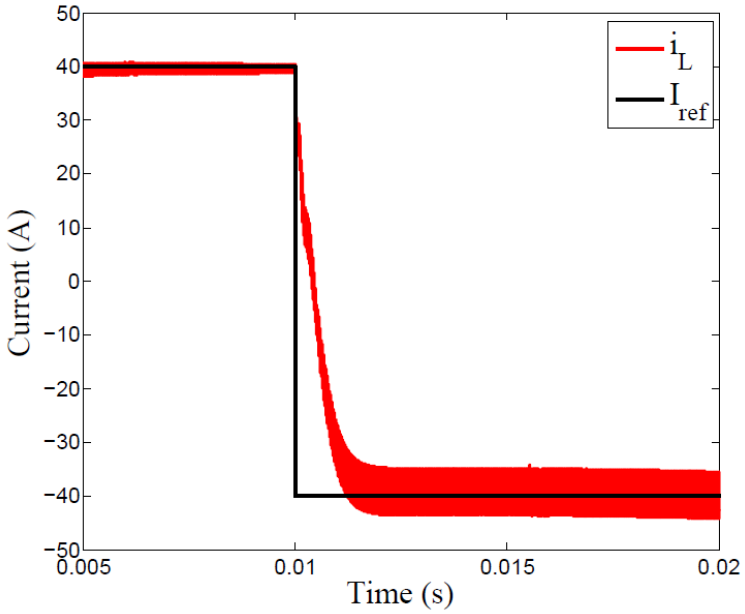


Figure 6.6: Inductor current step response of the cascaded configuration.

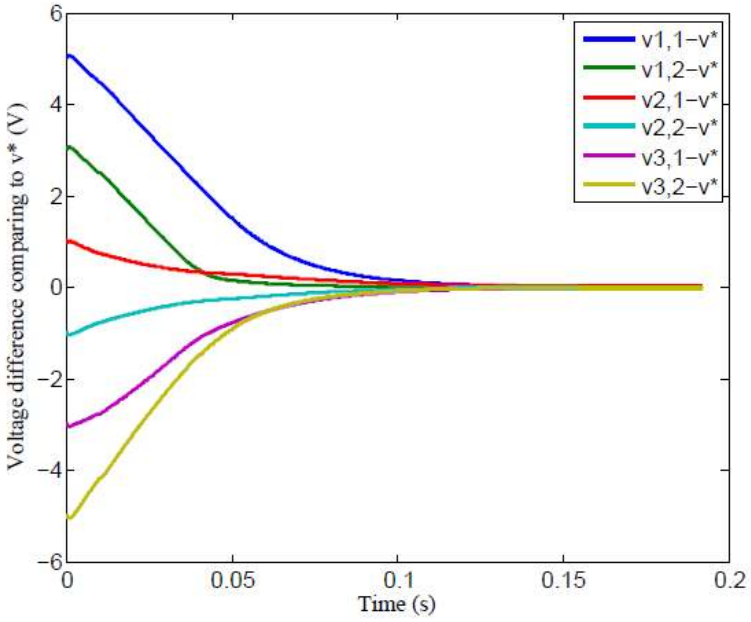


Figure 6.7: Simulated voltage balancing results of the proposed cascaded configuration.

Chapter 7

Conclusion

In this work, a non-isolated multi-port dc-dc converter and its variants are proposed. The proposed converter is capable of input voltage balancing for bidirectional power transfer with limited ground leakage current. The salient feature of the proposed converter is its reduced filter requirements and component count, which can lead to improved efficiency or provide significant cost savings from reduced filter component size and cost.

An interleaved switching strategy is developed for the converter such that the inductor current ripple is reduced and appears at doubling of the physical switching frequency.

To achieve the objectives of regulating output current and voltage balancing of the input ports, a sum and difference control strategy is developed for the proposed converter, where a current controller is used to regulate output current, and a delta controller is used to regulate input port battery voltages to zero. Practical control challenges such as voltage balancing oscillation and control saturation are also investigated.

The proposed converter can be extended to a $(2K + 1)$-port converter by cascading with itself or its variations. Several cascaded configurations are proposed, and one of them is selected for analysis and control design. The control strategy for a single module is extended to the cascaded configuration, where there are: one current controller, K delta controllers to regulate intramodule battery voltages to zero, and $(K - 1)$ tilde controllers to regulate the voltage sum of each module to the average module voltage of the cascaded structure.

Simulation models for the proposed converter and three-module cascaded configuration are built in Simulink for functionality analysis. Both the proposed converter and cascaded configuration are able to perform battery voltage balancing of the input ports while maintaining nominal bidirectional power transfer between the input ports and the output port. A simulation comparison between the proposed converter and a double-input single-output classical cascaded buck converter demonstrates that the peak-to-peak inductor

current ripple is reduced by 3.6 times while the output voltage and input reference node voltage ripple are reduced by 3.7 and 12.8 times, respectively. This significant reduction in switching ripple leads to a highly efficient converter.

Experimental testing with input power up to 3.3 kW confirms the simulation results and demonstrates that the converter prototype has above 99% efficiency over a wide range of input power. Furthermore, one cascaded configuration of the proposed converter and its control method are analyzed and simulated using Simulink to demonstrate bidirectional power transfer capability and voltage balancing for multiple input ports. It is shown in this research that the proposed converter offers a highly efficient and cost-effective means for achieving multi-port power processing and is well-suited for applications in DG and EV.

7.1 Future Research

The following are some areas of interest for future investigations related to this thesis:

- The variants of the cascaded configuration of the proposed converter shown in Fig. 6.2 to 6.4 have different capacitor placement. Consequently, these cascaded variants all have different control dynamics and should be studied individually. It is expected that more feedback signals might be needed for these converters to enable regulation of the internal voltage dynamics introduced by the extra capacitors;
- Further testing on the prototype to quantify and categorize power losses in addition to the efficiency analysis shown in Appendix A in order to better understand the difference between measured losses and calculated losses; and
- Further testing on the prototype with actual battery packs instead of super capacitors to verify the control for bidirectional power transfer and voltage balancing.

Bibliography

[1] Leakage current for appliances. *UL 101*, Apr. 2002.

[2] A. Affanni, A. Bellini, G. Franceschini, P. Guglielmi, and C. Tassoni. Battery choice and management for new-generation electric vehicles. *IEEE Trans. Ind. Electron.*, 52(5):1343–1349, Oct. 2005.

[3] A.I. Bratcu, I. Munteanu, S. Bacha, D. Picault, and B. Raison. Cascaded dc-dc converter photovoltaic systems: Power optimization issues. *IEEE Trans. Ind. Electron.*, 58(2):403–411, Feb. 2011.

[4] G. Buticchi, D. Barater, E. Lorenzani, and G. Franceschini. Digital control of actual grid-connected converters for ground leakage current reduction in pv transformerless systems. *IEEE Trans. Ind. Informat.*, 8(3):563–572, Aug. 2012.

[5] M. Calais and V.G. Agelidis. Multilevel converters for single-phase grid connected photovoltaic systems-an overview. In *Proc. ISIE Int. Symp.*, volume 1, pages 224–229 vol.1, 1998.

[6] M. Muneeb Ur Rehman M. Evzelman R. Zane Y. Levron D. Costinett, K. Hathaway and D. Maksimovic. Active balancing system for electric vehicles with incorporated low voltage bus. In *Applied Power Electronics Conference and Exposition (APEC)*, pages 16–20, 2014.

[7] D. Dorr. Determining voltage levels of concern for human and animal response to ac current. In *Power Energy Society General Meeting*, pages 1–6, 2009.

[8] YuanChuan Liu and YaowMing Chen. A systematic approach to synthesizing multi-input dc/dc converters. In *Power Electronics Specialists Conf.*, pages 2626–2632, 2007.

[9] O. Lopez, R. Teodorescu, F. Freijedo, and Jesus DovalGandoy. Leakage current evaluation of a singlephase transformerless pv inverter connected to the grid. In *Applied Power Electronics 22nd Ann Conf.*, pages 907–912, 2007.

[10] A. Marquez, J.I. Leon, S. Vazquez, and L.G. Franquelo. Advanced control of a multilevel cascaded h-bridge converter for pv applications. In *Industrial Electronics Society, IECON 2014 - 40th Ann Conf.*, pages 4548–4553, 2014.

[11] J. M A Myrzik and M. Calais. String and module integrated inverters for single-phase grid connected photovoltaic systems - a review. In *Power Tech Conf. Proc., Bologna*, volume 2, pages 8 pp. Vol.2–, 2003.

[12] T.H. Phung, J.C. Crebier, and Y. Lembeye. Voltage balancing converter network for series-connected battery stack. In *38th Ann. Conf. on IEEE Industrial Electronics Society*, pages 3007–3013, 2012.

[13] Zhijun Qian, O. Abdel-Rahman, Haibing Hu, and I. Batarseh. An integrated three-port inverter for stand-alone pv applications. In *Energy Conversion Congress and Exposition (ECCE)*, pages 1471–1478, 2010.

[14] Lars Rundqwist. *Anti-Reset Windup for PID Controllers*. PhD thesis, Lund Institute of Technology, 1991.

[15] E. Serban, M. Ordonez, and C. Pondiche. Dc-bus voltage range extension in 1500 v photovoltaic inverters. *IEEE Trans. Emerg. Sel. Topics Power Electron.*, 3(4):901–917, Dec 2015.

[16] L. Solero, A. Lidozzi, and J.A. Pomilio. Design of multiple-input power converter for hybrid vehicles. *IEEE Trans. Power Electron.*, 20(5):1007–1016, Sep. 2005.

[17] Truman C. Surbrook, Norman D. Reese, and Angela M. Kehrle. Stray voltage: Sources and solutions. *IEEE Trans. Ind. Appl.*, IA-22(2):210–215, Mar. 1986.

[18] G. Vazquez, P.R. Martinez-Rodriguez, J.M. Sosa, G. Escobar, and M.A. Juarez. Transformerless single-phase multilevel inverter for grid tied photovoltaic systems. In *Industrial Electronics Society 40th Ann. Conf.*, pages 1868–1874, 2014.

[19] F. Vellucci, G. Pede, F. D'Annibale, A. Mariani, R. Roncella, R. Saletti, F. Baronti, and G. Fantechi. Development and realization of lithium-ion battery modules for starting applications and traction of off-road electric vehicles. In *Electric Vehicle Symposium and Exhibition (EVS27)*, pages 1–10, Nov 2013.

[20] G.R. Walker and P.C. Sernia. Cascaded dc-dc converter connection of photovoltaic modules. *IEEE Trans. Power Electron.*, 19(4):1130–1139, July 2004.

[21] Zedong Zheng, Kui Wang, Lie Xu, and Yongdong Li. A hybrid cascaded multilevel converter for battery energy management applied in electric vehicles. *IEEE Trans. Power Electron.*, 29(7):3537–3546, July 2014.

Appendix A

Efficiency Analysis

An accurate theoretical loss model is important in quantifying and attributing power loss to better understand converter behaviour. It is also important in deciding thermal components of the converter. In this section, a power loss analysis is performed, and the losses are grouped into three categories based on the location of the loss. More specifically, the three groups of losses considered are MOSFET losses, inductor losses and other circuit conduction losses. The theoretical power losses are further studied by comparing with measured total power loss through curve fitting and coefficient matching. Because both the proposed converter and the comparable classical cascaded buck converter contain two buck switching cells, the following loss analysis is performed on a single buck converter with actual components selected for the proposed converter as shown in Fig. A.1.

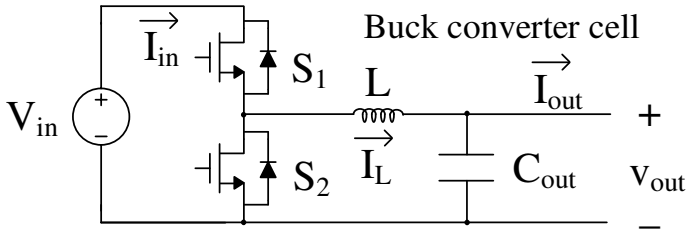


Figure A.1: A synchronous buck converter cell used for loss analysis.

A.0.1 MOSFET Losses

MOSFET losses include switching loss, conduction loss, body diode reverse recovery loss and conduction loss during dead time. More specifically, (A.1) and (A.2) describe the power that each of the MOSFET switches S_1 and S_2 needs to dissipate through heat.

$$P_{s1} = P_{s1,on} + P_{s1,off} + P_{s1,cond} + P_{rr} \tag{A.1}$$

$$P_{s2} = P_{s2,on} + P_{s2,off} + P_{s2,cond} + P_{diode,cond} \tag{A.2}$$

(A.3) to (A.10) show detailed equations on explicit loss calculations, and variables used are summarized in Table A.1. It should be noted that R_{ds} is temperature dependent.

$$P_{s1,on} = \frac{1}{2} V_{block} I_{ds,on} (t_{ri} + t_{fu}) f_s \tag{A.3}$$

$$P_{s1,off} = \frac{1}{2} V_{block} I_{ds,off} (t_{ru} + t_{fi}) f_s \tag{A.4}$$

$$P_{s2,on} = \frac{1}{2} V_{diode} I_{ds,off} t_{ri} f_s \tag{A.5}$$

$$P_{s2,off} = \frac{1}{2} V_{diode} I_{ds,on} t_{fi} f_s \tag{A.6}$$

$$P_{s1,cond} = R_{ds(T_1)} I_{L,rms}^2 D \tag{A.7}$$

$$P_{s2,cond} = R_{ds(T_2)} I_{L,rms}^2 (1 - D) \tag{A.8}$$

$$P_{diode,cond} = 2 V_{diode} I_L t_{dt} f_s \tag{A.9}$$

$$P_{rr} = Q_{rr} \frac{V_{block}}{V_{datasheet}} V_{block} f_s \tag{A.10}$$

Symbol	Definition	Source	Value
V_{block}	Switch blocking voltage	Operating point	60 V
$V_{datasheet}$	Blocking voltage	Datasheet	40 V
V_{diode}	Diode forward voltage	Datesheet	1.2 V
I_L	Average inductor current	Operating point	Varies
$I_{ds,on}$	Inductor current before MOSFET S_1 is switched on	Operating point	Varies
$I_{ds,off}$	Inductor current before MOSFET S_1 is switched off	Operating point	Varies
R_{ds}	Drain-source resistance	Datasheet	3.75 mΩ (25 °C)
		calculated	5.37 mΩ (108 °C)
R_L	Inductor resistance	Datasheet	1.51 mΩ
R_c	Connection resistance	Measurement	6 mΩ
$I_{L,rms}$	Inductor RMS current	Operating point	Varies
t_{ri}	Current rise time	Datasheet	79 ns
t_{fi}	Current fall time	Datasheet	14 ns
t_{ru}	Voltage rise time	Measurement	45 ns
t_{fu}	Voltage fall time	Measurement	45 ns
t_{rr}	Reverse recovery time	Datasheet	73 ns
t_{dt}	dead time	User defined	200 ns
Q_{rr}	Reverse recovery charge	Datasheet	73 ns
f_s	Switching frequency	User defined	60 kHz

Table A.1: Variables used in loss calculation.

A.0.2 Inductor Losses

Inductor conduction loss can be calculated with (A.11) where R_L is given in the datasheet as 1.51 mΩ.

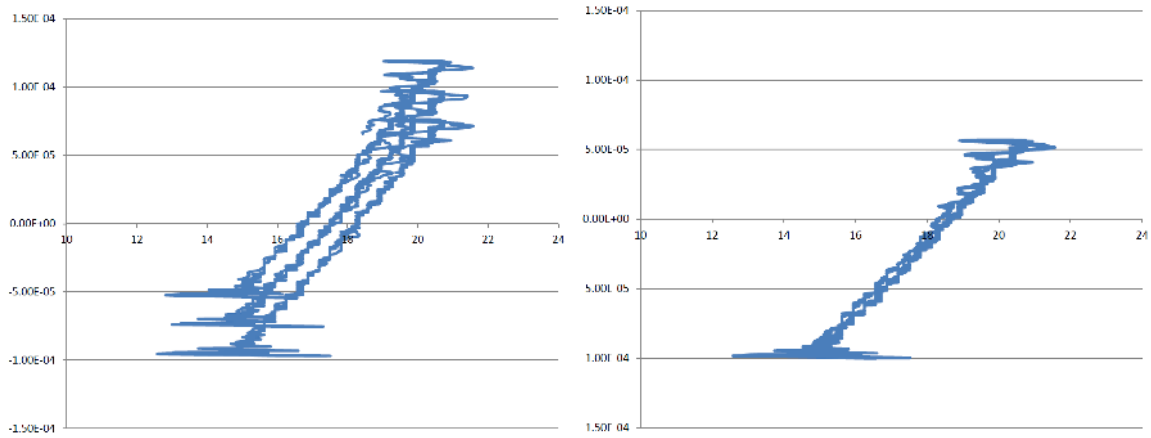
$$P_{L,cond} = R_L I_{L,rms}^2 \tag{A.11}$$

(A.12) is used to estimate the inductor magnetic core losses. Inductor voltage and current values are sampled and recorded over several switching periods. Differential flux linkage $d\lambda$ can be estimated by the difference equation in (A.13), and λ at each time step can be found by summing up the $\Delta\lambda$ values up to that time step.

$$P_{core} = f_s \int_{\lambda_0}^{\lambda_T s} i_L \, \mathrm{d}\lambda \tag{A.12}$$

$$\Delta\lambda = (t_n - t_{n-1}) \frac{v_n + v_{n-1}}{2} \tag{A.13}$$

A flux linkage-current plot is constructed to visualize the hysteresis loop. Because of the inductor serial resistance and measurement offset, the hysteresis loop might not coincide over several switching periods and an adjustment to the inductor voltage measurements need to be made to account for the dc offsets. An accurate adjustment to the voltage measurement at each time step can be made by subtracting a voltage related by a pseudo-inductor resistance and the current measurement. The pseudo-inductor resistance is modified iteratively from the specified inductor resistance until the hysteresis loops overlaps with one another over several switching periods. Fig. A.2 compares the hysteresis loop without and with voltage adjustment.



(a) (b)

Figure A.2: (a) Flux linkage and inductor current plot for duty cyle of 80% with no voltage adjustment. (b) Flux linkage and inductor current plot with voltage adjustment.

Once we are satisfied that an accurate estimation of λ is found, the inductor magnetic loss can be computed with discretized (A.12). Fig. A.3 shows the magnetic loss as a function of load current. It can be seen that in regions where the average current is greater than the peak inductor current, the magnetic loss is relatively constant. However, the estimation method used to calculate magnetic loss becomes inaccurate for low load current and produces very large core loss values. This discrepancy might have been caused by integration over an imperfect hysteresis loop where the ringing of the inductor voltage and current make graphical determination of a closed hysteresis loop very difficult. For

the simplicity of estimation, an average value of magnetic core loss in the acceptable region is calculated for each duty cycle and summarized in Table A.2.

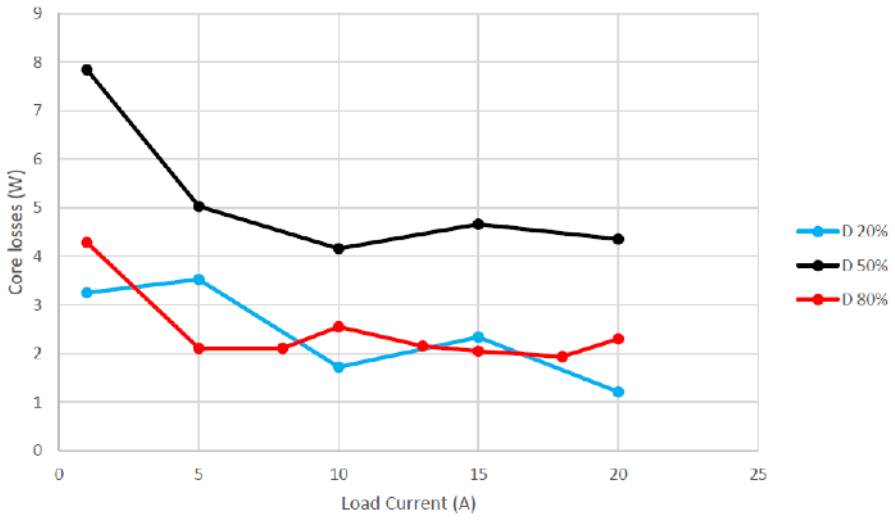


Figure A.3: Magnetic losses and load current plot for various duty cycle ratios.

	D 20%	D 50%	D 80%
P_{core}	1.76 w	4.39 w	2.18 w

Table A.2: Magnetic losses for various duty cycles.

A.0.3 Circuit Conduction Losses

Circuit conduction losses can be calculated with (A.14), where R_c is a lumped serial resistance that includes trace and connection resistance. In this converter design, optimal layout and heavy copper are used for the trace to minimize resistance. However, connections are made with copper washers and tightened with nuts and bolts. Consequently, it is expected that the connection resistance is the major contributor to the circuit resistive loss that is yet to be determined.

$$P_{circuit,cond} = R_c I_{L,rms}^2 \tag{A.14}$$

Because connection loss is difficult to measure directly, a micro-ohmmeter is used to measure the resistance of various numbers of connections, and the average resistance for a single connection is found to be approximately 1 mΩ. There is a total of 6 connection points in the buck converter prototype, resulting an estimated connection resistance of 6 mΩ.

A.0.4 Evaluation of the Loss Model

A single buck switching cell prototype is built with its input connected to a dc power supply and the output connected to a dc electronic load operating in constant current mode. The buck switching cell is controlled with an open duty cycle command that equals to 80%, and the output current or the average inductor current is adjusted by changing the current settings on the dc electronic load. Total power losses for various output current levels are measured by Yokogawa WT3000 high-precision power analyzer and compared against the total power losses predicted by the theoretical model as shown in Fig. A.4. It should be noted that in the theoretical power loss model, drain-source resistance R_{ds} is computed and adjusted for its temperature dependency according to the datasheet. The MOSFET temperature is recorded through a thermal camera.

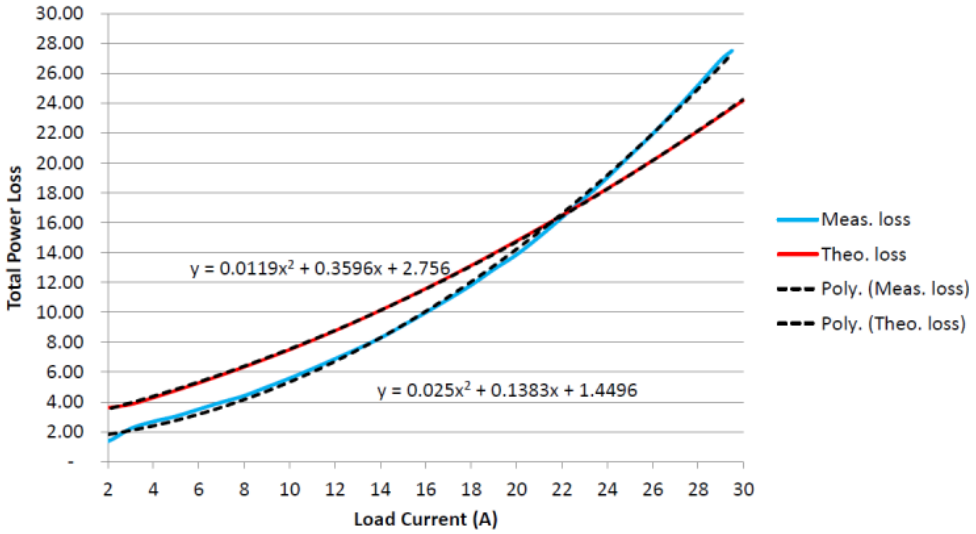


Figure A.4: Comparison of measured power loss of a single buck switching cell against the power loss calculated using the theoretical loss model for input voltages of 60 V and duty cycle equals that to 80%.

Trendline equations of second order polynomial show good fit to both the measured and calculated power loss. This is expected because for a fixed duty cycle command, switching frequency as well as relatively constant input and output voltages, converter conduction losses are related to the square of the current, and switching loss is linear to the current whereas the diode reverse recovery loss and the magnetic loss can be considered constant.

In order to relate the coefficients of the second order polynomial to parameters of the theoretical power loss model discussed in the previous sections, it is necessary to regroup

the power loss equations and express them in terms of average inductor currents. The RMS value of the inductor current $I_{L,rms}$ is related to the average inductor current I_L and peak inductor current ripple $\Delta i_{L,peak}$ through (A.15), where $\Delta i_{L,peak}$ is constant for a fixed duty cycle command.

$$I_{L,rms}^2 = I_L^2 + \frac{\Delta i_{L,peak}^2}{3} \tag{A.15}$$

Consequently, the relationship between power losses and I_L can be found in the following equations. (A.16) shows the loss terms that have second order relationship to the average inductor current, where (A.17) and (A.18) show the first order and constant terms, respectively. a, b, and c can be related to the trendline equation coefficients a_0, b_0, and c_0 by (A.19) to (A.21).

$$a(I_L^2 + \frac{\Delta i_{L,peak}^2}{3}) = P_{s1,cond} + P_{s1,cond} + P_{L,cond} + P_{circuit,cond} \tag{A.16}$$

$$b(I_L + \Delta i_{L,peak}) = P_{s1,on} + P_{s1,off} + P_{s2,on} + P_{s2,off} + P_{diode,cond} \tag{A.17}$$

$$c = P_{rr} + P_{core} \tag{A.18}$$

$$a = a_0 \tag{A.19}$$

$$b = b_0 \tag{A.20}$$

$$c = c_0 - a\frac{\Delta i_{L,peak}^2}{3} - b\Delta i_{L,peak} \tag{A.21}$$

The explicit expression of a and b can also be found from the theoretical power loss models as shown in (A.22) to (A.23). Consequently, trendline polynomial coefficients a_0, b_0, and c_0 can now be used to calculate parameters for the theoretical power loss models.

$$a = R_{ds} + R_L + R_c \tag{A.22}$$

$$b \approx \frac{1}{2}V_{block}(t_{ri} + t_{fu} + t_{ru} + t_{fi})f_s \tag{A.23}$$

Table A.3 compares key parameters used in the theoretical loss model and the same parameters calculated from the trendline coefficients.

	Circuit resistance	t_{ri}+t_{fi}+t_{ru}+t_{fu}	P_{rr}+P_{core}
Model value	6 mΩ	183 ns	2.88 w
Trendline calc.	19.7 mΩ	77 ns	1.58 w
Adjustment needed	+13.7 mΩ	2.4 times less	-1.3 w

Table A.3: Comparison of key parameters used in the theoretical loss model and the same parameters calculated from the trendline coefficients.

It can be seen in Table A.3 that the actual circuit resistance should be higher than the value of 6 mΩ used in the theoretical model. This is expected for the following reasons:

- Only resistance related to the circuit connections is measured and included in the theoretical loss model. Resistance related to the circuit trace is not included because it is difficult to determine accurately; and
- The dc resistance of the inductor shown in the datasheet is used in the theoretical model; however, the actual resistance could be higher due to skin effect and inductor construction.

On the other hand, a comparison between the loss curve trendlines indicates that the actual MOSFET switching time should be about 2.4 times less than the values used in the theoretical model. This is also expected due to the following reasons:

- t_{ri} and t_{fi} are difficult to measure, and as a result, the values in the datasheet are typically the values for the worst case scenario; and
- t_{ru} and t_{fu} are not given in the datasheet and thus measured using an oscilloscope. However, it is assumed in the model that the current rise and fall do not overlap with voltage rise and fall, which leads to an overestimated switching time.

Finally, the magnetic loss is also overestimated because:

- An accurate calculation of the magnetic loss requires an accurate alignment of the hysteresis loop over several switching cycles, which can not be done precisely using a graphical method; and
- Ringing noises due to switching make hysteresis loop alignment difficult, especially for a very narrow loop.

In summary, the theoretical loss model provides an insight into converter power loss and loss distribution. Through the comparison between the theoretical and measured

power loss, it can be seen that graphical methods with curve fitting and coefficient matching are valuable tools to validate and improve the theoretical model to allow for a more accurate thermal design and help identify possible improvement in the construction of future prototypes.