A Bluetooth Radio in 0.18-μm CMOS

Paul van Zeijl, *Member, IEEE*, Jan-Wim Th. Eikenbroek, Peter-Paul Vervoort, Suma Setty, Jurjen Tangenberg, Gary Shipton, *Associate Member, IEEE*, Eric Kooistra, Ids C. Keekstra, Didier Belot, Klaas Visser, *Member, IEEE*, Erwin Bosma, and Stephan C. Blaakmeer, *Associate Member, IEEE*

***Abstract*—This paper describes the results of an implementation of a Bluetooth radio in a 0.18-μm CMOS process. A low-IF image-reject conversion architecture is used for the receiver. The transmitter uses direct IQ-upconversion. The VCO runs at 4.8–5.0 GHz, thus facilitating the generation of 0° and 90° signals for both the receiver and transmitter. By using an inductor-less LNA and the extensive use of mismatch simulations, the smallest silicon area for a Bluetooth radio implementation so far can be reached: 5.5 mm^2. The transceiver consumes 30 mA in receive mode and 35 mA in transmit mode from a 2.5 to 3.0-V power supply. As the radio operates on the same die as baseband and SW, the crosstalk-on-silicon is an important issue. This crosstalk problem was taken into consideration from the start of the project. Sensitivity was measured at −82 dBm.**

***Index Terms*—Bandpass filter, CMOS RF integrated circuits, fractional-N frequency synthesizer, low-noise amplifier, phase-locked loop, poly-phase filters, silicon crosstalk, system on chip (SOC).**

I. Introduction

THE BLUETOOTH standard [1] is now recognized as a standard for short-range data and voice transfer. Bluetooth uses the 2.4–2.5-GHz ISM band with a frequency hopping spread spectrum system using GFSK modulation. As Bluetooth was intended to replace wired peripherals, the standard was defined and written such that low-cost implementation (i.e., in CMOS) is feasible.

Presentations at the ISSCC2001 [2] and ISSCC2002 [3] showed a number of solutions in 0.5-μm BiCMOS and 0.35- and 0.25-μm CMOS. The ASICs presented in these papers require a large silicon area and/or have a relatively high power consumption. This paper describes the radio part of a Bluetooth single-chip ASIC (both radio and baseband/SW are integrated on the same die) in 0.18-μm CMOS, which has a lower current consumption and smaller silicon-area compared to the radios in 0.35- and 0.25-μm CMOS technology.

As our radio has to be functional and realize sufficient sensitivity in the presence of the complete digital baseband and SW (i.e., the baseband hardware, and the SW are in RAM and ROM on the same die) running at its clock frequency, crosstalk from the digital part of the ASIC to the analog part of the ASIC is a significant problem. Our approach to this problem resulted in a (measured) sensitivity of −82 dBm.

Section II presents the architecture used in our single-chip Bluetooth ASIC. Section III discusses the inductor-less LNA. Section IV describes the implemented VCO. Section V discusses the implemented bandpass filter. Section VI discusses the centering of the bandpass filter in mass production. Our approach for analyzing the crosstalk-on-silicon problem is detailed in Section VII. Section VIII discusses miscellaneous issues, while Section IX concludes this paper with a summary and comparison with previous work.

II. The Radio Architecture

Fig. 1 shows the block diagram of the radio part of the single-chip Bluetooth ASIC. The heterodyne receiver uses an active poly-phase filter [4], [5] at a low IF. The lower the IF, the lower the Q of the bandpass filter and the lower the power consumption. However, for a low IF, the $1/f$-noise may become dominant. The IF was chosen to be 2 MHz as the best compromise between the $1/f$-noise and the Q-factor of the bandpass filter. The output signal of the bandpass filter is fed to a limiter and then demodulated. A limiter receiver is used in this architecture, as opposed to a linear receiver to avoid long automatic gain control (AGC) settling times. The strength of the received signal (RSSI) is AD-converted and together with the demodulated signal (RX-data) is supplied to the baseband part of the chip.

The reference voltage for the bandpass filter (and all other filters on silicon) is generated by an autotuner circuit in a master–slave configuration. The autotuner is realized as a phase-locked loop (PLL) coupled to the crystal-oscillator frequency, whereby the VCO in the autotuner is a replica of the gmC stages used in all filters.

The local-oscillator signals for the receiver and transmitter are derived from a voltage-controlled oscillator (VCO) running at 4.8–5.0 GHz. This enables the use of smaller on-chip inductors (and thus a smaller silicon area) with a higher Q, while the Q of the varactors does not significantly influence the oscillator performance. A divide-by-2 circuit generates the required quadrature signals for the RX and TX mixers. The PLL incorporates a delta–sigma modulator in the divider block to enable locking to all Bluetooth channels, for any crystal oscillator frequency between 10 and 40 MHz. The loopfilter of the PLL is off-chip as the cost of the five discrete Rs and Cs is below 5 cents and therefore not worth integrating.

The crystal-oscillator is a fully balanced circuit. It can be trimmed on-frequency by means of two 7-b arrays of capacitors that can be switched in parallel with the crystal. In the case

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P. van Zeijl, J.-W. Th. Eikenbroek, P.-P. Vervoort, J. Tangenberg, E. Kooistra, I. C. Keekstra, K. Visser, E. Bosma, and S. C. Blaakmeer are with the Bluetooth Technology Licensing Department, Ericsson Eurolab Netherlands, 7814 VA Emmen, The Netherlands (e-mail: Paul.van.Zeijl@eln.ericsson.se).

S. Setty and G. Shipton are with Ericsson Microelectronics, Swindon, SN5 7UN U.K.

D. Belot is with STMicroelectronics, F-38926 Crolles Cedex, France.

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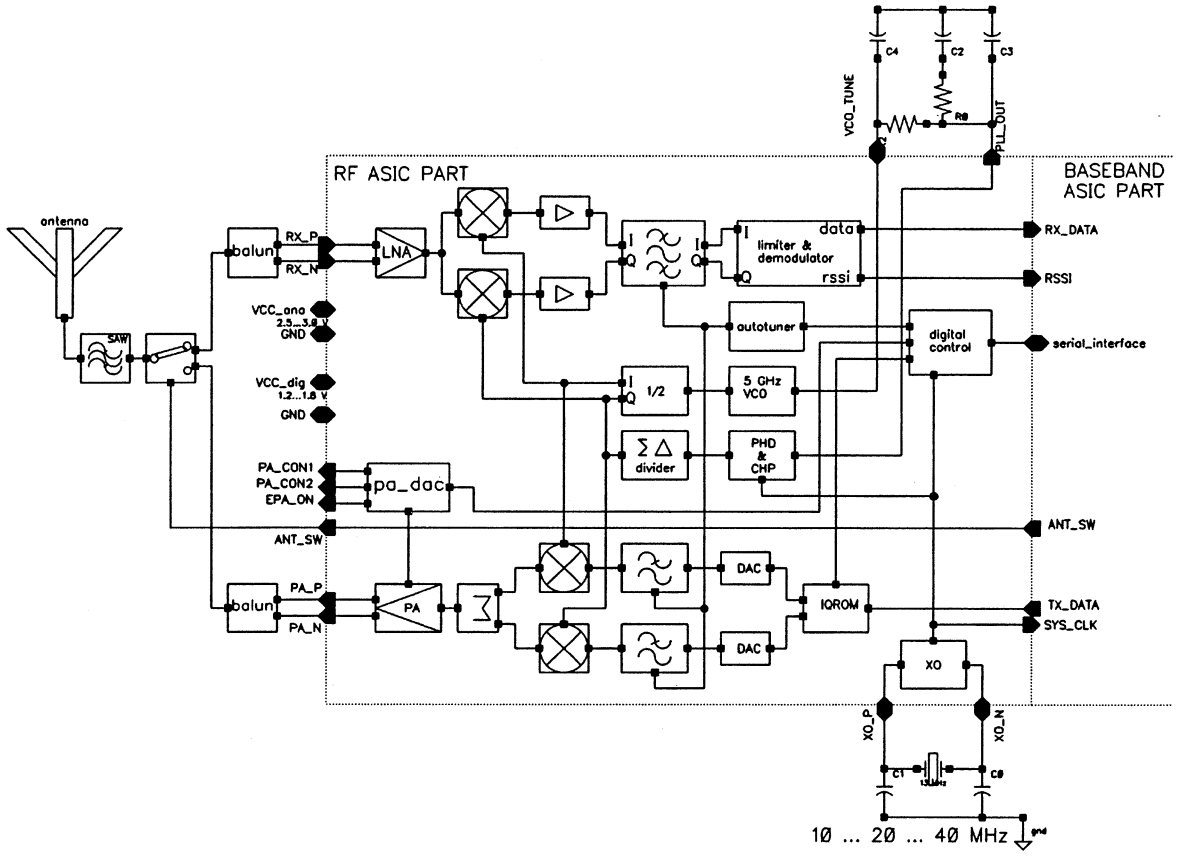

Fig. 1. Block diagram of the radio part of the ASIC.

that a crystal reference is already available in the application, (i.e., 13 MHz in GSM), such a signal can be injected into the XO_P pin.

The transmitter uses IQ-ROM modulation. The low-frequency I- and Q-signals are generated from the TX-data by a ROM and fed to two DA converters. The DA-converter signals are lowpass filtered and then upconverted to 2.4–2.5 GHz. An on-chip PA amplifies the signal to +4 dBm to the ASIC pins in a balanced output. The output power may be controlled in eight steps in order to save power and limit interference to other users.

The ASIC is prepared for Bluetooth Class 1 usage (i.e., +20 dBm output power): an off-chip PA can be used to amplify the on-chip generated +4 dBm to +20 dBm at the antenna. The power level of such an off-chip PA can be controlled by the pa-dac block.

The RF/radio ASIC contains an LNA, a PA, 3 VCOs, five bandgaps, eight regulators, two PLLs, two ADCs, seven DACs, three divider-chains, and a digital radio block including a delta–sigma modulator. Multiple bytes in the digital radio block are used for programming various functions in the radio, ranging from programming the synthesizer to setting various test modes. An on-chip multiplexer routes several on-chip signals to testpins to improve visibility and testability. The digital radio block is designed and (automatically) layed out as RF/radio part of the chip because of the close connection/cooperation with all analog blocks. The supply voltage for the RF/radio circuits is 2.5–3.0 V, except for the digital radio block, which runs at 1.8 V.

The digital circuits on the ASIC outside the RF/radio part are: the microprocessor, various UARTs, I2C, RAM, ROM, general purpose I/Os, and timers. These digital blocks all run from 1.8 V as in applications like cellular phones, and, like cellular phones, both the 1.8-V and the 2.5–3.0-V power supply voltage are available. Level-shifter circuits take care of the transfer of signals from 1.8 V from/to 2.5–3.0 V. At the start of the project, the serial interface between the digital part of the ASIC and the RF/radio part was defined. During the design, we had several meetings to discuss the floorplan of the ASIC. The design of the RF/radio part and the digital circuits was done independently and later on combined on a GDS2 layout level.

III. The LNA

Fig. 2 shows the schematic of the LNA: the LNA consists of a differential NMOS pair (M0–M1) with resistive loads R_{la} and R_{lb}. The drain–gate feedback resistors R_{fa} and R_{fb} together with the g_m of the differential pair and the load resistances determine the input impedance [6]. The voltage gain A_v and the input impedance Z_i of the LNA are given by

$$A_v = \frac{-R_l * (g_m R_f - 1)}{R_l + R_f}$$

$$Z_i = \frac{2 * R_f}{1 - A_v}.$$

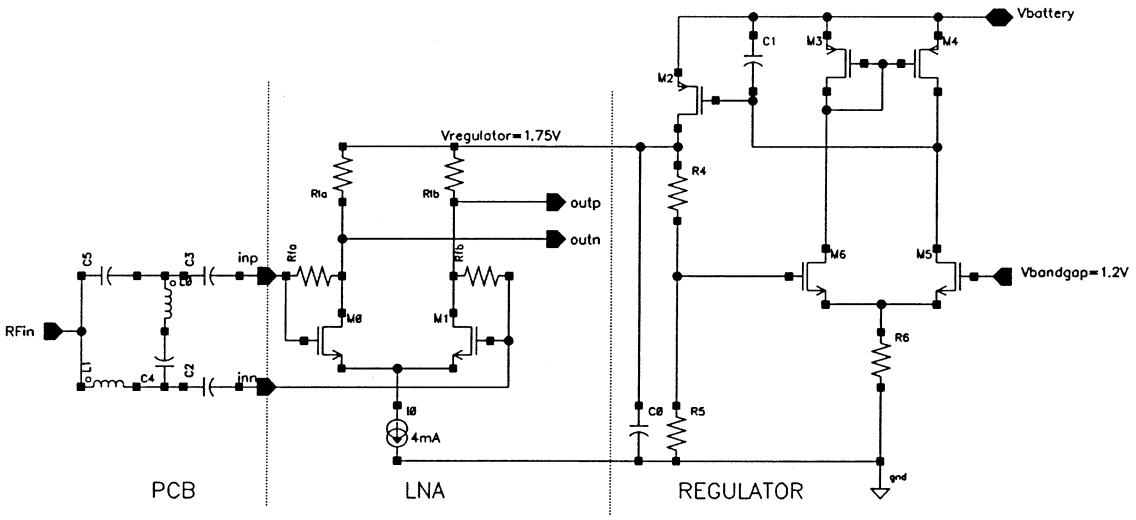

Fig. 2. The LNA and regulator schematic.

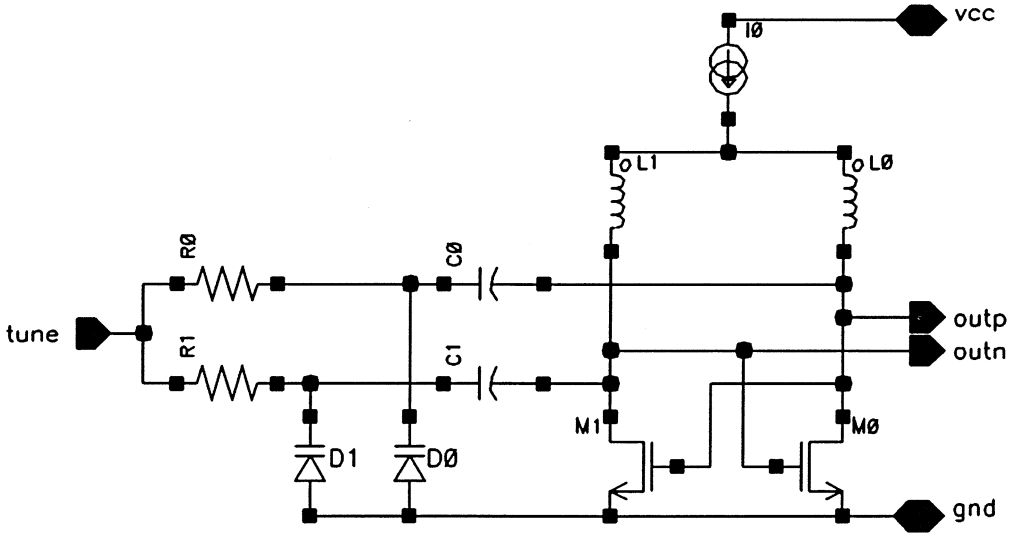

Fig. 3. VCO schematic.

The LNA does not use inductors in order to save silicon area. The balun transforms the 50 Ω on the PCB to 150 Ω on the ASIC resulting in a noise figure of 3.5 dB at 2.5 GHz. The third-order intermodulation intercept point is -5 dBm, while the 1-dB compression level is -15 dBm (referred to the input). This LNA performance can only be reached by using devices with a minimum length of 0.18 μm for M0–M1. However, the maximum voltage of these devices is limited to 1.9 V for a product lifetime of ten years. As the customer requirement for the supply voltage is 2.5–3.0 V, we used regulators to derive an on-chip regulated voltage of 1.75 V. The process supports a second oxide thickness, which is needed for the interface to off-chip digital circuitry anyway. The devices using this thick oxide have a minimum length of 0.36 μm and a maximum voltage of 3.6 V. The schematic of the voltage regulator is also drawn in Fig. 2, using thick-oxide devices M2–M6. Resistors R4–R5 determine the voltage gain of the regulator, in this case $1.75/1.2 = 1.46$. Capacitors C0–C1 are added for stability reasons. An advantage of the regulator is that it isolates the LNA from any interference on the power supply lines. The LNA voltage regulator is also used for the mixers in the receiver front-end. For other circuits on the ASIC (i.e., high-frequency prescalers, LO-bufer stages, mixers, PA–RF circuits) that benefit from the performance of the thin-oxide devices, similar voltage regulator circuits are implemented.

IV. VCO

Fig. 3 shows the schematic of the VCO. It consists of two cross-coupled NMOS devices M_0–M_1 realizing the negative resistance, together with the inductors L0–L1, capacitors C0–C1, and varactors D0–D1. The inductors are made in (standard) extra thick metal 5 and metal 6 and reach a Q of 10 at 5 GHz. Diode varactors with a high Q ($>$50 at 5 GHz) are used for tuning. Biasing is done by current source I_0 on top of the oscillator. As the power supply sensitivity is still very high (on the order of some MHz/V), a regulator is implemented. The measured phase noise is -122 dBc/Hz at a 3-MHz offset frequency.

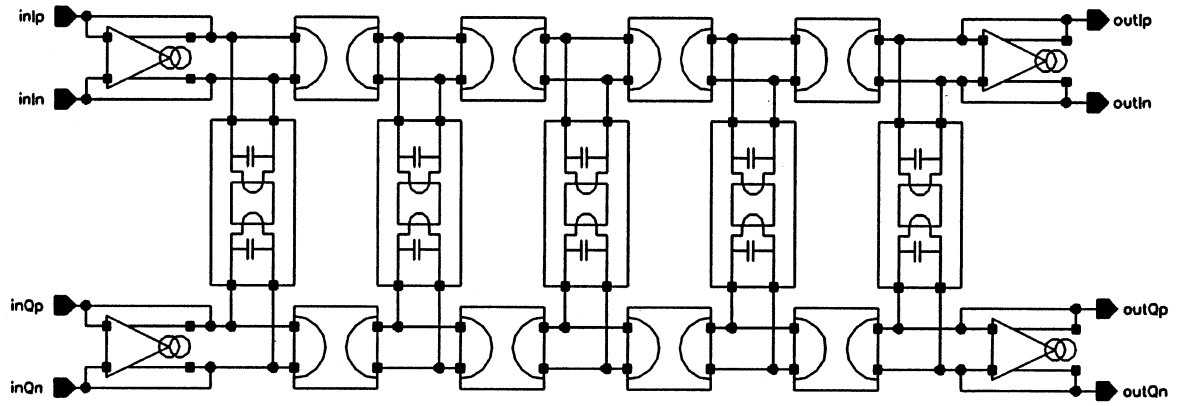

Fig. 4. The overall schematic of the poly-phase bandpass filter.

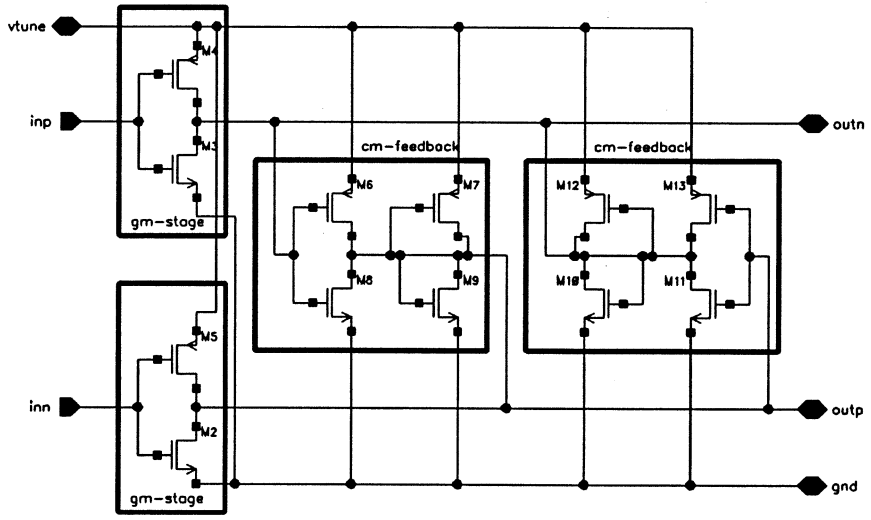

Fig. 5. The basic g_mC-cell.

An array of capacitances can be switched in parallel with the transistors to trim the VCO on-frequency in the case of process spread. Programming has to be done in the application.

V. Receive Bandpass Filter

The selectivity filter is a fifth-order Butterworth filter with a 1-MHz bandwidth. The active poly-phase filter [4], [5] consists of four terminations of $1/g_m$ at the I- and Q-inputs and at the I- and Q-outputs (see Fig. 4). The five resonators (consisting of a gyrator with capacitive loads at the I- and Q-side) are connected between the I- and Q-channel. Gyrators in the forward I- and Q-paths isolate the resonators from each other.

Fig. 5 shows the basic g_mC-cell used in the active poly-phase filter. It consists of inverter stages as presented in [7]. The local power supply voltage of all these inverters determines the filter center frequency and is coupled to the reference voltage generated by the autotuner. This inherently decouples the local supply voltage from the battery, thereby increasing power-supply rejection.

The g_m-value of this g_mC-cell is determined by the g_m of the NMOS and PMOS of the inverters (denoted as "gm-stage" in Fig. 5). Two common-mode feedback stages (denoted as "cm-feedback" in Fig. 5) are present to fix the common-mode level at the outputs outp-outn. The filter capacitance C is determined by the sum of all MOS capacitances in this cell. Consequently, the width and length of the devices are chosen such that both the required g_m and the filter capacitance C are realized (see [8]). As large device lengths are needed to realize this, the f_T of the devices is reduced significantly, down to five to ten times the filter center frequency. Consequently, the gate-channel nonquasi-static effect, as modeled by the $nqsmod$-parameter in the BSIM3V3.2 model, is very important in order to design such a filter with a flat passband and prevent it from oscillating.

Fig. 6 shows the measured transfer of the filter. The bandwidth of the filter is 1 MHz centered at 2 MHz. As you can see, the passband is very flat, indicating no parasitic effects. The out-of-band rejection is better than 70 dB, also indicating no spurious responses and/or oscillations of the filter. This filter, together with a specially designed driving amplifier, outperforms the Bluetooth distortion and adjacent channel intermodulation specifications.

Fig. 7 shows the measured receiver selectivity from two samples, together with the Bluetooth specification. The "hump" that appears at a channel offset of -4 MHz is actually the image channel in our low-IF receiver. It is clear that the Bluetooth requirements are fulfilled.

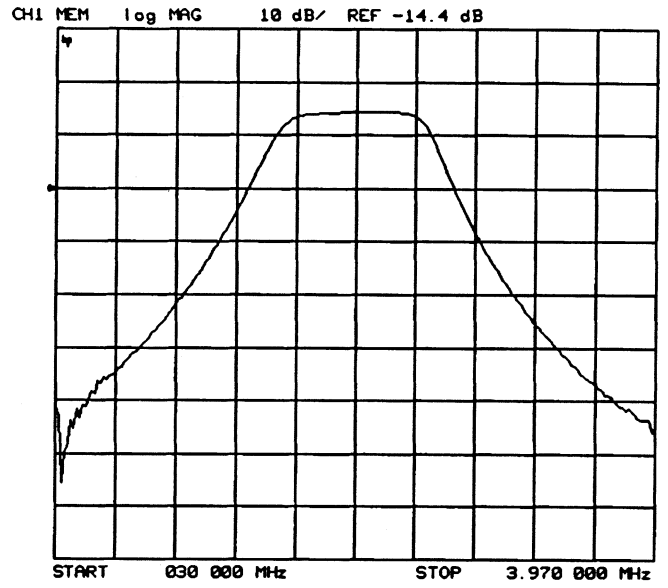

Fig. 6. The measured bandpass filter transfer.

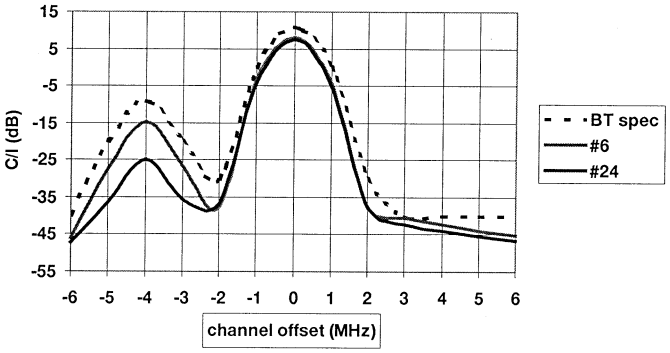

Fig. 7. The measured receiver selectivity.

VI. Autotuner

Fig. 8 shows the block diagram of the autotuner. It consists of a phase-frequency detector (PHD), a lowpass filter, a VCO, and a divider ($1/N$). The VCO uses the same basic g_mC-cell as in the bandpass filter (see Fig. 5). The PLL then takes care that the divided VCO signal is exactly synchronized with the crystal frequency. As the VCO tune voltage is copied to act as a tune voltage for the bandpass filter (and all other filters on silicon), the bandpass filter will also be centered. Only mismatch between the g_mC-cell in the VCO and the g_mC-cell in the bandpass filter will give rise to the bandpass filter being off-center.

Mismatch can have a huge impact on silicon area, as mismatch scales inversely proportional with the square root of the area of the devices [9]. Thus, for instance, if the mismatch is a factor of two too large, the area has to be increased by a factor of four! Mismatch information on low-frequency effects, i.e., mismatch in resistance for resistors, mismatch in capacitance for capacitors, and mismatch in threshold voltage and transconductance of MOS devices, must therefore be available and implemented in the Process Design Kit in order to optimize silicon area.

In the case of our autotuner, this is not enough. As the VCO in the autotuner and the bandpass filters use the same g_mC-stages

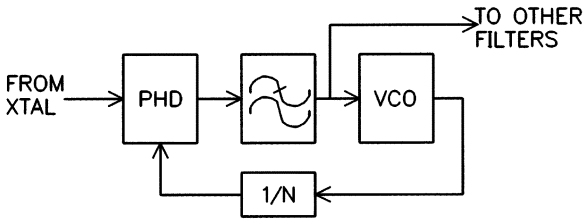

Fig. 8. Block diagram of the autotuner.

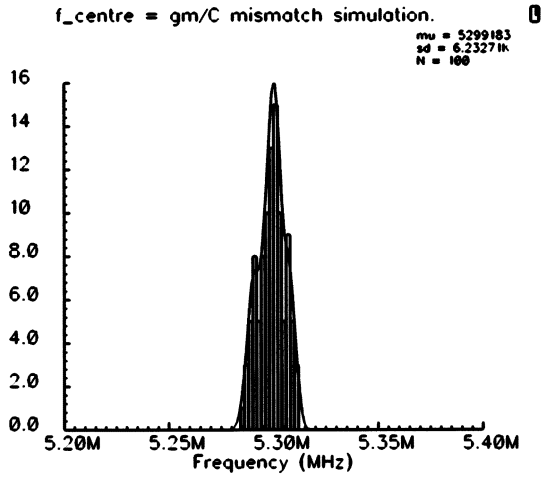

Fig. 9. The result of a Monte-Carlo simulation on the g_mC resonator center frequency.

(see Fig. 5), the mismatch in MOS capacitance becomes very important. This mismatch has to be known and implemented in the Process Design Kit in order to simulate the mismatch between the center frequency in the VCO and the center frequency of the bandpass filter in this master–slave configuration. Fig. 9 shows an example of a simulation result of the autotuner-VCO. As can be seen from the simulation results in Figs. 9 and 4, the standard deviation on filter center frequency is on the order of 6 kHz (i.e., $3\sigma = 18$ kHz, which has been confirmed by measurements), which is low enough not to become a performance problem in mass production.

VII. Silicon Crosstalk

A problem with the design of a single-chip radio-baseband-software ASIC is crosstalk. Crosstalk may be caused by crosstalk on the PCB, crosstalk via the bonding wires and package, crosstalk via ground and supply lines and crosstalk due to the silicon substrate. The main issue of this crosstalk problem is that we do not have ways to easily predict the effects (magnitude) of the crosstalk. PCBs, packages, and ground and supply-line series resistances have to be modeled, thus increasing the complexity of the design and thus simulation time.

The interfering signals can have consequences dominated by either linear or nonlinear behavior. Nonlinear crosstalk may create modulation of signals (FM/AM, and thus create extra spurious components) or shifts bias points and gives pushing and/or pulling effects on oscillators like a VCO or a crystal oscillator.

Silicon crosstalk (or in general any crosstalk) can be minimized by separation of the desired signal and the interfering signal in the frequency domain (this may prove difficult due to high data rates), separation in the time domain (no digital activity during reception/transmission of signals), or by lowering the interference source (introduce jitter on clocks) and/or isolation (use extra layout measures such as shielding or triple-well), or compensation and balancing. But how much does this improve our design? The answer to this question should be found early in the design, otherwise the ASIC may fail type approval and/or mass production in the end.

The most important aspect in the discussion on silicon crosstalk is that the number of gates in the digital part of the chip is so large (>1 M) that it is not practical to include them all in analog simulations. The fast slopes of digital signals in a 0.18-μm process generate harmonics in the gigahertz range, even when the digital part is only clocked at $10 \cdots 40$ MHz. If software is present in on-chip ROM, the exact behavior will be unpredictable.

State-of-the-art tools allow modeling of the substrate crosstalk after the layout has been finalized but investigating a completely layed out chip is very time consuming; most probably even longer than silicon processing itself. Sometimes, the modeling only starts after receiving first silicon, because there are "problems." On top of that, designers still consider the substrate crosstalk as "black magic." Our strategy was to start dealing with this problem during the design phase of the project.

The digital blocks (and also the memory access) on the ASIC were modeled in terms of power supply voltage, current consumption, frequency, and their behavior since the signals in these block behave either like clocked signals or more like pseudorandom-bit (PRB) sequence signals. Then, a simple effective large inverter with the same performance (i.e., the same current consumption) was used as a replacement for this large digital block. As an example, we model two digital blocks: the microprocessor and the RAM. The micro-processor consist of 75 kgates, runs at 10 MHz, and consumes 5 mA at $Vcc = 1.5$ V. The microprocessor is similar to a purely clocked block. We replace this complete block by a single large inverter which is 70.000 times larger than the minimum-sized inverter in our 0.18-μm CMOS process. The RAM consist of 256 kb, is accessed with a clock of 5 MHz, and consumes 6 mA at $Vcc = 1.5$ V. The RAM is accessed in a pseudorandom manner. We replace this RAM by a single large inverter which is 600 000 times larger than the minimum-sized inverter in our 0.18-μm CMOS process. The combination of both blocks (or even more blocks) can now be used in a silicon-crosstalk simulation.

At the start of the project, only a floorplan of the ASIC was available (see Fig. 10). We used this floorplan together with the program SubstrateStorm [10] to generate an RC-netlist as a model for the substrate. This RC-netlist was then used for silicon-crosstalk simulations.

The combination of the digital effective inverters, the substrate netlist, and the sensitive analog circuitry, like the LNA and VCO, were then simulated. Effects of the digital interference on the analog circuitry were then minimized or gave rise to specifications on the analog blocks. See [11], [12] for more details on the procedure.

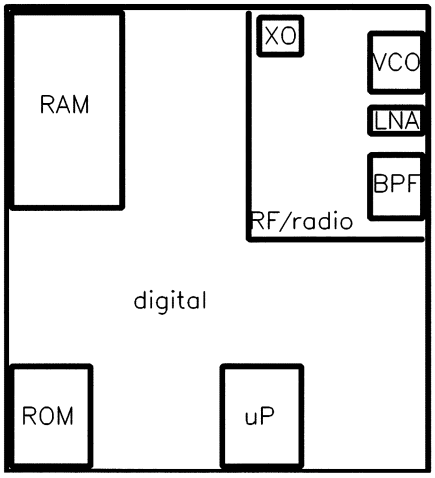

Fig. 10. The floorplan of the single-chip ASIC.

In the case of our single-chip Bluetooth ASIC, several measures were taken for minimizing the crosstalk: in the layout, a specially designed P-type wall isolates the radio from the baseband (also see [13]). This wall is approximately 300 μm wide and has multiple bumps to the ball-grid-array (BGA) package such that all digital interference traveling to the analog part are picked up and shorted to the ground connection in the package. The area consumed by this isolation wall is 1.4 mm^2, which will be lowered significantly in future versions. The isolation provided by this wall is dependent on the number of ground connections from the wall to the package (or PCB) and the length of the wire to the package (or PCB). In our case, we use 13 bumps with a wire length below 1 mm (or an inductance below 1 nH) and then the wall gives us some 25 dB of isolation at 2.5 GHz. The isolation decreases 6 dB/octave for lower frequencies until it flattens out around 100 MHz. Isolation increases with distance, but, more importantly, it increases with the size of the blocks on either end, i.e., the size of the block that generates the interference and the size of the block that picks up the interference.

All sensitive circuits in the analog part of the ASIC are balanced and have high common-mode rejection and low common-mode to differential-mode conversion, such that interference on the sensitive nodes is minimal. Separate supplies (we use five supply domains in the digital part of the ASIC and five more in the RF/radio part of the ASIC) and the extensive use of power supply regulators increases the power-supply rejection of sensitive circuit like the LNA and the VCO such that interference that is present on the power supplies does not enter these circuits.

As stated in the previous section, high-frequency mismatch information was needed for the g_mC filter design and optimization. It was also needed for RF design, for example, the LNA in Fig. 2 in combination with the desire to realize a low common-mode to differential-mode conversion for minimizing silicon-crosstalk. As we are operating the LNA close to its

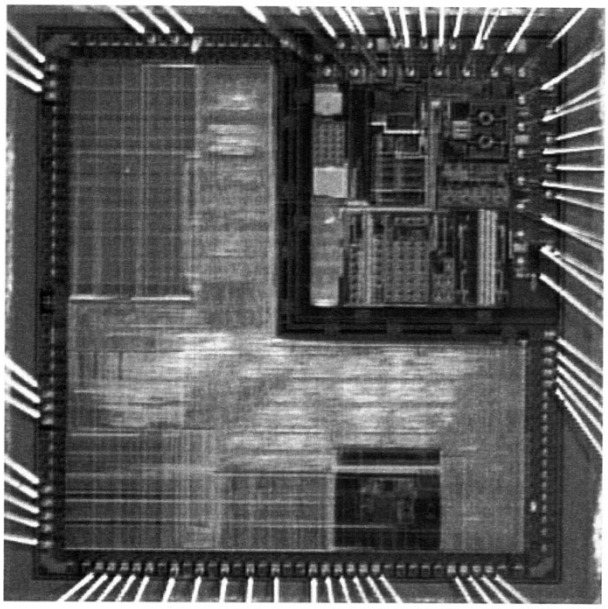

Fig. 11. Micrograph of the complete chip including digital.

−3-dB bandwidth, the parasitic capacitances in the load resistors, the feedback resistors and the MOS devices play a role in the common-mode to differential-mode conversion.

Of course, it is not sufficient to only solve silicon-crosstalk, other crosstalk issues (PCB, package, power decoupling) have to be solved as well. The measured sensitivity of the receiver, while Bluetooth reception is taking place (so the digital part is running), is −82 dBm.

VIII. Miscellaneous

The RFCMOS8 process with dual oxide thickness (3.2 nm giving 0.18-μm devices and 7 nm giving 0.36-μm devices) was used. Two extra masks realize a high-Q metal–metal capacitor and a buried-N-layer, thus giving the possibility of isolating the MOS devices from the substrate.

Fig. 11 shows a photograph of the ASIC. The radio part of the ASIC is in the right-hand upper corner: it occupies 5.5 mm^2 including pads (4.0 mm^2 excluding pads). The photograph was taken on a bonded version of the ASIC in a CQFP80 package. We used this package for debugging and functionality tests. For production, the ASIC will be flip-chip mounted on a BGA. All ASIC pins fulfill 2-kV (human-body model) ESD protection, including the RF pins.

Fig. 12 shows a plot of the measured RSSI value versus input power. The RSSI value is monotonic and has a range from −70 to −30 dBm. It fulfills Bluetooth specifications.

The power consumption in various Bluetooth modes [1] is very low due to averaging: the receiver, transmitter, and synthesizer are not continuously ON. For instance, in the HV1-mode, the radio is in receive (transmit) for 30% (30%) of the time. The synthesizer is switched on well in advance of a receive or transmit slot in order to lock the PLL. The resulting averaged current consumption is then 23 mA for the HV1-mode, 9 mA for the HV3-mode, and 0.3 mA for the PAGE-SCAN-mode, as shown in Fig. 13.

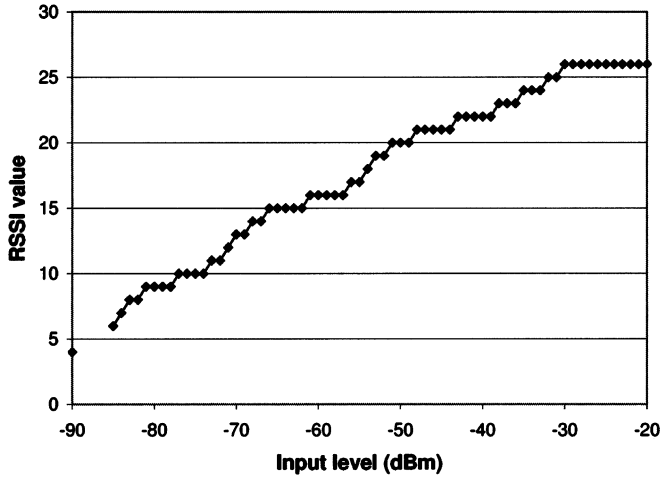

Fig. 12. Average current consumption.

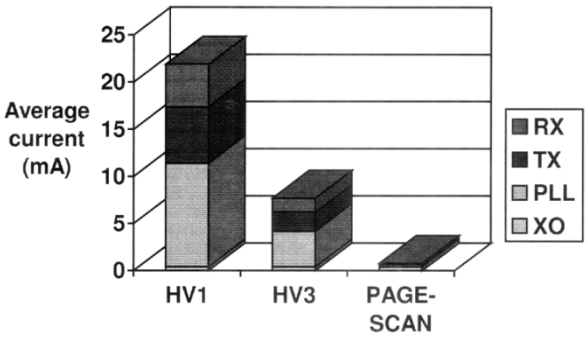

Fig. 13. Measured RSSI versus input power.

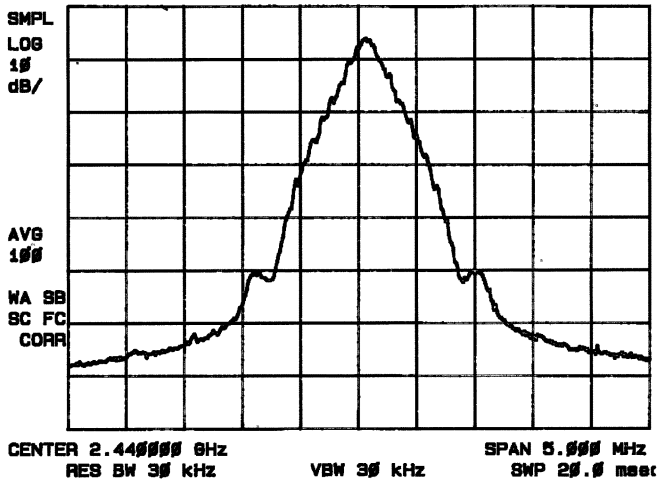

Fig. 14. Transmitter output spectrum.

The transmitter output spectrum with a pseudorandom data signal supplied to the transmit-IQROM is shown in Fig. 14. The spectrum is quite close to the ideal Bluetooth transmit spectrum.

Table I shows a performance summary. The most important Bluetooth specifications are reached. First data transmissions between this Bluetooth ASIC and other Bluetooth radios have already taken place.

Table II shows a comparison between papers presented at ISSCC 2001 [2] and ISSCC 2002 [3] and our work. Our radio

TABLE I
PERFORMANCE SUMMARY

Parameter	Bluetooth specification	Measured
Sensitivity (BER=10^{-3})	-70 dBm	-82 dBm
IP_3	-21 dBm	-14 dBm
maximum usable input level	-20 dBm	0 dBm
RSSI range	-60 to -40 dBm	-70 to -30 dBm
CNR (Δf=3 MHz)	-121 dBc/Hz	-122 dBc/Hz
Channel switching	200 μs	80 μs

TABLE II
COMPARISON TO PREVIOUS WORK

	Technology	silicon-area (mm^2)	Icc_RX (mA)	Icc_TX (mA)	Vcc (V)
TEL (RF + BB) '2001-13.1	0.25 μm CMOS	40	41	52	2.5
OKI (RF) '2001-13.2	0.35 μm CMOS	18	66	47	2.7-3.3
om (RF) '2001-13.3	0.35 μm CMOS	20?	46	47	2.7-3.3
ant (RF) '2001-13.4	0.5 μm SiGE BiCMOS	12?	16	12	1.6-3.0
ı Wave (RF) '2002-5.1	0.35 μm SOI BiCMOS	19.5	39	37	2.7
lica (RF) '2002-5.3	0.25 μm CMOS	13.3	45	36	3.0
i (RF) '2002-5.5	0.35 μm BiCMOS	11.2	45	35	2.7
ork (RF) '2002-5.1	0.18μm CMOS	5.5 (4.0)	30	35	2.5-3.0

is 2–4 times smaller compared to the IME/OKI, Broadcom, Conexant, Silicon Wave, Trancilica, and Hitachi radios. The RX part of our radio consumes 30%–50% less current compared to the solutions in 0.35- and 0.25-μm CMOS. Only the SiGe BiCMOS solution from Conexant has a lower power consumption.

IX. CONCLUSION

We reported the RF part of a single-chip Bluetooth ASIC. The direct upconversion transmitter uses 35 mA, while the receiver consumes 30 mA from the 2.5–3.0-V power supply. An active poly-phase bandpass filter realizes the channel selection. An autotuner automatically centers the bandpass filter independent of process corners, power supply voltage, or temperature. The modeling of mismatch, especially the mismatch in MOS capacitance, is essential in realizing a high yield in mass production. Our approach to silicon crosstalk resulted in a (measured) sensitivity of -82 dBm. This transceiver is the smallest integrated CMOS Bluetooth radio so far.

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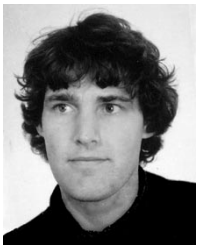

Paul van Zeijl (M'91) received the M.S. degree from the Delft University of Technology, Delft, The Netherlands, in 1985 and the Ph.D. degree in 1990 for the study toward a fully integrated FM Upconversion Receiver Front-end with on-chip SAW filters.

He was awarded the "VEDER PRIJS" for his contribution to the successful integration of radio circuitry in 1991. From 1991 to 1997, he worked for Ericsson Business Mobile Networks, Enschede, The Netherlands. From 1997 onward, he has worked for Ericsson Eurolab Netherlands, Emmen, The Netherlands. From 1991 to 1997, he worked on the standardization of DECT cordless telephones and on the realization of integrated circuits for DECT. From 1997 onward, he worked on integration of radio and single-chip ASICs for paging and Bluetooth in CMOS technology. He is a Senior Specialist in radio ASIC integration since 2000. His interests are analog, radio, and RF integrated circuits in bipolar and CMOS technologies. He has written several technical papers and holds several patents.

Jan-Wim Th. Eikenbroek was born in Delft, The Netherlands, in 1957. He received the M.S. degree in electrical engineering and the Ph.D. degree from the University of Delft, Delft, The Netherlands, in 1984 and 1989, respectively. His master's thesis was on the subject of bipolar translinear circuits, and his dissertation was on the subject of an integrated AM short-wave upconversion receiver front-end.

In 1989, he joined Ericsson Eurolab Netherlands, Emmen, The Netherlands, where he designed low-power radio front-ends for paging receivers. Currently, he is a Senior Specialist in radio system design and involved in the development of future extensions of the Bluetooth standard. His main research interests are in the field of RF radio-system design and synthesizers.

Peter-Paul Vervoort was born in Vlaardingen, The Netherlands, in 1968. He received the M.S. degree in electronics from the University of Twente, Enschede, The Netherlands, in 1994.

Since 1995, he has been working for Ericsson Eurolab Netherlands, Emmen, The Netherlands, on integrated analog radio circuits for application in paging and Bluetooth in CMOS technology. His interests are in RF and low-frequency analog circuits and systems in CMOS technology.

Suma Setty received the M.Eng. degree in electrical/electronic engineering from Imperial College of Science and Technology, London University, London, U.K., in 1993.

She worked as a Research Assistant in the Department of Electrical/Electronic Engineering of Imperial College from October 1993 to October 1997, initially in the area of analog design automation and later in the area of CMOS analog circuit design. Since February 1998, she has been employed at Ericsson Microelectronics, Swindon, U.K., and is working in the area of analog/RF ASIC design for wireless applications.

Jurjen Tangenberg received the B.E. degree in electronics engineering from Rens & Rens polytechnical school, Hilversum, The Netherlands, in 1995 and the M.S. degree in electronics engineering from the University of Twente, Enschede, The Netherlands, in 1998.

Since 1998, he has been with Ericsson Eurolab Netherlands, Emmen, The Netherlands. His interests are high-frequency CMOS circuits like VCO, LO-buffers, and divider circuits.

Gary Shipton (A'91) received the B.Sc. degree in electrical and electronic engineering from the University of London, Queen Mary College, London, U.K., in 1978.

He first worked for Plessey Telecommunications on high-speed multiplexing equipment and later with STMicroelectronics designing mixed-signal ICs for consumer applications. Since joining Ericsson Microelectronics, Swindon, U.K., in 1997, he has worked on high-level modeling and circuit design for mixed-signal ICs used in telephony codecs and Bluetooth. He has also been a member of a specialist group involved in the specification and development of Bluetooth2.

Eric Kooistra was born in Sneek, The Netherlands, on September 25, 1967. He studied electrical engineering at the University of Twente and graduated in 1991. In 1995, he completed the two year post-masters program Information and Communication Technology at the Eindhoven University of Technology.

Since 1995, he has worked at Ericsson Eurolab Netherlands, Emmen, The Netherlands. His technical interests are the design and implementation of digital signal processing functionality for radio ASICs.

Ids C. Keekstra was born in Engwierum, The Netherlands, on August 7, 1967. He received the B.S. degree in electronic engineering from the Technical College, Leeuwarden, The Netherlands, in 1990.

In 1993, he joined ICT Deventer as an automation engineer. In 1996, he joined Philips Consumer Electronics, Eindhoven, The Netherlands, where he was involved in the field of audio and video amplifiers and high-resolution A/D converters. In 2000, he joined Ericsson Eurolab Netherlands, Emmen, The Netherlands, where he is involved in the design of analog integrated RF circuits.

Didier Belot received the D.U.T Electronique degree from the Institute Universitaire de Technologie of Grenoble, Grenoble, France, in 1982, and the M.S. degree from the Ecole Nationale Superieure d'Electronique et de Radioelectricite de Grenoble, Grenoble, France, in 1991.

In 1983, he joined the Bipolar Device Characterization and Modelization Group, Thomson Semiconductor. In 1986, he joined Thomson "Etude et Fabrication de Circuits Integres Speciaux" where he was involved with digital CMOS design. In 1988, he was involved with the design of high-speed ECL/CML data communication ICs at STMicroelectronics, Crolles, France. In 1996, he moved to the Radio Frequency design. Presently he manages a group involved with the development of circuits for Mobile Phones and Local Network standards in Central Research and Development, STMicroelectronics.

Klaas Visser (M'92) received the M.S. degree in electronics engineering from the University of Twente, Enschede, The Netherlands in 1998.

He worked for the library technology group Advanced Memory Design center of Philips Semiconductors Eindhoven (LTG/AMDC), The Netherlands. He contributed to the development of embedded ROMS and SRAMS in a logical 0.25-μm CMOS process of Philips Semiconductors (C050). In 2001, he joined Ericsson Microelectronics, Emmen, The Netherlands. He is involved in the development of radio and single-chip ASICs for Bluetooth in several 0.18-μm CMOS technologies.

Erwin Bosma received the B.E. degree in electronics engineering from Hanzehogeschool, Groningen, The Netherlands, in 2000.

Since 2000, he has been working at Ericsson Eurolab Netherlands, Emmen, The Netherlands. His interests are high-frequency CMOS integrated circuits and Bluetooth systems.

Stephan C. Blaakmeer (S'00–A'01) was born in Stiens, The Netherlands, in 1976. He received the M.S. degree in electrical engineering from University of Twente, Enschede, The Netherlands, in 2001 on the subject of RF-CMOS ring oscillators.

Since 2001, he has been with Ericsson Eurolab Netherlands, Emmen, The Netherlands. He is involved in the development of radio ASICs for Bluetooth. His interests are in the field of RF and analog CMOS circuits.