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A Bootstrapped Switch for Precise Sampling of Inputs with Signal Range beyond Supply Voltage

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Abstract— **Bootstrapped switches are used in a variety of applications including DC-DC converters, pipelined analog-to-digital converters and high voltage switches and drivers. Current work on highly integrated power management applications often requires the ability to measure voltage quantities that exceed the supply voltage in magnitude. This is primarily due to a basic need to maximize efficiency by running the power management IC on as low supply voltage as possible, while still maintaining the ability to sample and measure quantities from the surroundings that could well exceed the battery voltage. In this paper a new bootstrapped switch is presented. The switch enables the precise sampling of input signals well greater than the chip supply voltage with no static power consumption, and without activating on-chip parasitic body diodes. The bootstrapped switch, presented here, is designed to sample an input signal with a 0-5.5 V range at a supply voltage of 2.75 V. Measurement data shows functionality for a 0-6 V input signal range with a supply voltage as low as 1.2 V.**

I. Introduction

Bootstrapping circuits are used in power management systems and analog-to-digital converters [1], [2], [3], [4]. In power management systems, DC-DC converters often employ bootstrapping techniques to drive the high-side (HSD) switch [5]: both high-side and low-side devices are often implemented with drain extended or DMOS N-channel transistors. The driving of the HSD switch requires using a voltage higher than the supply thus requiring the bootstrapping of the gate control. In ADCs, high-speed pipelines must sample the input signal within a very short time and must ensure an accurate charging of the sampling capacitor. The function is properly realized with bootstrapped switches that are used instead of complementary transistor switches. The result obtains a faster operation with smaller transistors and better-controlled clock-feedthrough.

Bootstrapped switches are highly effective in terms of power consumption and require no static current consumption to function. The power losses are only dynamic losses that occur during switching and are due to two contributions: the shoot-trough current that occurs when the logic gates controlling the switch's gate change their logic state, and the power required to charge and discharge capacitive nodes of the switch. The use of an effective switch with a small parasitic capacitance reduces both terms.

Recent power management solutions often integrate on the same chip multiple switched-mode regulators, multiple low-dropout regulators, voltage references, low-power low-speed SAR ADCs, digital control cores, and serial interface units. The solutions should be able to share resources (voltage references, current references, etc.) among different sections of the chip thus obtaining optimum power efficiency with low power losses during the sleep mode. Normally the shared resources require being active during the sleep or low power modes. The ADC is one of the shared resources and is typically a very low power component used to supervise and monitor on-chip and off-chip voltages. The architecture normally used is a multi-channel SAR ADC.

Advanced power management systems require proper operation maintaining all functionality with a wide range of supply battery voltages. Namely, the ADC is required to operate even with very low supply voltages and is also required to precisely measure off-chip voltages that can be significantly higher than the used on-chip supply. The above-described situation is challenging not only for the special techniques required for level-shifting of the high-voltage to be measured but also for the need to ensure that no on-chip parasitic diode is forward biased under any condition. Moreover, in order to have a proper sampling the switches must be turned on independent of the difference (sometimes positive) between input and supply voltage.

This paper presents a bootstrapped switch to be used for sampling input signals with a range exceeding the supply voltage [6]. The switch enables a precise input sampling without requiring extra power consumption. The proposed circuit is implemented using a conventional CMOS technology and does not require special technology steps or extra masks. The reliability and the lifetime of the entire circuit are not affected by the high-voltage operation of the proposed circuit.

This work is divided into four sections. After this introduction, section II reviews commonly used bootstrap switches and discusses features and limitations when the bootstrap switch is used for voltages surpassing the supply. Section III describes

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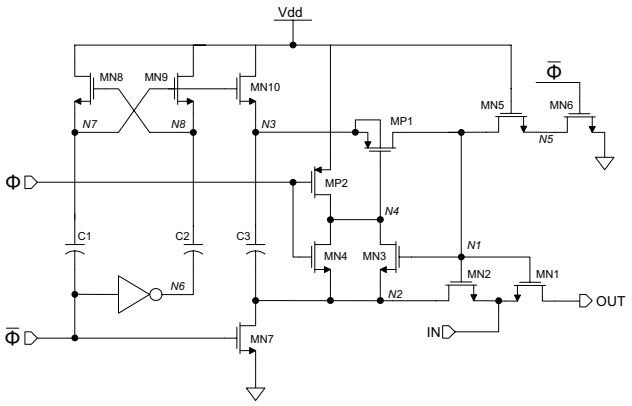
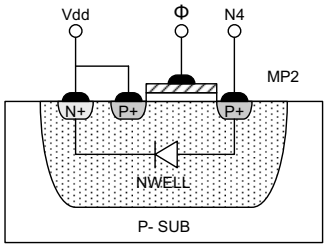


(a)



(b)

Fig. 1. Conventional Bootstrap Switch (a) Circuit Schematic (b) Cross Section of MP2 showing Parasitic Body Diode

the proposed solution. Section IV is on simulations, circuit implementation and experimental results. Section V is on conclusions and discusses the possible uses of the obtained results.

II. Conventional Bootstrap Switch

The most widely used bootstrapped switch in ADC applications [1], [2], [3] is shown in Fig. 1. The transistor MN1 achieves the switch and the remaining part of the circuit serves to generate a gate voltage that is shifted up by MN2, C3 and MP1 with respect to the input voltage. The output of the boosted switch charges the sampling capacitor in ADCs. The voltage across C3 does not exceed the supply so that the driving voltage of the switch transistor is not larger than the supply. Thus, the stress of the gate oxide is within the limits as required by reliability.

The use of the circuit in Fig. 1 with input voltages larger than the supply is not possible. P-channel devices cannot handle a voltage higher than its well bias. If the source (or drain) - well diode is forward biased a large current flows and possibly permanently damages the circuit. The P-channel device of Fig. 1 which will end up with an improperly biased well is MP2. When Φ is high MN4 goes ON and applies the input voltage to the drain of MP2. For an input voltage higher than the well voltage, it would be necessary to automatically switch the well bias to the higher voltage with a complication of the circuit and problems due to the bias switching transient [7].

III. Proposed Bootstrap Switch

Fig. 2 shows the proposed bootstrap switch. The circuit requires only one clock cycle to reach the steady-state operation as it is for the bootstrap switch mentioned above. In the steady-state C1, C2, and C3 are charged at V_{dd}. These capacitors are used to boost the transistors MN5, MN6 and the switch. The phase Φ controls the operation of the circuit. Namely, when Φ is high the switch is on; when Φ is low the switch is off. The steady-state voltages of the used capacitors and the phase control lead to the node voltages given in Table I. They result from the following description of the circuit operation:

- During Φ = 0, MP4 will be OFF because its $V_{gs} = V_{N2} - V_{N3} = 0$, while its drain is at $V_{N1} = 0$
- During Φ = 0, MP3 will be ON because its source is at $V_{N5} = 2V_{dd}$ while its gate is at V_{dd} which will charge N4 to $2V_{dd}$ from the charge stored on C1.
- During Φ = 1, MN2 starts charging N1 until N1 reaches $V_{dd} - V_{tn}$, where V_{tn} is the threshold voltage of an NMOS device. After that MN2 turns OFF because N1 goes to a value above V_{dd} and because there is no longer enough gate overdrive. After that point the circuit works such that the path through MP4 takes over and drives N1 to $V_{dd} + V_{in}$.
- During Φ = 1 and for $V_{in} < V_{tp}$, where V_{tp} is the threshold voltage of a PMOS device, MP4 starts by being OFF because its $V_{gs} = V_{in} < V_{tp}$ ($V_{N3} = V_{dd} + V_{in}$ while N2 stays at V_{dd} because of C4). MN13 will be turned ON pulling N2 to V_{in} which will turn ON MP4 because V_{gs} of MP4 becomes equal to V_{dd} now. As MP4 turns ON the positive feedback loop provided by MN14 and N1 will further connect N2 to V_{in} through MN14.
- During Φ = 1 and for $V_{in} > V_{dd} - V_{tn}$, MN13 will always be OFF because its $V_{gs} < V_{tn}$ (its gate is at V_{dd}, its source is at $V_{in} > V_{dd} - V_{tn}$, while its drain is at V_{dd} or V_{in}). As N3 gets pushed to $V_{dd} + V_{in}$, the voltage on N2 (initially a floating node charged to V_{dd}) will be determined by the capacitive division between C4 and the gate-source parasitic capacitance associated with MP4. By increasing the size of C4, we guarantee that there is enough gate overdrive for MP4 after the capacitive division. This will guarantee that MP4 will turn ON and start charging N1, and the positive feedback through MN14 will further guarantee that N2 is charged to V_{in}
- During Φ = 1 and for $V_{tp} < V_{in} < V_{dd} - V_{tn}$, the switch operates according to a mix of the two cases described above.

The above description and the voltages given in Table I show that in any step of operation and under any condition all the parasitic diodes are reversely biases. Thus the circuit enables switching even if the input voltage is larger than the used supply.

IV. Implementation and Results

The proposed bootstrapped switch was integrated in a 0.35 μm twin-well technology. The transistors MN10 and

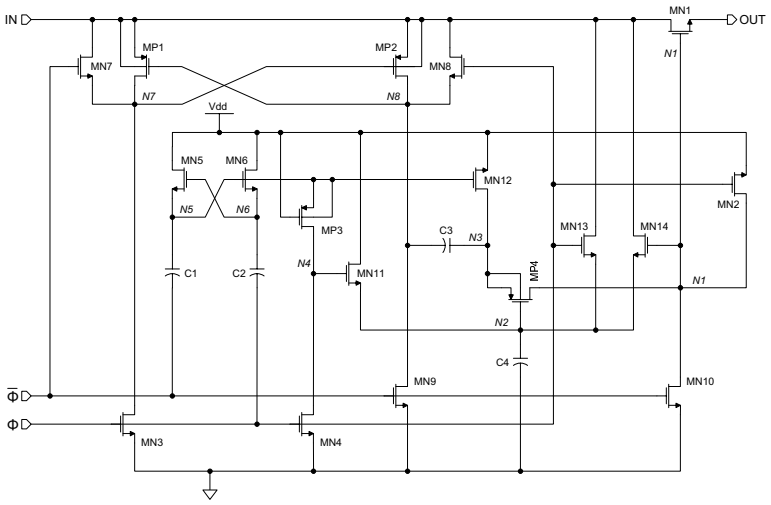


Fig. 2. Proposed Bootstrapped Switch

Node	Φ = 0	Φ = 1
Φ	0	V_{dd}
N1	0	$V_{dd} + V_{in}$
N2	V_{dd}	V_{in}
N3	V_{dd}	$V_{dd} + V_{in}$
N4	$2V_{dd}$	0
N5	$2V_{dd}$	V_{dd}
N6	V_{dd}	$2V_{dd}$
N7	V_{in}	0
N8	0	V_{in}

TABLE I
STATE OF THE NODES AT Φ = 0, AND Φ = 1

MN4, which undergo the greatest oxide stressing, were implemented as thick oxide devices, made available by the used technology. However, the thick oxide option is not a limit to the general use of the proposed circuit. With digital CMOS technologies that do not have thick oxide devices MN10 and MN4 can each be replaced by a series pair of normal transistors and obtain good reliability [1]. The bootstrapped switch is part of the input stage of an ADC with input range exceeding the supply voltage. A standalone version is also incorporated in the chip for characterization purposes.

Fig. 3 shows the simulated gate driving voltage as a function of the input voltage. V_{dd} is equal to 2.75 V and the input range is from 0 to 5.5 V ($2V_{dd}$). Observe that the driving voltage is slightly less than V_{dd} for low input signals and drops by just about 200 mV when the input is almost twice the supply voltage. The result makes the switch suitable for high-frequency sampling: the high-driving voltage and its limited drop will determine a small harmonic distortion. The maximum drain-to-channel voltage allowed by the process reliability limits the maximum input voltage. With technologies with drain-extended devices the design of the switch can be tailored for very high input range operation. Fig. 4 shows the simulated waveforms for an input sine wave with a swing of 0-5.5 V. The supply voltage is 2.75 V. The gate voltage during the on phase tracks the input signal and is shifted up by approximately 2.75 V.

Fig. 5 shows the corresponding measured sampled signal. As expected even if the input goes up to twice the supply voltage the obtained output signal tracks the input signal very well.

The nominal supply voltage is 2.75 V. However the circuit can operate with a lower supply voltage. By inspection of the circuit it can be found that the minimum allowed supply is $2V_{tn}$. Measurement results show that the circuit operates properly for a supply voltage as low as 1.2 V. With this supply voltage the switch can work with input signals up to 6 V. Therefore, the obtained maximum ratio of V_{in}/V_{dd} is 5. The current through the input generator is less than 1 μA. Therefore, the load to the input is negligible and, obviously, there are no diodes that are forward biased.

Fig. 6 shows the microphotograph of the test chip. The active area required for the implementation of the switch was less than 0.008 mm^2.

V. CONCLUSION

A new bootstrapped switch capable of operating with an input voltage much higher than the supply voltage has been presented. The operation is obtained thanks to a circuit solution that avoids forward biasing in the diffusion-well junctions. The switch is suitable for many applications, including various data-converter architectures (SAR-ADC, pipeline, etc.) The switch is able to control the output transistor with a V_{gs} that is almost constant over a wide range of switched voltage. This ensures a low harmonic distortion. Finally, the voltage stress on the transistor gates is well controlled leading to no degradation of the circuit reliability.

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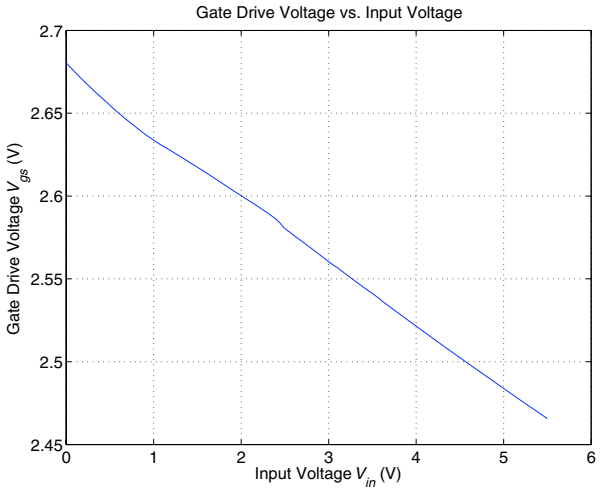

Fig. 3. Gate Drive Voltage V_{gs} vs. Input Voltage V_{in}

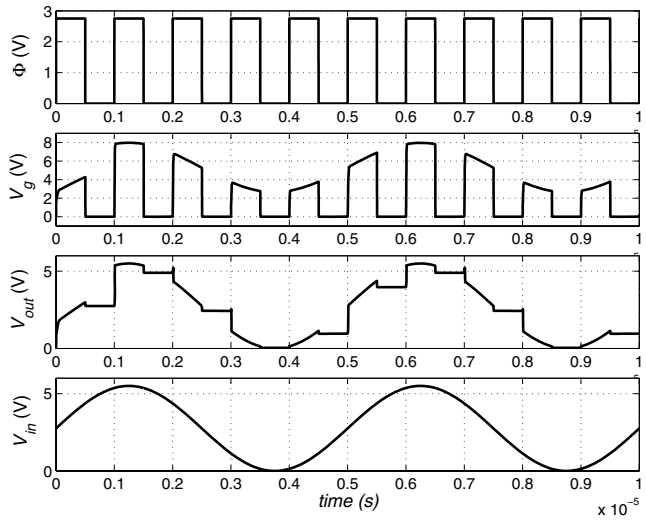

Fig. 4. Simulated Switch Behavior with a Dynamically Changing Input Signal

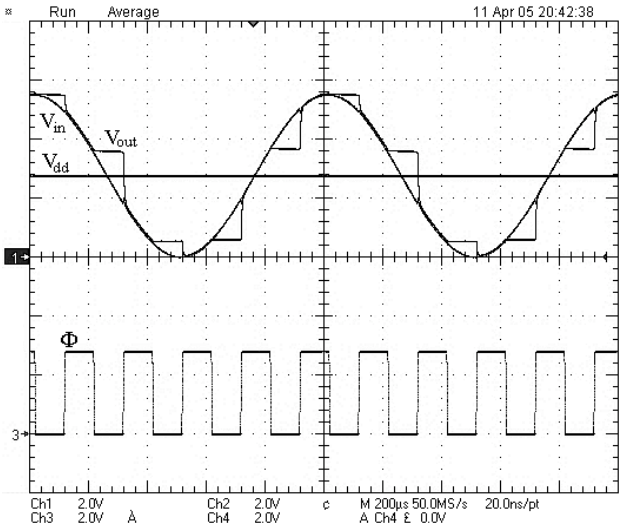

Fig. 5. Measured Switch Behavior with a dynamically Changing Input Signal

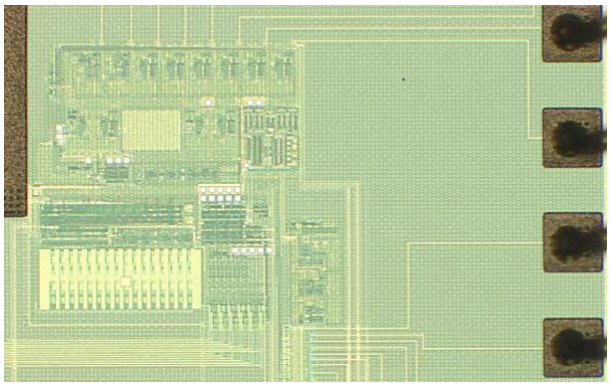

Fig. 6. Die Photo of Test Chip Containing Proposed Bootstrapped Switch

useful suggestions, and their support in bringing about a speedy implementation of this work on silicon.

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