A CAD Framework for Co-Design and Analysis of CMOS-SET Hybrid Integrated Circuits

Santanu Mahapatra[1], Kaustav Banerjee[2], Florent Pegeon[3], Adrian Mihai Ionescu[1]

[1]Electronics Laboratory (LEG), Institute of Microelectronics and Microsystems (IMM), Swiss Federal Institute of Technology Lausanne (EPFL), ELB-Ecublens, Lausanne, CH 1015, Switzerland

[2]Department of Electrical & Computer Engineering, University of California Santa Barbara, CA 93106-9560, USA

[3]Silvaco Data Systems, 55 rue Blaise Pascal, ZIRST II, 38330 Montbonnot St. Martin, Grenoble, France

Email: Santanu.Mahapatra@epfl.ch, kaustav@ece.ucsb.edu, florent.pegeon@silvaco.com, Adrian.Ionescu@epfl.ch

ABSTRACT

This paper introduces a CAD framework for co-simulation of hybrid circuits containing CMOS and SET (Single Electron Transistor) devices. An improved analytical model for SET is also formulated and shown to be applicable in both digital and analog domains. Particularly, the extension of the recent MIB model for single/multi gate symmetric/asymmetric device for a wide range of drain to source voltage and temperature is addressed. Circuit level co-simulations are successfully performed by implementing the SET analytical model in Analog Hardware Description Language (AHDL) of a professional circuit simulator SMARTSPICE. Validation at device and circuit level is carried out by Monte-Carlo simulations. Some novel functionality hybrid CMOS-SET circuit characteristics: (i) SET neuron (ii) Multiple valued logic circuit and (iii) a new Negative Differential Resistance (NDR) circuit, are also predicted by the proposed SET model and analyzed using the new hybrid simulator.

I. INTRODUCTION

Although scaling of CMOS technology has been predicted to continue for another decade, novel technological solutions are required to overcome many limitations of the CMOS [1]. Several *nanotechnologies* are rapidly evolving, but at this point it seems unlikely that any of them can completely replace CMOS [2]. However, co-design of CMOS and some suitable nanotechnology seems more plausible [3]. In fact, in the near future, it seems highly probable that CMOS technology will need to share its present domination on modern ICs with fundamentally new nanotechnologies such as Single Electron Transistors (SET) that use a few electrons [4]. It appears that CMOS and (SETs) are rather complementary: SET is the *campaigner of low-power consumption* [5,6] and of new functionality while CMOS has advantages like high-speed driving and voltage gain, which can compensate exactly for SET's intrinsic drawbacks. Therefore, although a complete replacement of CMOS by single-electronics is highly unlikely in the near future, it is also true that combining SET and CMOS can bring out new functionalities [7-8], which are un-mirrored in pure CMOS technology.

It is well known that Computer Aided Design (CAD) and simulation of electron devices and circuits (using tools like SPICE) are one of the key factors contributing to the success of the CMOS technology. Therefore, a successful implementation of SET as a candidate for hybrid CMOS-nano VLSI also demands accurate modeling and simulation of CMOS-SET devices and circuits. Hence, suitable simulation framework for exploration of hybrid CMOS-SET circuit architectures is highly desirable. In this paper we introduce a new CAD framework for co-simulation of hybrid CMOS-SET circuits. An improved analytical model for SET is also formulated and shown to be applicable in both digital and analog domains. The SET model is validated using Monte Carlo simulations, which are typically used as a benchmark for accurate SET- device and circuit level simulations. Some novel functionality CMOS-SET circuit architectures are analyzed using the new hybrid simulator.

A schematic of a SET, which consists of a tiny conductive island, two high resistive (>26kΩ) tunnel junctions, and an opaque gate is shown in **Fig. 1**. It is worth noting that the operation of the SET devices is based on the *Coulomb Blockade* phenomenon [9], which is quite unique compared to the principle of operation of MOS transistors. By exploiting this particular Coulomb Blockade phenomenon, several *niche* applications of SET devices have been demonstrated in logic circuits (inverter, logic gates etc.)[5,6,10], analog circuits (neuron cell, negative differential circuit [8,11]) and in mixed signal circuits (quantizer [7]) regime.

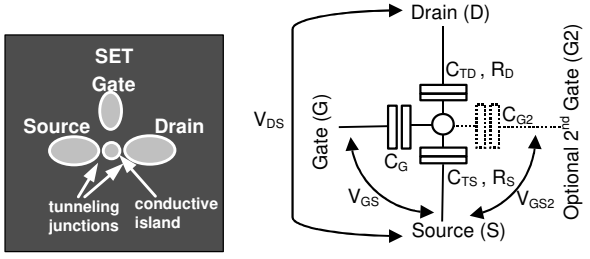


Fig. 1: Schematic of a SET. Here C_G is the gate capacitance, C_{G2} is the optional second gate capacitance, C_{TD} and C_{TS} are the drain and source tunnel junction capacitances, respectively, and R_D and R_S are drain and source tunnel junction resistances, respectively.

II. SET SIMULATION: AN OVERVIEW

Monte Carlo (MC) simulation method is the most popular approach that is employed to simulate single electron devices and circuits. Some of the widely used single-electron MC simulators are SIMON [9], MOSES [12] and KOSEC [13]. Some efforts have also been made to simulate single electron device and circuit characteristics by Master Equation Method (e.g.: SETTRANS [14] simulator). It should be noted that:

1) These methods calculate single electron device and circuit characteristics based on "Orthodox Theory" [9] (i.e., manipulating electron energy with the help of complex Fermi-Dirac distribution and Fermi's golden rule) instead of using any analytical model of SET.

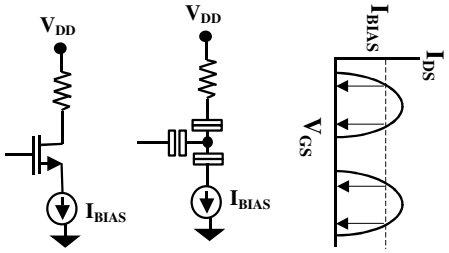
ICCAD'03, November 11-13, 2003, San Jose, California, USA.

2) These simulators are developed in order to simulate generalized single electron devices (where the charging energy of the island is determined not only by the drain, source and gate capacitances associated with it but also other capacitances associated with other islands in the same circuit) and it is quite impossible to find an analytical model for single electron devices. [Note: SET (where the charging energy of the island is determined solely by the drain, source and gate capacitances associated with it) is a special case of generalized Single Electron Devices].

III. CHALANGES OF SET-CMOS CO-SIMULATION

Some previous works have addressed [15] the hybrid SET-CMOS simulation based on background MC or Master equation simulation of SET devices combined with conventional analytical-model based on SPICE simulation for MOSFETs. However, the major disadvantage of these approaches is time-consuming computation (especially for the calculation of transient response, current sources and resistances), and concrete limitations for more complex circuits.

It should also be noted that simulation of SET devices are not as straightforward as CMOS devices. Some architecture, which is commonly used in CMOS technology, may be 'forbidden' in SET circuit. One such example is shown in **Fig. 2**. The architecture in **Fig. 2(a)** is commonly used in CMOS (eg. Differential Amplifier) however similar SET prototype [**Fig. 2(b)**] may create instability in the circuit (and convergence problem in simulation) as the periodic I_{DS}-V_{GS} characteristics of a SET offer several possible values of V_{GS} is for a certain value of I_{BIAS} [**Fig. 2(c)**]. We'll see in §VIII.III how we can exploit such an apparent limitation to provide NDR characteristics in a hybrid CMOS-SET IC.



(a) (b) (c)

Fig. 2: (a) A current bias MOSFET with a floating gate (b) corresponding SET prototype (c) Different possible value of the gate voltage for in (b) for a fixed current bias.

Apart from MC and Master Equation method, "Macro Modeling" technique [16] has also been employed in order to simulate SET devices and circuits. Although this technique is SPICE compatible and useful for co-simulation with MOS, its non-physical (or, empirical) nature makes it an inconvenient tool for practical SET-CMOS hybrid IC design. Therefore, a successful implementation of SET as a candidate for post-CMOS VLSI demands an accurate analytical SET model instead of Monte Carlo (MC) simulation, Master Equation Method or macro modeling.

Recently, two analytical models (MIB [5,17] and another model proposed by Uchida *et al.*[18]) have been reported, which appears to be extremely exciting for practical IC design. These models are physically based, and can explain device characteristics properly and are easy to use them in conventional SPICE simulator for the co-simulation with CMOS devices.

The model reported by Uchida *et al.*[18] is adequately accurate at higher temperature, however it is only applicable to the *single* gate resistively *symmetric* device and it cannot explain the background charge effect, which is significant for SET operations. On the other hand MIB, which is applicable to single/multiple-gate symmetric/asymmetric device, and can explain the crucial background charge effect, is not as accurate as the other [18] at higher temperatures due to its semi-empirical modeling of the temperature effect. One point to be noted is that, both of these models are developed under the basic assumption of $|V_{DS}| \le e/C_\Sigma$ (e is the elementary charge and C_Σ is the total capacitance of SET island with respect to ground), which is quite practical for *digital* circuit (as the SET loses its Coulomb Blockade region and hence the digital switching property when $|V_{DS}| > e/C_\Sigma$). However, for the *analog* application of SET [8], one needs a model, which should be applicable to any value of V_{DS}. This is due to the fact that:

(i) In a current biased SET (which is a common building block of analog SET circuits) the $|V_{DS}|$ could be more than e/C_Σ .

(ii) In CMOS-SET hybrid architecture MOSFET biases may impose $|V_{DS}| > e/C_\Sigma$ to operate the SET.

In this work, we have modified the MIB model in order to extend its validity over $|V_{DS}| > e/C_\Sigma$ specifically for *analog* circuit operation. Moreover, we have modeled the temperature (T) effect physically so that MIB can predict the device behavior accurately at higher temperatures. In order to exploit the proposed model for SET-CMOS hybrid IC design, MIB has been implemented by the Verilog-A interface (which is one type of Analog Hardware Description Language) in professional circuit simulator SMARTSPICE [19]. Using SMARTSPICE different simulations have been performed in SET device and circuit level for different benchmark circuits and good agreement with MC simulation has been observed.

IV. ANALYTICAL MODELS FOR SET: MIB

SET analytical model MIB, is founded on the "orthodox theory of single electron tunneling" [9] (i.e., charge is discrete but energy is continuous, tunnel junction resistance is more than the quantum resistance ~ 26KΩ etc.), is based on a practical assumption that the interconnect capacitance associated with the gate, source and drain terminals are much larger than the device capacitances, which ensures the total capacitance of the island with respect to ground to be equal to the summation of gate and source/drain tunnel capacitances i.e.,

$$C_\Sigma = C_G + C_{G2} + C_{TD} + C_{TS} \quad (1)$$

This assures that the SET characteristics are independent of the capacitances of neighboring devices but only depend upon the nodal voltages of source, gate and drain terminals.

In this work, the following improvements are made over the earlier version [5] of MIB:

- MIB is extended for $|V_{DS}| \le 1.5e/C_\Sigma$ for *resistively symmetric device and* $|V_{DS}| \le 1.2e/C_\Sigma$ *for resistively asymmetric device,* which is essential for analog applications of SET. It is found that for $|V_{DS}| > 1.5e/C_\Sigma$, variation of I_{DS} with V_{GS} becomes too small to exploit in any circuit application.
- The temperature effect is modeled physically that enables to extend the temperature range of MIB.
- Another key result, the Subthreshold Slope can be estimated analytically.

The algorithm for the calculation of drain current in MIB model (**Fig. 3**) can be briefly discussed as follows:

Based on the external bias voltages (V_{DS}, V_{GS}, V_{GS2}) the *initial* (before any electron tunneling occurred) island potential (V_{island}) can be calculated as:

$$V_{island} = (C_{TS}/C_\Sigma)V_{DS} + (C_G/C_\Sigma)V_{GS} + (C_{G2}/C_\Sigma)V_{GS2} - ne/C_\Sigma \quad (2)$$

where n is a real number representing the background charge. Now, according to the "orthodox theory", when the potential difference between island-and-source or drain-and-island becomes larger than V_Σ *[= e/(2C$_\Sigma$)]*, one electron tunnels-in or tunnels-out from the source to island or island to drain and as a result V_{island} decreases (for tunnel-in) or increases (for tunnel-out) by an amount of $2V_\Sigma$. However, if the potential difference between island-and-source or drain-and-island becomes less than V_Σ no electron tunneling happens and device enters into Coulomb Blockade region. The first pair of '*while*' statements in MIB algorithm (**Fig. 3**) is used to modify the initial island potential (V_{island}) in order to capture the periodic Coulomb Blockade oscillation characteristics of SET. Based on this modified value of V_{island}, the drain current (I_{DS}) is formulated as

$$I_{DS} = I_D I_S/(I_D+I_S) \quad (3)$$

Here I_S and I_D are the electron-tunneling *current* from source-to-island and island-to-drain respectively which can be expressed as

$$I_S = \frac{V_{island} - V_\Sigma}{R_S} \frac{1}{1 - exp\left(-\frac{V_{island} - V_\Sigma}{V_T}\right)} \quad (4)$$

$$I_D = \frac{V_{DS} - V_{island} + V_\Sigma}{R_D} \frac{1}{1 - exp\left(-\frac{V_{DS} - V_{island} + V_\Sigma}{V_T}\right)} \quad (5)$$

where V_T (= k_BT/e, k_B is the Boltzmann's constant) is the thermal voltage. It should be noted that these expression of I_S and I_D are purely based on the "orthodox theory" of single tunneling and completely different from the older version of MIB (where temperature effect was modeled empirically).

In order to include the $|V_{DS}| > e/C_\Sigma$ effect, in this work, we have added an extra component to the main component of the drain current as shown in **Fig. 3.**

It is worth noting that all the model parameters of MIB are physical: (i) drain and source tunnelling capacitances (C_{TD} and C_{TS}), (ii) first and second gate capacitances (C_{G1} and C_{G2}), (iii) drain and source tunnel junction resistances (R_D and R_S), and the background charge (n).

V. IMPLEMENTATION OF MIB IN Verilog-A

Verilog-A [19] is a "high level hardware description language" of analog systems by which one can mix SMARTSPICE device models (such as BSIM [19], EKV [19] etc.) and Verilog-A modules in the same netlist. In this work, we have implemented MIB model for SET devices in Verilog-A language and then simulated by the SMARTSPICE simulation kernel as shown in **Fig. 4.** In this way, we can use MIB analytical model to co-simulate SET device with any other solid-state device (MOS, BJT etc.) instead of using the time consuming MC technique [9,12,15]).

In the present work one can use various level of complexity of MIB which are listed as:

LEVEL1: $T = 0$, $|V_{DS}| \le e/C_\Sigma$ (for hand calculation)

LEVEL2: $T < e^2/(20k_BC_\Sigma)$; $|V_{DS}| \le e/C_\Sigma$ (for digital operation)

LEVEL3: $T < e^2/(20k_BC_\Sigma)$; $|V_{DS}| \le 1.5e/C_\Sigma$ for symmetric and $|V_{DS}| \le 1.2e/C_\Sigma$ for asymmetric SET. (analog purpose)

It should be noted that the SET module is implemented with default values of the model parameters (gate capacitances, tunnel junction capacitances and resistances, and back ground charge), which can be changed easily through the MODEL CARD in the SPICE netlist.

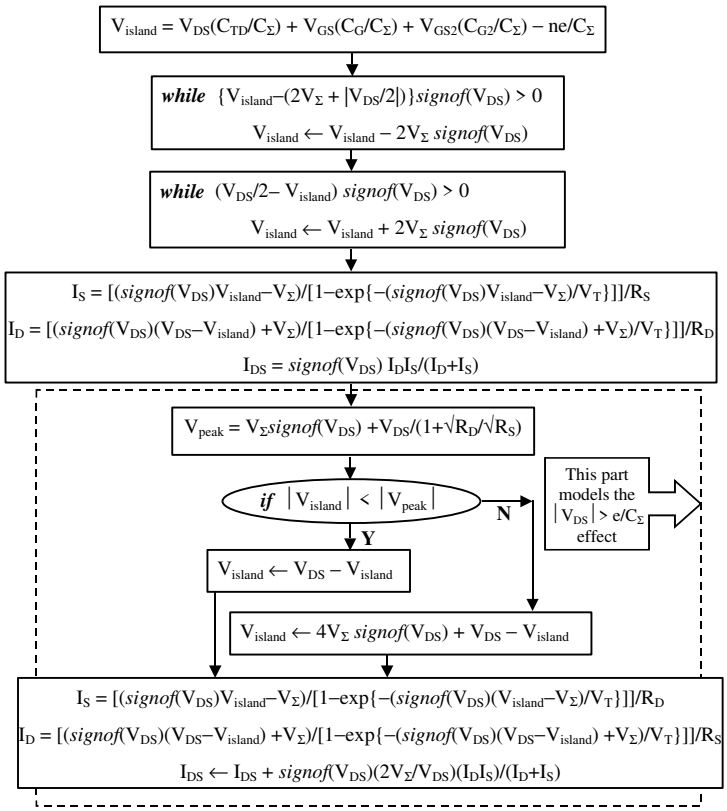
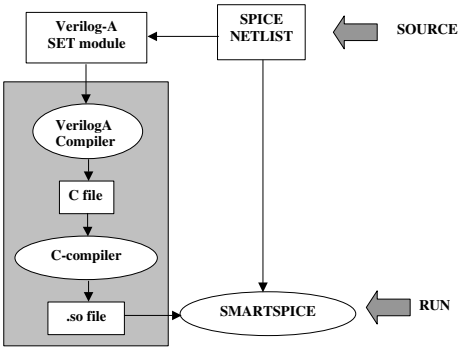


Fig. 3: Flowchart for the MIB analytical Model.

VI. MIB MODEL VERIFICATION

Proposed model (embedded in SMARTSPICE) has been verified against the simulated data from widely accepted Monte Carlo simulator SIMON [9]. **Figure 5(a)** reveals the validity of our model for a wide range (even more than e/C_Σ) of values of V_{DS}, which is important for SET analog operation. **Figure 5(b)** demonstrates the accuracy of our model for asymmetric SET. It should be noted that by introducing asymmetry one could reduce the static power dissipation in SET logic while keeping the dynamic power dissipation and propagation delay almost constant [5]. However importance of resistively asymmetric current biased SET in analog applications has not yet been demonstrated. **Figure 5(c)** exhibits the validity of MIB model for a wide range of temperature up to $T = e^2/(20k_BC_\Sigma)$, Note: According to Kirihara *et al.*[20] maximum temperature for stable SET logic operation is $e^2/(40k_BC_\Sigma)$. From our new model the subthreshold slope (S) of SET is found to be $S = dV_{GS}/d\log_{10}I_{DS} \approx (C_\Sigma k_BT)/(0.434eC_G)$.

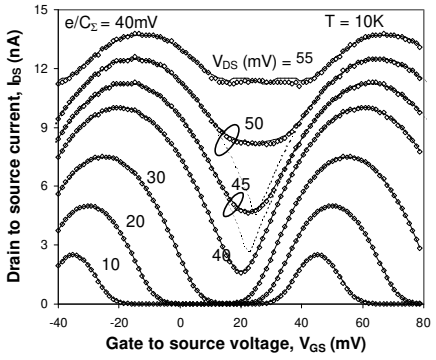


(a)

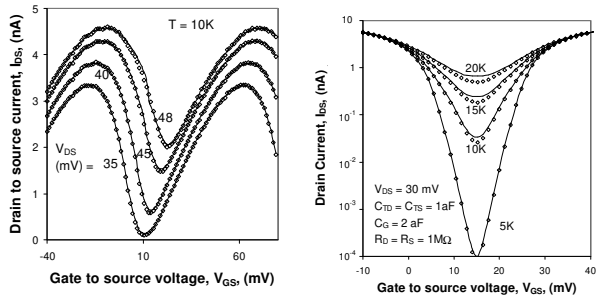
```
module set(drain,gate1,gate2,source);
        inout drain,gate1,gate2,source;
        electrical drain,gate1,gate2,source;

        // Default value of the model parameters
        parameter real CTS = 1e-18, CTD = 1e-18
        parameter real CG = 2e-18, CG2 = 0;
        parameter real RD = 1e6, RS = 1e6;
        parameter real N = 0; // Background Charge
        parameter real T = 0;

        analog
        begin
                ::::::::::::::::::::::::::::::::MIB Subroutine
        end
endmodule
```

(b)

Fig. 4: (a) Working principle of Verilog-A in SMARTSPICE (b) partial architecture of Verilog-A SET module.



(a)



(b) (c)

Fig. 5: Verification of MIB model for (a) symmetric SET device with C_G = *2aF,* C_{TD} = C_{TS} = *1aF* and R_D = R_S = *1MΩ*. Here symbols denote Monte Carlo simulation (SIMON) and solid line represents MIB LEVEL3 and dotted line represents MIB LEVEL2 (without $|V_{DS}| > e/C_\Sigma$ correction). (b) asymmetric device with C_G = *2aF,* C_{TD} = *1.5 aF,* C_{TS} = *0.5aF* and R_D = *1MΩ and* R_S = *5MΩ* (c) effect of temperature on the device characteristics.

VII. PURE SET LOGIC CIRCUIT SIMULATION

Static and transient responses of an SET inverter cell are successfully predicted [**Fig. 6**] by SMARTSPICE simulation. Comparison and good agreement with MC simulation reveals the accuracy of our SPICE simulation in both static and dynamic regimes as given in **Fig. 6(a) & (b)**.

One should note that an SET inverter is different from typical CMOS inverter in the following respects:

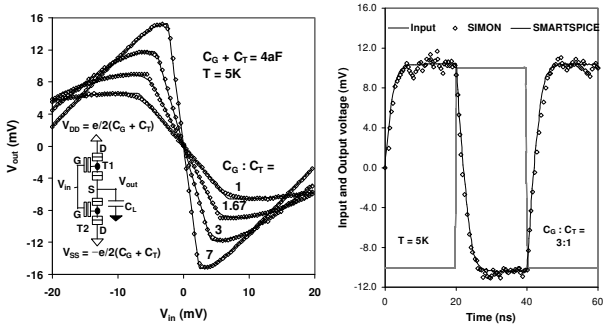
(i) In SET inverter the two transistors are completely identical to each other (in contrast with CMOS inverter where we have one p-MOS and one n-MOS)

(ii) Unlike the CMOS counterpart, the SET inverter does not offer a constant voltage level when the output is in logic high or low.

(iii) The gain of SET inverter is quite low compared to CMOS inverter and it is determined by C_G/C_T ratio.

(iv) Contrast to the CMOS inverter, power dissipation in SET logic is dominated by static power dissipation.

A detailed analysis of SET inverter along with the effect of background charge, device asymmetry and temperature on the inverter characteristics could be found in [5].



(a) (b)

Fig. 6: (a) Schematic of SET-inverter and static and (b) transient characteristics for different values of C_G/C_T (solid line = SMARTSPICE and symbol = SIMON). T1 and T2 are identical with R_D = R_S = *1MΩ,* C_T = C_{TD} = C_{TS} and load capacitance C_L = *1fF*. The oscillations in the MC simulation in Fig.(b) are due to the noise in random number generator.

VIII. HYBRID CMOS-SET IC SIMULATION

As it is mentioned previously that a complete substitution of CMOS by single-electronics is highly improbable in the near future, therefore we have to combine SET and CMOS in order to bring out new functionalities. For these reason it is extremely important to develop a simulator, which can able to co-simulate SET devices with CMOS. In the following sections we will discuss three examples of CMOS-SET hybrid IC.

VIII.I. SET CASCADE NEURONE

Since a powerful signal processor demands a large neural network, therefore, due to the power dissipation and size of the neural chip it is difficult to design efficient neural network by

CMOS technology. However, one can exploit the ultra low power dissipation of SET devices and its nano feature size in order to realize compact neural device.

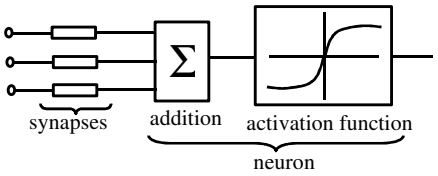


Fig. 7: Functional block diagram of a neuron.

The basic building block of a neuron is given in **Fig. 7.** Most challenging part of this neuron cell is to design the activation function block, which is generally expressed by sigmoidal function as given below

$$f(x) = (1-e^{-ax})/(1+e^{-ax}) \qquad (1)$$

As proposed by M. Goossens [8], the activation function of a basic neuron cell can be implemented by two cascaded current biased SET as presented in **Fig. 8.**

According to Goosens [8], for the proper operation of the circuit, the drain and source tunnel capacitances of the SETs have to be equal ($C_{TD} = C_{TS}$) and gate capacitances have to be twice of that ($C_G = C_{G2} = 2C_{TD}$). One point should be noted that in order to drive *nA* current through the SET one has to bias the MOS transistors in sub-threshold (weak inversion) region.

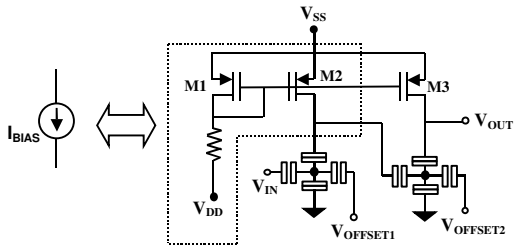


Fig. 8: Basic structure for the realization of the activation function of a neuron as proposed by Goossens [8].

Using SMARTSPICE, the static characteristics of the neuron cell [8], has been simulated accurately and good agreement with MC simulation [**Fig. 9**] demonstrates the reliability of our physical analytical model. Note: In this figure, MIB model without $|V_{DS}| > e/C_{\Sigma}$ correction is represented by dotted line, and that exhibits inaccuracy with MC simulation for a certain range of input voltage, which demonstrates the requirement of a SET model to be valid over $|V_{DS}| = e/C_{\Sigma}$ for analog circuit applications.

VIII.II. MULTIPLE VALUED LOGIC

Multiple-valued logics (MVLs) have potential advantages over binary logics with respect to the number of elements per function and operating speed. Most MVL circuits, been fabricated with MOS and bipolar devices, have limited success partially because the devices are inherently single-threshold or single-peak, and are not fully suited for MVL. Inokawa *et al.*[7] have recently proposed a hybrid SET-CMOS MVL circuit for practical application (e.g., quantizer for digital communication system).

Fig. 10(a) shows the schematic of the hybrid MVL circuit [7]. The MOSFET with the fixed bias V_{GG} is used to suppress the variation of drain to source voltage of the SET. The simulated V_{in}-V_{out} characteristics of this circuit is demonstrated in **Fig. 10(b)** which shows good resemblance with the measured data as presented in [7].

It is impossible to achieve such characteristics by using pure conventional SET circuit because the voltage gain of SET circuits are very small.

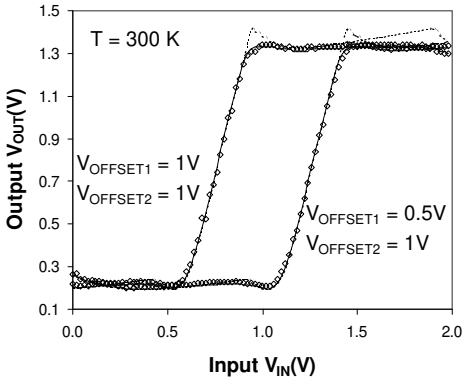
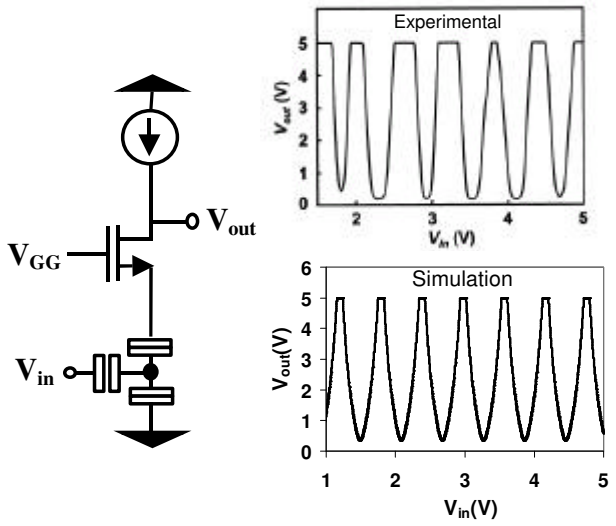


Fig. 9: Characteristics of basic SET-CMOS hybrid neuron cell [5] (with $C_G = C_{G2} = 0.04aF$, $C_{TD} = C_{TS} = 0.02aF$, $R_D = R_S = 1M\Omega$) as predicted by SIMON (symbol) and SMARTSPICE (solid & dotted line). Note: I_{bias} is taken to be ideal current source of *50nA* for SIMON simulation and for SMARTSPICE simulation the MOS current source is designed in such a way that it can drive the same bias current through the SET.



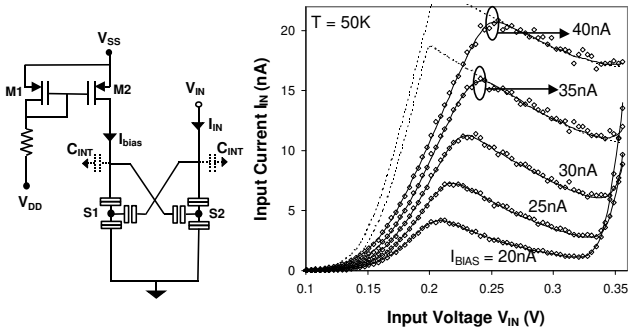
(a) (b)

Fig.10: (a) A schematic of the universal literal gate comprising a SET and a MOSFET [7]. (b) Comparison between measured and simulated V_{in} –V_{out} characteristics of the universal literal gate at T = 27K. The SET device parameters are $C_G = 0.27aF$, $C_{TD} = C_{TS} = 2.7aF$, $R_D = R_S = 200k\Omega$ and MOS device parameters are $W = 12\mu m$, $L = 14\mu m$, $t_{ox} = 90nm$. V_{GG} is set to *1.08V* and V_{out} is hard-limited at *5V*.

VIII.III. HYBRID NDR CIRCUIT

A Negative Differential Resistance (NDR) is a resourceful element with a wide variety of circuit applications such as: oscillators, amplifiers, logic cell and memory. **Figure 11(a)** demonstrates an alternative CMOS-SET architecture of NDR

device [21], which is composed of two cross-connected SETs (S1 and S2) and one MOS current mirror. The I-V characteristics of this NDR circuit and the effect of bias current on the circuit behavior are demonstrated in **Fig. 11(b)**. The CMOS current source and the first SET (S1) creates a feedback loop that helps to decrease the gate-to-source voltage (V_{GS}) of second SET (S2) for a certain range of increasing input voltage (V_{IN}), and that follows a decrease in the drain current (or the input current, I_{IN}) of S2, which creates the NDR effect. It is found this NDR architecture appears more versatile than previously reported structure [11] in terms of dynamic range of NDR region, current controllability and drivability, and offers a very effective solution for real implementation of the NDR functionality.



(a) (b)

Figure 11: (a) Schematic of CMOS-SET hybrid NDR circuit, where, the interconnect capacitance C_{INT} is much bigger than the SET device capacitances (b) NDR characteristics as simulated by SMARTSPICE (solid line: MIB LEVEL3 and dotted line: MIB LEVEL2) and by MC simulation (by replacing the CMOS current mirror by ideal current source, denoted by symbols) for the SET device parameters $C_G = 0.2$ *aF,* $C_{TD} = C_{TS} = 0.15aF$, $R_D = R_S = 1M\Omega$ for S1 and $C_G = C_{TD} = C_{TS} = 0.15aF$, $R_D = R_S = 1M\Omega$ for S2. In order to drive *nA* current through the SET one has to bias the MOS transistors of the current source in the weak inversion or in moderate-inversion region.

It should be noted that similar circuit architecture [22] (cross coupled MOS devices) is also used for oscillator design (in order to provide negative differential resistance) in CMOS technology. In contrast with such cross-connected CMOS architecture, the proposed SET circuit requires an adapted current bias [see I_{BIAS} in **Fig. 11(a)**] to provide NDR behavior.

IX. CONCLUSION

A CAD framework is presented for the design and analysis of CMOS-SET hybrid circuits. An improved analytical model for SET is also formulated and shown to be applicable in both digital and analog domains. Particularly, the extension of the recent MIB model for single/multi gate symmetric/asymmetric device for a wide range of drain to source voltage and temperature is addressed. Proposed model is implemented in professional circuit simulator SMARTSPICE by its Verilog-A interface for the co-simulation with CMOS devices. The model has been validated in both device and circuit level and compared with Monte Carlo simulations. It is worth noting that the proposed MIB model is particularly adapted for both digital and analog hybrid CMOS-SET applications. The need and interest of CMOS-SET hybrid IC simulation has been demonstrated for three IC architecture that demonstrate new functionality compared with pure CMOS: (i) SET neuron, (ii) Multiple Valued Logic circuit (iii) new Hybrid NDR circuit.

References:

[1] The *International Technology Roadmap for Semiconductors* (ITRS), 2002 Edition.

[2] J. A. Hutchby, et al., "Extending the road beyond CMOS," *IEEE Circuits and Devices Magazine*, Volume: 18 Issue: 2, pp: 28 –41, March 2002.

[3] M. M. Ziegler and M. R. Stan, "A case for CMOS/nano co-design," *Proc. ICCAD*, 2002, pp. 348-352.

[4] A.M. Ionescu, M. Declercq, S. Mahapatra, K. Banerjee, J. Gautier, "Few electron devices: towards hybrid CMOS-SET integrated circuits", *DAC* 2002, pp. 88-93.

[5] S. Mahapatra, A.M. Ionescu, K. Banerjee, M.J.Declerq, "Modelling and analysis of power dissipation in single electron logic", *Technical Digest of IEDM 2002.*

[6] K. Uchida, J. Koga, R. Ohba, A. Toriumi, "Programmable single-electron transistor logic for low-power intelligent Si LSI", *ISSCC* 2002, Vol. 2, pp. 162-453.

[7] H. Inokawa, A. Fujiwara, Y. Takahashi, "A multiple-valued logic with merged single-electron and MOS transistors" *IEDM* 2001, pp. 147 -150.

[8] M. Goossens, "Analog neural networks in single-electron tunneling technology", Delft University Press, Nederlands.

[9] C. Wasshuber, "Computational Electronics", Springer Verlag, New York.

[10] Y. Ono and Y Takahashi, " Single electron pass transistor logic and its application to a binary adder", *Symposium on VLSI Circuits 2001*, pp. 63-66.

[11] C. P. Heij, D. C. Dixon, P. Hadley and J. E. Mooij, "Negative differential resistance due to single-electron switching", *Applied Phys. Lett.*, Vol. 74, No. 7, pp. 1042-1044, 1999.

[12] R. H. Chen, A. N. Korotkov, and K. K. Likharev, "A new logic family based on single-electron transistors", *Device Research Conference*, pp. 44-45, 1995.

[13] KOSEC(KOrea Single Electron Circuit simulator) is developed in Nanoelectronics Laboratory, Korea University, Seoul, Korea.

[14] http://hana.physics.sunysb.edu/set/software

[15] M. Fujishima, S. Amakawa and K. Hoh, "Circuit simulators aiming at single-electron integration", *Jpn. J. Appl. Phys*., Vol. 37, pp. 1478-1482, 1998.

[16] Y. S. Yu, S. W. Hwang, and D. Ahn, "Macromodeling of single electron transistors for efficient circuit simulation", *IEEE Trans. Electron Devices*, Vol. 46, No. 8, pp 1667-1671, 1999.

[17] S. Mahapatra, A.M. Ionescu, K. Banerjee, "A quasi-analytical SET model for few electron circuit simulation", *IEEE Electron Dev. Lett*., Vol. 23, No. 6, pp. 366 –368, 2002.

[18] K. Uchida, K. Matsuzawa, J. Koga, R. Ohba, S. Takagi, and A. Toriumi, "Analytical single-electron transistor (SET) model for design and analysis of realistic SET circuits", *Jpn. J. Appl. Phys.*, Vol. 39, Part 1, No. 4B, pp. 2321-2324, 2000.

[19] SMARTSPICE User Manual, SILVACO Inc., www.silvaco.com

[20] M. Kirihara, N. Kuwamura, K. Taniguchi and C. Hamaguchi: Ext. Abst. 1994 *Int. Conf. Solid State Devices and Materials* (Business Center for Academic Socities Japan, Tokyo, 1994), pp. 328.

[21] Ongoing research in authors' group.

[22] A. Hajimiri, T. H. Lee, "The design of low noise oscillators", Kluwer academic publishers, 1999, Boston, USA.