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LETTER

# A Capacitively Coupled Digital Isolator Using Multiple-pulse-coding Architecture with CMTI of 200 kV/μs and Static Current of 60 μA

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**Abstract** This paper presents a capacitively coupled digital isolator with low power consumption and superior Common Mode Transient Immunity (CMTI). It proposes a multiple-pulse-coding architecture and a receiver with an adaptive architecture, which improve the transmission accuracy, eliminate the CMT and achieve low power consumption. The multiple-pulse-coding characterizes edge signal with multi-pulses. The receiver consists of an adaptive pre-amplifier and an adaptive comparator. Fabricated in a 0.18 μm CMOS process, the chip achieves 200 kV/μs CMTI, 60 μA static current, 250 μA dynamic current and 14 kV isolation breakdown voltage with the area of the isolation capacitance of $2\times10^4$ μm$^2$.
**key words:** digital isolator; CMTI; low power consumption; multiple-pulse-coding; adaptive architecture; pre-amplifier.
**Classification:** Integrated circuits (memory, logic, analog, RF, sensor)

## 1. Introduction

Electrical isolators such as digital isolators are widely employed in low-power applications, such as electricity meter, industrial automation and solar inverters that require the safety transmission between different voltage domain [1-6]. Digital isolators with exceptional Common Mode Transient Immunity (CMTI) and low power consumption are becoming increasingly significant in the noisiest and harsh environment. This means that the signal must be precisely transmitted while remaining immune to extremely fast Common Mode Transient (CMT) and other noise. Furthermore, the isolator should have a low power consumption.

In comparison with optocoupler isolators, transformer isolators [1, 2, 3, 4, 7-24] and capacitive isolators [5, 6, 25-30] are sprouting up as general isolation architectures because of their smaller size, faster speed, lower power consumption and better CMTI. Ref. [1] presents a polyimide-based digital isolator using on-chip inductor and the On-Off Keying (OOK) architecture. In Ref. [1], the OOK transmitter (TX) resonates directly with the transformer to generate a high frequency carrier signal based on LC tank oscillator. Moreover, in front of the RX, an AC-coupled bias network is used to attenuate the CMT noise without affecting the carrier signal. Therefore, Ref. [1] can achieve 200 kV/μs CMTI. However, the power consumption reaches 2.8 mA due to the kick-start scheme oscillation using the OOK architecture. In addition, the micro-transformer, which is typically larger than 250 μm in diameter, occupies too much area and even need another die to place it [4]. To solve the problems of large occupied area of the transformer and the large power consumption, Refs. [2, 3] presents a digital isolator using smaller transformers and pulse modulation. Here, the pulse modulation, which is sensitive to signal edge, has extremely low static power consumption. However, its anti-interference ability is inferior than OOK modulation and has lower CMTI. In addition, the transformer in Ref. [2] still has a diameter of 230 μm, requiring a high-gain receiver to compensate for poor gain. Therefore, Ref. [2] developed a GHz-band signal generation, which inevitably degrades the CMT and noise immunity. Hence, Ref. [2] achieves 1.6 mA power consumption and Ref. [3] achieves 0.3 mA power consumption. However, only 35 kV/μs and 25 kV/μs CMTI could be provided due to the small transformer and the limited of pulse modulation. To achieve smaller isolation element area and higher CMTI, Ref. [5] presents a $SiO_2$-based digital isolator using capacitors and OOK architecture. The area required for the capacitive isolation in Ref. [5] is $3.00\times10^4$ μm$^2$, which is about 1/5 that of a conventional micro-transformer. However, capacitive isolators are limited to CMTI of 100 kV/μs even with the OOK modulation [1, 5]. Moreover, the currently available capacitive isolator still requires current consumption of 1.5 mA, which should be further decreased.

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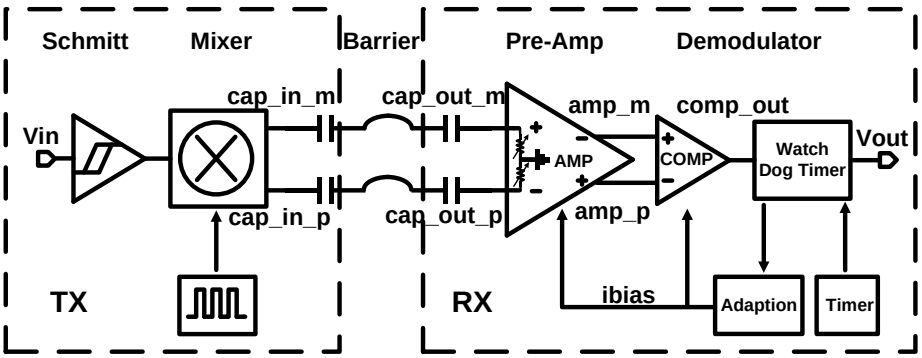



**Fig. 1.** Block diagram of the proposed capacitively digital isolator architecture with the low power consumption and the superior CMTI.

This paper proposes a $SiO_2$-based capacitively coupled digital isolator, which adopts a multiple-pulse-coding architecture and a receiver with an adaptive architecture. The multiple-pulse-coding architecture features high CMTI and low power consumption, compared with OOK and conventional pulse modulation. It characterizes a rising edge signal with 12 high-frequency short pulses and a falling edge signal with 6 high-frequency short pulses. It is applied to improve the accuracy of transmission, eliminate the effect of CMT and achieve the low power consumption. Furthermore, this paper proposes an adaptive architecture to modify the size and the duration of the bias current based on the number of pulses, thus alleviating the strong dependence of signal transmission on the static bias current. Besides, the receiver with an adaptive architecture consists of an adaptive pre-amplifier, an adaptive comparator and a watch dog timer, which restores multi-pulses and transmits them into rising edge or falling edge. Here, ≥ 9 pulses are decoded in the rising edge, while ≥ 3 and < 6 pulses are decoded in the falling edge, which can improve the noise immunity. Therefore, the receiver work in the lowest current bias mode when there is no signal transmitted.

In addition, the adaptive pre-amplifier is designed into a gate-cross-coupled common-gate amplifier with an active zero load, which further improves the noise immunity and CMTI. By applying the proposed active zero load, the high-frequency gain retains to high value, while the low-frequency gain is greatly attenuated.

This paper is organized as follows. Section 2 introduces the proposed multiple-pulse-coding architecture and the receiver with an adaptive architecture of the capacitively coupled digital isolator. Section 3 describes the detailed circuit implementation of the adaptive pre-amplifier and the adaptive hysteresis comparator. Section 4 presents the measurement results and finally a conclusion is given.

## 2. Isolator Architecture

Fig. 1 shows the proposed $SiO_2$-based capacitively coupled digital isolator using the multiple-pulse-coding architecture and the receiver with an adaptive architecture. The TX modulates the digital input signal $V_{in}$ into *cap_in_m* and *cap_in_p* and then transmits them through the isolation capacitor. The mixer enables the TX to keep generating the fully-differential high-frequency multiple-pulse signal to reject noise or CMT. Next, the RX receives the *cap_out_m* and *cap_out_p* and then restores them into *comp_out* and, at last, decodes them into $V_{out}$. Here, the RX adopts a gate-cross-coupled common-gate pre-amplifier, a hysteresis comparator circuit and a watch dog timer circuit to restore the multiple-pulses and decode the wide number range of multiple-pulses to the original edge signal.

The capacitive isolator employed in this work is so small that the amplitude of the signal received by the RX node is small and sensitive. Thus, for normal signal transmission, a high gain receiver is adopted. However, it leads to the limitation of CMTI and high bias current for signal amplification. Therefore, the multiple-pulse-coding architecture and the receiver with an adaptive architecture are proposed for surmount this weakness.

Here, key nodes' waveforms of the multiple-pulse-coding modulator and demodulator are shown in Fig. 2. Here, the adaption is the time that the receiver works in high current bias, which is designed for further reducing the power consumption. The waveform's detailed description will be handled in the multiple-pulse-coding and adaptive receiver sections, respectively.

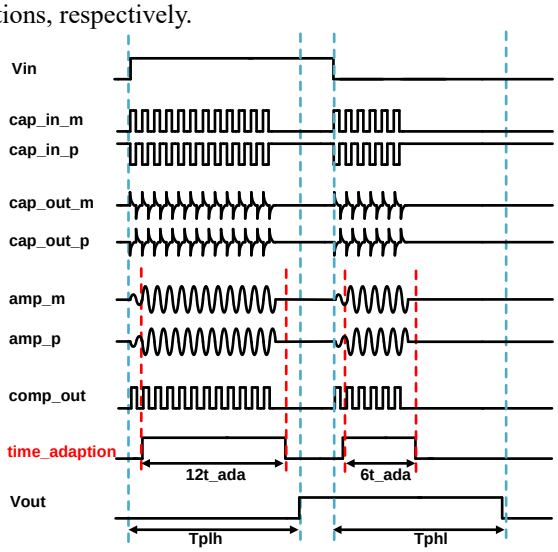



**Fig. 2.** Modulator and demodulator operation waveform.

2.1 Multiple-pulse-coding

This work proposes a multiple-pulse-coding architecture to meet the demand of signal transmission accuracy and low power consumption. Compared with OOK and conventional pulse modulation, the multiple-pulse-coding can achieve high capability in noise tolerance and low power consumption simultaneously.

The multiple-pulse-coding characterizes a rising edge signal with 12 high-frequency short pulses and a falling edge signal with 6 high-frequency short pulses. When detecting the first pulse signal, the watch dog timer starts timing with a preferred setting detection time of 100 ns. Then, within the predetermined detection time limit of 100 ns, if the number of pulses is ≥ 9, the watch dog circuit will decode them in the rising edge signal, and if the number of pulses is ≥ 3 and < 9, the watch dog circuit will decode them in falling edge signal, and if the number of pulses is < 3, the watch dog circuit will treat them as interference and will not output the signal. Thus, there are 3 allowable error ranges of pulses caused by CMT or noise, which improves the reliability of signal transmission.

In addition, the counter will be cleared when the predetermined time frame is exceeded. Meanwhile, the predetermined time of 100 ns is designed as the propagation delay between $V_{in}$ and $V_{out}$, which is longer than 16 cycles of the pulses. Furthermore, the watch dog timer does not detect the edge and is always in the sleep state when the input signal is held high or low for a long time. Besides, the transmitter works in digital domain for less static power consumption.

2.2 Adaptive Receiver

The receiver consists of an adaptive pre-amplifier, an adaptive high-pass filter before the pre-amplifier, an adaptive comparator and a watch dog timer circuit. It significantly reduces the power consumption and improves the accuracy of data transmission. Here, the bias current of the pre-amplifier and the comparator is adaptive, resulting in a static power consumption of only 60 μA. Then, when a pulse signal is detected by the watch dog timer, the pre-amplifier and the comparator will receive an "open" signal from the watch dog timer and enter the high performance mode, increasing the bias current. The pre-amplifier with high bias current facilitates decent high-frequency gain and the comparator with high bias current ensures the high speed comparison performance. Furthermore, the duration of high bias current mode is also adaptive and increases with the number of pulses detected by the watch dog timer, which can further reduce the dynamic power consumption.

Fig. 3 shows the proposed implementation scheme of the duration of the high bias current mode. The watch dog timer detects the amount of the pulses and sets the duration of adaption. Here, the adaption modular turns on the high bias current mode and triggers of *T_delay* time after the first pulse is detected. Then, when the counter detects a pulse, the duration is extended by *t_ada* time. That is, a rising edge of input signal will make the high bias current mode last for 12 *t_ada*, and a falling edge of input signal will make the high bias current mode last for 6 *t_ada*. The watch dog timer is bound to be reset after *T_delay* time, which is longer than 12 *t_ada*.

Here, the bias current of receiver working in low performance mode is 1/6 of that working in high performance mode, which means that if the work always working in high performance, the static bias current will arrive to 360 μA. Then, the dynamic current under 1 Mbps signal of this work is 250 μA. If the chip of digital isoaltor works without proposed adaptive architecture, the dynamic current will reach 1.3 mA.

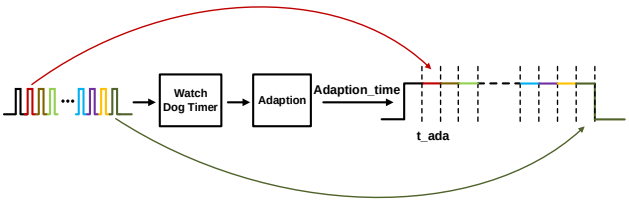



**Fig. 3.** Implementation scheme of duration of high bias current mode.

## 3. Circuit Implementation

This work employs a gate-cross-coupled common-gate amplifier with an active zero load and a hysteresis comparator. Furthermore, the bias current of the pre-amplifier and the comparator are adaptive based on the multiple pulses. Therefore, the circuit implementations of the pre-amplifier and the comparator are also discussed in following.

3.1 Adaptive Pre-amplifier

Fig. 4 gives the circuit implementation of the proposed pre-amplifier, which consists of an adaptive gate-cross-coupled common-gate amplifier, a coupling capacitor, an active zero load and an adaptive high-pass filter. The pre-amplifier is fully differential with symmetric layout to improve noise immunity. Here, the bias circuit is made up of an $IPTAT_1$, $IPTAT_2$, $M_{N4} \sim M_{N2}$, $M_{N3} \sim M_{N1}$, $M_{P2}$ and $R_2$, $R_3$. With the consistent bias circuit for differential signal, the pre-amplifier provides a good common-mode rejection. Moreover, the gate-cross-coupled common-gate amplifier doubles the differential-mode gain to $2G_m$, and cancels the common-mode gain for further common-mode rejection. When there is no pulse signal detected by watch dog timer, the *adaption* signal is set low logically, which means that the pre-amplifier is working in low bias current mode. Here, only $IPTAT_1$ is set as bias current, providing low gain for the pulse signal. Therefore, $M_{N5}$ is turned off and meanwhile, $R_3$ and $R_4$ are connected in series for a higher sampling resistance. Here, it can provide higher gain. When there is a pulse signal detected by the watch dog timer, the *adaption*

signal will be set logic high for a corresponding time. Then, $IPTAT_1$ and $IPTAT_2$ are combined to work as a bias current to improve the gain of pre-amplifier at high frequency. Meanwhile, $M_{N5}$ is turned on and only $R_3$ is set as sampling resistance, to avoid the interfere from CMT. Here, CMT is dominated by $dV_{CMT}/dt$. A potential shift at the capacitance causes a displacement current. A 200 kV/μs CMT from the TX side may cause more than 1 V *IR* drop on $R_3$ and $R_4$. The DC operation bias of the pre-amplifier is constructed over the sampling resistance $R_3$ and $R_4$, resulting in a DC operation offset. The proposed high-pass filter absorbs the current caused by CMT with minimal impact on the operation of the pre-amplifier.

Furthermore, an active zero compensation circuit, composed of $M_{P1}$, $R_1$ and $C_1$, is designed as the load of the amplifier. Here, an active zero is implemented using a local feedback. In the active zero circuit, the local feedback $T_{AZC}$ is composed of $R_1$, $C_1$ and $g_{MP1}$. Due to this inductive load, the high frequency carrier signal can be amplified and the low frequency noise can be eliminated by the pre-amplifier.

The decent gain of the proposed pre-amplifier adapting active zero and the high-pass filter has already been verified. Equation (1) (2) describes the overall transfer function working in low bias current mode and high bias current mode. Moreover, the $G_{MN2}$ doubles the $g_{MN2}$ under this bias.

$$\frac{V_{out}}{V_{in}} \approx \frac{s(R_3+R_4)C_5}{s(R_3+R_4)C_6+s(R_3+R_4)C_5+1} \times \frac{2g_{MN2\_low}(1+sR_1C_1)}{g_{MP1\_low}+sC_1+s^2R_1C_1C_2} \tag{1}$$

$$\frac{V_{out}}{V_{in}} \approx \frac{sR_3C_5}{sR_3C_6+sR_3C_5+1} \times \frac{2g_{MN2\_high}(1+sR_1C_1)}{g_{MP1\_high}+sC_1+s^2R_1C_1C_2} \tag{2}$$

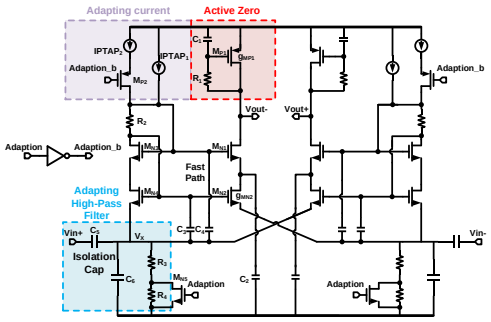



**Fig. 4.** The proposed adaptive pre-amplifier with active zero load and high-pass filter.

3.2 Adaptive Hysteresis Comparator.

Fig. 5 gives the circuit implementation of the proposed comparator, which consists of an adaptive hysteresis comparator and filter. This comparator can improve the accuracy of signal transmission without sacrificing power consumption. Here, the hysteresis strength is decided by the bias current, which is adaptive according to the detected pulses. The comparator in the large bias current mode integrates a strong hysteresis, leading to reliable signal overturning. Moreover, the offset is self-adaptively adjusted with the mode, that is, combining high offset with high bias current mode and combining low offset with low bias current mode, which further avoids the noise caused by the high speed of the comparator. Besides, $N_{bias}$ creates and adjusts the offset of the comparator, making an original offset to determine initial value. Simultaneously, it adopts a filter that provides a decent improvement in CMTI by canceling the glitch generated by the CMT while maintaining signal transmission.

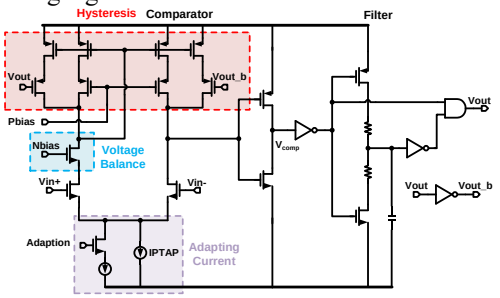



**Fig. 5.** The proposed adaptive hysteresis comparator.

## 4. Chip Fabrication and Experimental Results

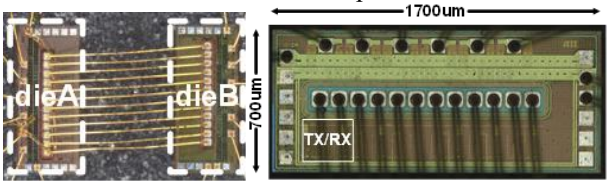
4.1 Chip Fabrication.

The proposed capacitively coupled digital isolator was implemented and verified using a 0.18 μm isolated CMOS technology without additional process required. The bottom metal layer is used as the lower plate of the capacitance, the top metal layer is used as the upper plate of the capacitance, and the 20 μm thick $SiO_2$ between the two layers is used as the insulation material. Here, the isolation technology, 20 μm thick $SiO_2$, can provide 7,000 V isolation voltage. Moreover, with the "back to back configuration" that uses bonding wires to connect the isolation capacitances on both sides of the die, the capacitance provides twice the isolation breakdown voltage, which is 14 kV.

As shown in Fig. 6 (a), there are two dies on one chip with six transmission channels, each channel containing two isolation capacitances for differential transmission. Fig. 6 (b) gives the single die photo of the prototype with area of around 1700×700 μm$^2$. The isolation element area of one channel is 2×10$^4$ μm$^2$, which is 1/2 that of [1], 1/10 that of conventional transformer-based isolator and 2/3 that of [5]. The prototype operates with input and output voltage of 2.25 V to 5.5 V. Besides, it can operate over a wide temperature range of -55 ℃ to 125 ℃.

The test platform for the propagation function and CMTI can measure the electrical parameters and dynamic characteristics of the isolator as shown in Fig. 7. CMT, confirmed by $dV_{CMT}/dt$, is generated by the IGBT, an isolator driver which is a floating power supplied by a battery and high-voltage power supply. Moreover, the value of $dV_{CMT}/dt$ is determined by a charging resistance and capacitance.

Finally, the CMTI is calculated by detecting the presence of erroneous transmission in the output of the RX.




(a) (b)

**Fig. 6.** Micrograph of the (a) chip, (b) single die.

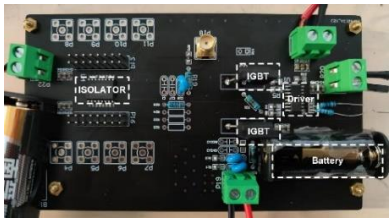
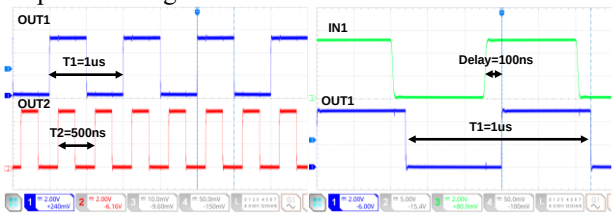



**Fig. 7.** Testing platform of propagation function and CMTI.

## 4.2 Experimental Results

Here, DR1 and DR2 are the different input data rate for two channels, which can measure the cross-talk between these two channels. An operation is shown in Fig. 8 (a), in which two channels transmit 2 Mbps and 4 Mbps signals, and signals can be conveyed normally. Besides, there is no crosstalk in the output signals between the two channels. Fig. 8 (b) demonstrates that the delay between the input and output of the signal is near 100 ns.




(a) (b)

**Fig. 8.** Propagation test: (a) DR1=2 Mbps, DR2=4 Mbps, (b) DR1=2 Mbps.

Fig. 9 shows the power consumption in different frequency of input signal. Here, the static bias current is 60 μA, and the dynamic current is 0.25 mA in 5 V at 1 Mbps data rate with 5 V supply and 15 pF load.

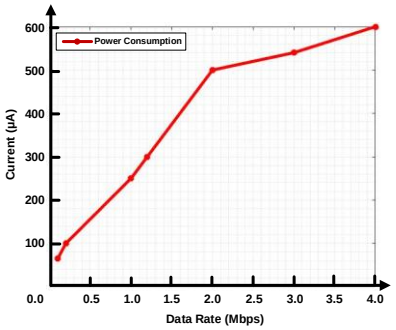
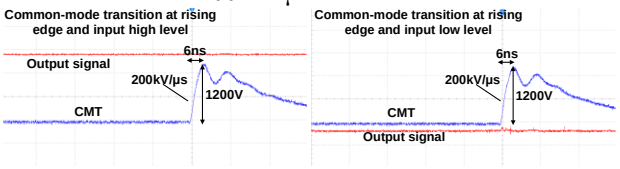



**Fig. 9.** Power Consumption with the data rate.

Fig. 10 shows the measured CMTI performance for a positive CMT pulse under the typical operating conditions, i.e., a CMT voltage amplitude of 1,200 V and a slew rate of 200 kV/μs. Fig.10 (a) (b) shows that the input signal set to logically high level and low level respectively. In this test platform, the yellow line represents CMT occurring in die A. Here, the signal can be transmitted normally regardless of whether the output is high or low,, which signifies that the CMTI can achieve 200 kV/μs.




(a) (b)

**Fig. 10.** CMTI test with 200 kV/μs, 1,200 V amplitude (a) input high level (b) input low level.

Table I shows a summary of the proposed work and the prior state-of-the-art performance. It can be inferred from the table that the proposed work achieved superior CMTI and low power consumption.

**Table 1** Performance comparison tables.

| | VLSI 2016 [1] | JSSC 2012 [2] | ADI ADuM1100 2015 [3] | MWSCAS 2022 [4] | TI ISO77xx 2020 [5] | This Work |
|---|---|---|---|---|---|---|
| **Isolation Element** | Transformer | Transformer | Transformer | Capacitor | Capacitor | Capacitor |
| **Isolation Element Area Per Channel ($\mu m^2$)** | N/A | $4.15\times10^4$ $\mu m^2$ | N/A | N/A | $3.00\times10^4$ $\mu m^2$ | $2.00\times10^4$ $\mu m^2$ |
| **Isolation Material** | Polyimide | $SiO_2$ | Polyimide | $SiO_2$ | $SiO_2$ | $SiO_2$ |
| **Modulation Architecture** | OOK | Pulse | Pulse | OOK | OOK | Pulse |
| **CMTI (kV/μs)** | 200 | 35 | 25 | N/A | 100 | 200 |
| **Idd@5 V, 1 Mbps (mA)** | 2.8 | 1.6 (@DC) | 0.3 | 1.4 | 1.5 | 0.25 |
| **Isolation Voltage (kV)** | 20 | 2 | 10 | 2.5 | 5 | 14 |
| **Supply Range (V)** | 1.7~5.5 | 3.3~5.5 | 3.0~5.5 | N/A | 2.25~5.5 | 2.25~5.5 |

## 5. Conclusion

This paper presents a small-size on-chip capacitively coupled digital isolator with low power consumption and superior CMTI. It proposes a multiple-pulse-coding architecture and a receiver with an adaptive architecture, which improve the transmission accuracy, eliminate the CMT and achieve low power consumption. The multiple-pulse-coding characterizes edge signal with multi-pulses. Furthermore, the receiver with adaptive architecture modifies the size and the duration of the bias current based on the number of pulses, alleviating the strong dependence of the signal transmission on the static bias current. Fabricated in a 0.18 μm CMOS process, the chip achieves 200 kV/μs CMTI, 60 μA static current and 250 μA dynamic current. In addition, it can provide twice the isolation voltage with "back to back configuration" to achieve an isolation breakdown voltage of 14 kV with the area of the isolation capacitance of $2\times10^4$ μm$^2$. The prototype operates at an input voltage and output voltage of 2.25 V to 5.5 V and a wide temperature range of -55 ℃ to 125 ℃.

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