A Capacitor Cross-Coupled Common-Gate Low-Noise Amplifier

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Abstract—The conventional common-gate low-noise amplifier (CGLNA) exhibits a relatively high noise figure (NF) at low operating frequencies relative to the MOSFET f_T, which has limited its adoption notwithstanding its superior linearity, input matching, and stability compared to the inductively degenerated common-source LNA (CSLNA). A capacitor cross-coupled g_m-boosting scheme is described that improves the NF and retains the advantages of the CGLNA topology. The technique also enables a significant reduction in current consumption. A fully integrated capacitor cross-coupled CGLNA implemented in 180–nm CMOS validates the g_m-boosting technique. It achieves a measured NF of 3.0 dB at 6.0 GHz and consumes only 3.6 mA from 1.8 V; the measured input-referred third-order intercept (*IIP3*) value is 11.4 dBm. The capacitor cross-coupled g_m-boosted CGLNA is attractive for low-power fully integrated applications in fine-line CMOS technologies.

Index Terms—Common-gate amplifier, low-noise amplifier (LNA), noise figure (NF), RF integrated circuits.

I. INTRODUCTION

WITH power consumption increasingly becoming a controlling factor in CMOS receiver design, the development of low power RF circuit techniques is necessarily generating considerable attention. The first on-chip active stage of an RF receiver is usually a low-noise amplifier (LNA). The well-known Friis equation sets its two most important specifications—low noise factor and high gain [1]. The basic common-source LNA (CSLNA) topology provides better noise performance than the conventional common-gate LNA (CGLNA) at low operating frequencies relative to the MOSFET f_T; however, lower noise figure (NF) is often achieved using higher power consumption or off-chip matching components. Hence, the CSLNA topology is sub-optimum in low-power fully integrated applications. Increasing RF operating frequencies motivate the need for circuit design techniques that improve the NF of CGLNA and preserve its linearity, stability and low power consumption advantages. The capacitor cross-coupled CGLNA (CCC-CGLNA) [2] described herein achieves these goals.
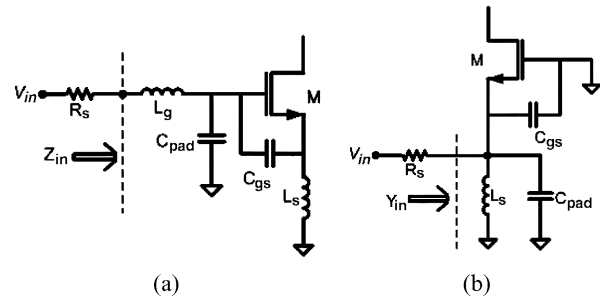
Fig. 1. Basic LNA stages. (a) CSLNA. (b) CGLNA.

Section II briefly compares the conventional CSLNA and CGLNA topologies [3], and Section III describes the general g_m-boosting technique. The capacitor CCC-CGLNA topology [2] is described in Section IV, and design and measurement results are presented in Section V.

II. CSLNA VERSUS CGLNA TOPOLOGIES

The critical benchmarks for characterizing the performance of an LNA are gain, NF, power consumption, reverse isolation, stability, linearity, ease of input matching and matching accuracy usually relative to 50 Ω.

The currently popular CSLNA topology [Fig. 1(a)] uses inductive degeneration to match the input impedance at resonance $(\omega_T L_s)$ to 50 Ω [4]. Its input impedance can be expressed as

$$Z_{\text{in,CSLNA}} \approx sL_g + \left(\frac{1}{sC_{\text{pad}}} \right) // \left(\omega_T L_s + sL_s + \frac{1}{sC_{gs}} \right) \tag{1}$$

where $\omega_T = g_m/C_{gs}$ is the unity current gain frequency of the MOSFET. An effective series resonance created at the RF operating frequency leads to a noiseless resistive input match, which accounts for the superior noise performance of the CSLNA configuration. Its minimum noise factor including channel thermal noise and induced gate noise is given by

$$F_{\text{min,CSLNA}} = 1 + \frac{\gamma}{\alpha} \left(\frac{\omega_0}{\omega_T} \right) \frac{2\delta\alpha^2}{5\gamma} Q_{\text{opt}} \tag{2}$$

where $Q_{\text{opt}} = \sqrt{1 + 2|c|\sqrt{5\gamma/\delta\alpha^2} + (5\gamma/\delta\alpha^2)}$ [3], α, γ, and δ are bias-dependent parameters [5], c is the correlation coefficient between the gate noise and drain noise of the MOSFET, and ω_0 is the operating frequency.

In contrast to the CSLNA, a CGLNA [Fig. 1(b)] uses a parallel resonant network to match the input impedance at resonance $(1/g_m)$ to 50 Ω. The overall input admittance is

$$Y_{\text{in,CGLNA}} \approx g_m + s(C_{\text{pad}} + C_{gs}) + \frac{1}{sL_s} \qquad (3)$$

where the body effect of the nMOS device has been neglected.

The noise factor including the channel noise and induced gate noise is

$$F_{\text{CGLNA}} = 1 + \frac{4kT\gamma g_{d0}\Delta f}{\frac{4kT}{R_s\Delta f}} \left(\frac{1}{g_m R_S}\right)^2$$
$$+ \frac{4kT\delta g_g\Delta f}{\frac{4kT}{R_s\Delta f}} \left(\frac{1}{g_m R_S}\right)^2. \qquad (4)$$

With $g_g = (\omega C_{gs})^2/5g_{d0}$ and an input matching condition of $g_m R_S \approx 1$

$$F_{\text{CGLNA}} = 1 + \frac{\gamma}{\alpha} + \frac{\delta\alpha}{5}\left(\frac{\omega_0}{\omega_T}\right)^2 \approx 1 + \frac{\gamma}{\alpha} \qquad (5)$$

where the third term, accounting for the gate noise contribution, is usually negligible. Two important conclusions are drawn from the analysis and discussion above.

A. Contribution of Gate Noise to NF

The contribution from gate noise to the overall noise factor, F_{CGLNA}, is usually insignificant. For example, to a first order, it can be shown that even for an operating frequency $\omega_0/\omega_T \sim 0.5$, its contribution to the overall F_{CGLNA} is less than 5%. In a CSLNA, however, the series RLC tank enhances the gate noise contribution to F_{CSLNA} by its Q factor. If the contributions of gate and correlated noise sources are not considered properly in selecting the Q value, a higher overall NF may result. Inaccurate and incomplete modeling of the gate and correlated noise sources usually renders this selection problematic in simulations; only measured results are dependable. In contrast, simulation of common-gate topologies does not suffer from large inaccuracies in gate noise modeling.

B. Noise Factor at High Frequencies

F_{CGLNA} is weakly dependent on ω_0/ω_T while F_{CSLNA} is linear in ω_0/ω_T. Thus, the CGLNA stage has fundamentally superior noise performance for a higher operating frequency ratio, ω_0/ω_T. This point is further developed in Section IV.

One advantage of the series resonant tank at the CSLNA input is increased effective transconductance [3]. In fact, under a matched input condition, it can be shown that

$$G_{m,\text{CSLNA}} = g_m Q = \frac{1}{2R_S}\left(\frac{\omega_T}{\omega_0}\right) = G_{m,\text{CGLNA}}\left(\frac{\omega_T}{\omega_0}\right). \qquad (6)$$

Thus, at low operating frequencies where $\omega_T/\omega_0 \approx 5 - 10$, CSLNA has higher gain than CGLNA. However, a high Q input match also makes CSLNA more sensitive to process, voltage, and temperature (PVT) variations [6] and reduces its linearity. A CSLNA also exhibits inferior reverse isolation and stability

TABLE I
ADVANTAGES (+) AND DISADVANTAGES (-) OF LNA STAGES

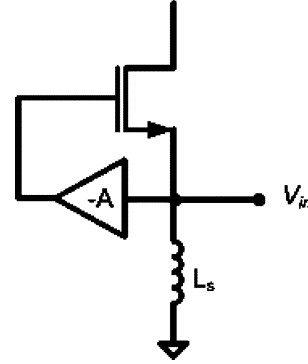| Parameter	CSLNA	CGLNA
Noise Factor	+	-
Effective G_m	+	-
Parasitic Sensitivity	-	+
Input Matching	-	+
DC power	-	+
Reverse Isolation	-	+

Fig. 2. Basic CGLNA stage with g_m-boosting feedback amplifier.

due to the Miller effect originating from the feedforward capacitor C_{gd}.

Table I compares the two basic LNA topologies. It clearly indicates that a CGLNA topology is more attractive if its effective g_m is increased and its noise factor is decreased. A design technique for meeting these objectives is described in the next section.

III. GENERAL g_m-BOOSTING TECHNIQUE

Ignoring the effects of gate noise, (5) can be expressed in greater detail as

$$F_{\text{CGLNA}} = 1 + \frac{4kT\gamma g_{d0}\Delta f}{\frac{4kT}{R_s\Delta f}}\left(\frac{1}{g_m R_S}\right)^2$$
$$= 1 + \frac{\gamma}{\alpha}\frac{g_m}{\frac{1}{R_s}}\left(\frac{1}{g_m R_S}\right)^2$$
$$= 1 + \frac{\gamma}{\alpha}\frac{g_{mi}}{\frac{1}{R_s}}\left(\frac{1}{G_{m,\text{eff}} R_S}\right)^2. \qquad (7)$$

In (7), g_{mi} represents the small-signal transconductance of the MOSFET and $G_{m,\text{eff}}$ is the effective transconductance of the active stage at the source terminal. Stated another way, g_{mi} is related to channel thermal noise and $G_{m,\text{eff}}$ to input matching. In a conventional CGLNA, $G_{m,\text{eff}} = g_{mi} = 1/R_s$ constrains the lower bound on the noise factor to $(1 + \gamma/\alpha)$. Note, however, that if $G_{m,\text{eff}}$ is boosted independently by modifying the input matching condition, F_{CGLNA} is reduced. This is accomplished (Fig. 2) using a g_m-boosting scheme wherein inverting amplification, A, is introduced between the source and gate terminals so that $G_{m,\text{eff}} = (1 + A)g_{mi}$ [3]. The resulting increase in the effective transconductance brings at least two significant improvements to the CGLNA topology.
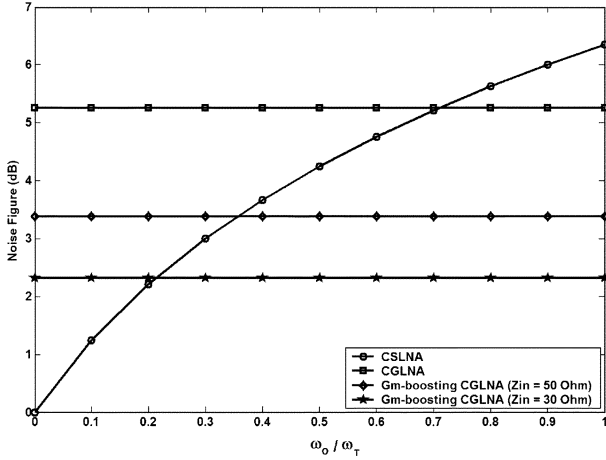
Fig. 3. Noise figure versus ω_0/ω_T for various LNA topologies.

A. Noise Factor

The noise factor now becomes

$$F_{\text{CGLNA},g_m-\text{boosting}} = 1 + \frac{\gamma}{\alpha} \frac{g_{mi}}{\frac{1}{R_s}} \left(\frac{1}{(1+A)g_{mi}R_S}\right)^2$$

$$= 1 + \frac{\gamma}{\alpha} \frac{1}{(1+A)} \qquad (8)$$

using the new input matching condition $1/R_s = (1+A)g_{mi}$. Thus, $(F-1)$ in (8) is reduced by the factor $(1+A)$. Of course, this analysis assumes that the amplification stage itself does not contribute significant noise, which, in turn, motivates a passive implementation of A.

Fig. 3 plots the NF as a function of ω_0/ω_T of the g_m-boosted CGLNA configuration. The noise factors of the conventional CSLNA and CGLNA circuits are also plotted for comparison. The g_m-boosted CGLNA stage exhibits superior noise performance compared to the CSLNA for $\omega_0/\omega_T > 0.35$.

In many cases, an exact input match to 50 Ω for the LNA is not absolutely necessary to meet practical specifications. For example, setting the input impedance $(1/(1+A)g_{mi})$ to 30 Ω results in $S_{11} \approx -12$ dB, which means that less than 10% of the incident power is reflected [7]. The beauty of this tradeoff is that it allows g_{mi} to be increased to further reduce the noise factor. As illustrated in Fig. 3, designing for a 30 Ω input impedance allows the g_m-boosting CGLNA to outperform the CSLNA for $\omega_0/\omega_T > 0.2$.

B. Power Consumption

The decoupled input matching condition of the g_m-boosted CGLNA also means that $g_{mi} = 1/(1+A)R_s$. Now the intrinsic transconductance is $(1+A)$ times less than that of the conventional CGLNA, which reduces the power consumption by the same factor.

IV. CAPACITOR CROSS-COUPLED CGLNA

One possible way to achieve passive inverting amplification in the g_m-boosted CGLNA is shown in Fig. 4 wherein a differential topology allows the differential active devices to be capacitor cross-coupled [2].
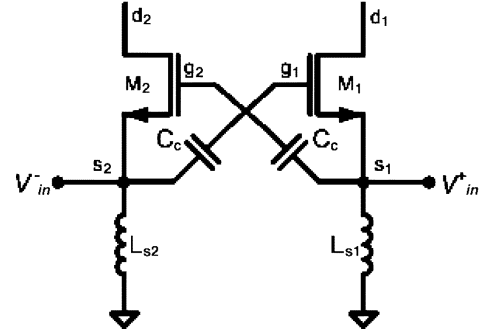

Fig. 4. Capacitor cross coupling in a differential CGLNA.

The inverting amplification value, A, for the topology of Fig. 4 is approximately given by the capacitor voltage division ratio

$$A = \frac{C_c}{C_c + C_{gs}} = \frac{1}{1 + \frac{C_{gs}}{C_c}} \qquad (9)$$

which, in turn, gives an effective transconductance of

$$G_{m,\text{eff}} = \left(\frac{C_{gs} + 2C_c}{C_{gs} + C_c}\right) g_{mi} \qquad (10)$$

and an approximate noise factor of

$$F_{\text{CGLNA,CCC}} \approx 1 + \frac{\gamma}{\alpha} \left(\frac{C_{gs} + C_c}{C_{gs} + 2C_c}\right). \qquad (11)$$

Thus, $C_C \gg C_{gs}$ results in $A \approx 1$ and

$$G_{m,\text{eff}} \approx 2g_{mi} \qquad (12a)$$

$$F_{\text{CGLNA,CCC}} \approx 1 + \frac{\gamma}{2\alpha}. \qquad (12b)$$

Hence, the noise factor is reduced and the effective transconductance is increased with a concomitant decrease in power dissipation as described earlier.

V. DESIGN AND MEASUREMENT RESULTS

Fig. 5 shows a CCC-CGLNA designed to operate at 6.0 GHz in a 180-nm RF CMOS process. Differential transistors M_1 and M_2 are biased and sized for $1/2g_{mi} = 40\,\Omega$. Although an input impedance of 30 Ω enables higher gain and lower NF, this design is matched to 40 Ω to maintain a safety margin on S_{11} to account for possible modeling and simulation errors. Since the gates of the input transistors are not connected to an ac ground as in the conventional case, cascode devices M_3 and M_4 are added to improve the reverse isolation. The capacitors (C_C) are 4.7 pF and are used to cross couple M_1 and M_2. On-chip inductors L_s are used to tune out the total capacitances at the source nodes including pad capacitances. A tapped-capacitor impedance match is used at the output to allow incorporation of the pad capacitances into C_p. The simulated Q values of on-chip inductors L_s and L_d are approximately 10.

Fig. 6 shows measured S_{11} and S_{22} input and output matching characteristics, respectively. S_{11} is less than -10 dB at 6.0 GHz and above owing to the inherent broad-band input match of the common-gate topology. S_{22} is -7.3 dB at
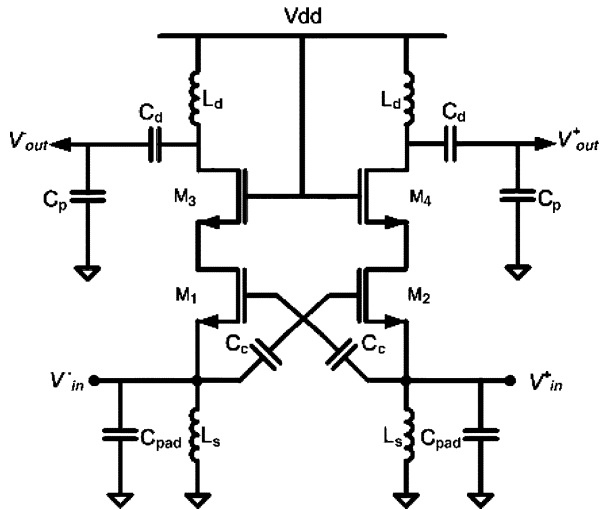
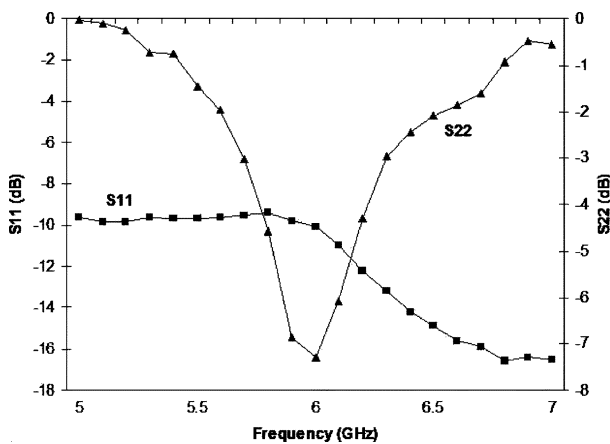Fig. 5.   Complete capacitor cross-coupled differential CGLNA stage.

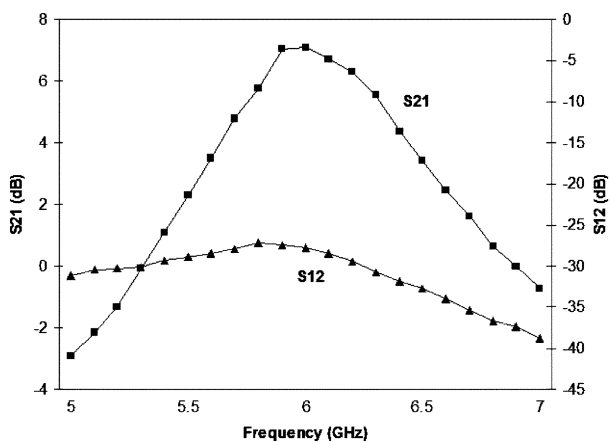Fig. 6.   Measured S_{11} and S_{22}.

Fig. 7.   Measured S_{21} and S_{12}.

6.0 GHz. This is about 5 dB poorer than expected from the simulated results and is probably due to an overestimation of the Q of L_d.

The measured power gain S_{21} and reverse isolation S_{12} plots are displayed in Fig. 7. The maximum power gain of 7.1 dB at 6.0 GHz is lower (by 2 dB) than expected from the simulation results due to imperfect output matching.
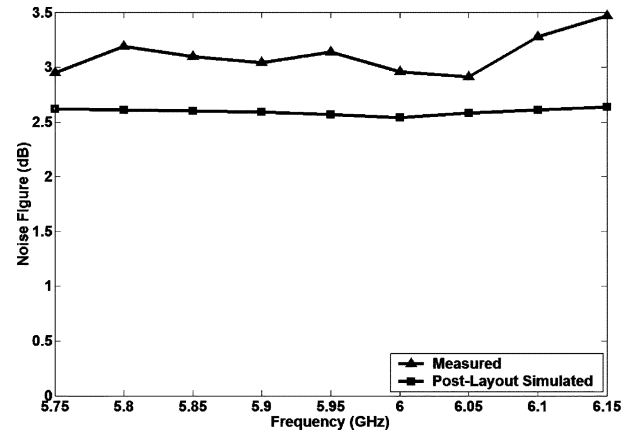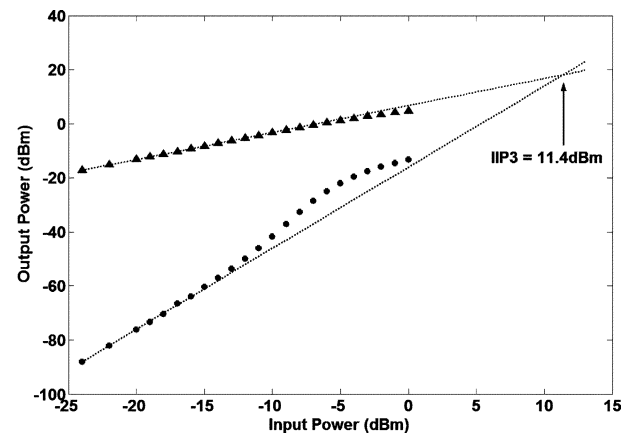

Fig. 8.   Measured NF from 5.75–6.15 GHz.

Fig. 9.   Measured gain, IM3, and extrapolated IIP3 results.

A NF plot of the CCC-CGLNA is shown in Fig. 8. The fully integrated LNA achieves a NF of 2.97 dB at 6.0 GHz. This is an excellent NF value for a CGLNA topology, and it compares favorably with fully integrated CSLNA designs [8]. Note again that many common-source LNA circuits achieve excellent NFs at the cost of higher power consumption or the use of some off-chip matching components.

In order to verify the accuracy of the simulated NF value of a CGLNA, and to see the impact of induced gate noise to the overall NF, the measured value is compared to the simulated NF in the same plot (Fig. 8). For fair comparison, the CCC-CGLNA is re-designed so as to have its simulated S-parameters identical to the measured results. The parasitic resistances and capacitances are also extracted from the layout and taken into the account in simulation. Still some discrepancies between the simulated and measured results are observed. They might be attributed to measurement inaccuracies ($\sim$0.25 dB) and the effect of pads [9].

The third-order intercept point (*IP3*) is measured using a two-tone test with equal-amplitude 6.0- and 6.005-GHz signals. An excellent input-referred third-order intercept (*IIP3*) value of 11.4 dBm is obtained as shown in Fig. 9. It is noted here that the linearity experiences degradation with the increase in the input power above -12 dBm. A probable cause is the mixing of higher order terms into the IM3 product at larger input power levels. This, however, is not a cause for concern because the normal input power level at the input of the LNA is usually
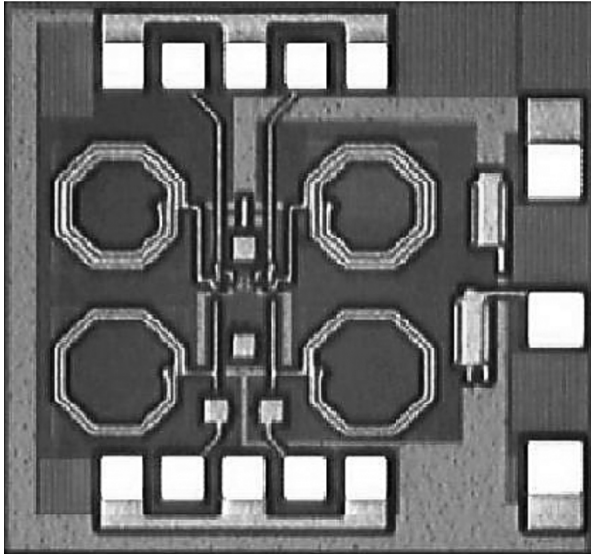
Fig. 10.   Chip micrograph of the capacitor CCC-CGLNA.

TABLE II
MEASUREMENT RESULTS FOR CCC-CGLNA

Parameter	Measured Results
Frequency	6.0GHz
Noise Figure	3.0dB
Gain (S_{21})	7.1dB
IIP3	11.4dBm
DC current	2x1.8mA
Power Supply	1.8V
Technology	180nm CMOS

much smaller [10]. The capacitor cross-coupled g_m-boosted CGLNA draws 3.6 mA (2 × 1.8 mA) of dc bias current from a single 1.8-V power supply. A chip micrograph is shown in Fig. 10. Implemented in a 180-nm 48 GHz f_T RF CMOS process, the total die area including pads is 975 μm × 975 μm. Table II summarizes the measured results.

VI. CONCLUSION

A g_m-boosting technique to reduce the power consumption and improve the NF of a CGLNA is described. A capacitor cross-coupled LNA is presented as an implementation of the general technique. The fully integrated differential LNA consumes 3.6 mA from 1.8 V and attains a measured NF of 3.0 dB at 6.0 GHz. The proposed technique makes the CG topology attractive for low-power and high-frequency fully integrated designs.

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