A Capacitor-Less CMOS Active Feedback Low-Dropout Regulator With Slew-Rate Enhancement for Portable On-Chip Application

Edward N. Y. Ho and Philip K. T. Mok, *Senior Member, IEEE*

***Abstract*—A low-dropout regulator for on-chip application with active feedback and a slew-rate enhancement circuit to minimize compensation capacitance and speed up transient response is presented in this brief. The idea has been modeled and experimentally verified in a standard 0.35-μm CMOS process. The total compensation capacitance is 7 pF. From experimental results, the implemented regulator can operate from a supply voltage of 1.8–4.5 V with a minimum dropout voltage of 0.2 V at a maximum 100-mA load and $I_{\rm Q}$ of 20 μA.**

***Index Terms*—Active feedback, analog circuits, capacitor-less low dropout (LDO), dc–dc regulator, low-dropout (LDO) voltage regulators.**

I. Introduction

LOW-DROPOUT (LDO) regulators are widely used in integrated on-chip power management applications in mobile and battery-powered devices requiring clean supply voltage and small device area [1], [2]. Minimizing quiescent current and dropout voltage while maintaining good regulation and fast response is the main issue of the LDO regulator design. For portable applications, off-chip components such as output filtering capacitors should be minimized to reduce printed-circuit-board layout space and speed up manufacturing process. However, to provide good performance, current LDO regulators usually require off-chip filtering capacitors ranging from 1 to 10 μF [3]–[7] for a stable output voltage. For on-chip application, this amount of capacitance cannot be integrated in silicon. An output capacitor-less LDO regulator is needed for this application.

During load transients, the output capacitor acts as a charge buffer to absorb (provide) the current difference between the load and the power transistor. Reduction of the output filtering capacitor will lead to severe output voltage changes during fast load current transients, which the power-line-sensitive devices supplied by the LDO regulator cannot tolerate. Since the output capacitor is small, a dominant pole will no longer be located at the output node, unlike the typical LDO regulators.

Manuscript received July 16, 2009; revised October 5, 2009. First published January 22, 2010; current version published February 26, 2010. This work was supported in part by the Research Grant Council of Hong Kong SAR Government, China, under Project 617707. This paper was recommended by Associate Editor G. A. Rincon-Mora.

The authors are with the Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Kowloon, Hong Kong (e-mail: eemok@ece.ust.hk).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCSII.2009.2038630

Recently, a lot of researchers have proposed various strategies to produce output capacitor-less LDO regulators [10]–[12]. Many of them are based on pole-splitting compensation approach [10], [12]. They view the power MOSFET in an LDO regulator as an amplifier, and, therefore, LDO regulators are variations of two- or three-stage amplifiers. The differences are that an LDO regulator has a large gate capacitor and gain variation at the power MOSFET at different load current conditions. This creates problems with stability over different loading current levels and causes serious overshoots/undershoots during fast load transients. To solve these problems, two approaches are proposed: 1) Active feedback compensation strategy is used [8] to provide higher loop response and smaller total on-chip compensation capacitors, and 2) slew rate enhancement circuitry is implemented to provide an ultrafast feedback response loop to cater for output variations during output transient dynamics.

In this brief, a low quiescent current small on-chip capacitance fast load-transient response capacitor-less LDO regulator is presented. The concept of the proposed LDO regulator is discussed in Section II. Circuit implementation and experimental results are given in Sections III and IV, respectively. The conclusion is given in Section V.

II. Proposed LDO Regulator Structure

Fig. 1(a) displays a conventional three-stage pole-splitting LDO regulator structure. It consists of one two-stage error amplifier, a pole-splitting network, and a power transistor, which can be treated as an output gain stage to the whole feedback network. To drain large output current, the power transistor has to be large compared with the internal transistors. Therefore, the capacitance at the gate of the power transistor is very large. For on-chip power management purposes, the power line capacitance will be small and in the range of tens to hundreds of picofarads. The response time of the LDO regulator will be slew-rate-limited at the gate of the power transistor.

Fig. 1(b) illustrates the proposed LDO regulator design with fast transient response. A high-speed loop that consists of $G_{\rm ma}$ and $G_{\rm mx}$ has been introduced into the system to provide extra current to charge and discharge the gate capacitor. Therefore, response time can be much quicker. There are several requirements for the high-speed loop: low power, easy implementation, and small in area. The accuracy of the loop is not a major concern because the loop is used to provide temporary voltage regulation during transient moments. The steady line and load regulation performance is determined by the main high-gain loop.

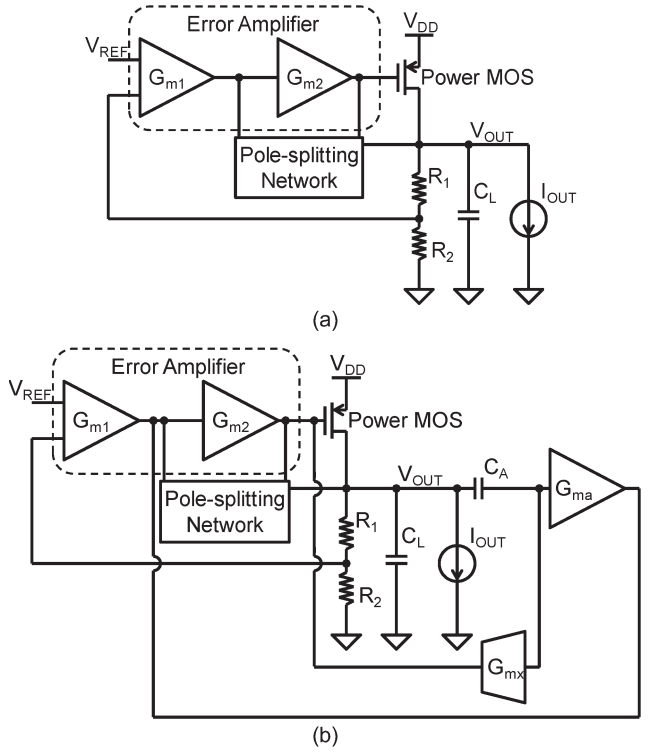

Fig. 1. (a) Conventional LDO design. (b) Proposed LDO design.

The high-speed feedback loop will also introduce a stability problem because both the high-gain and high-speed loops regulate the output voltage at the same time. As a result, a complex pole will be generated. This will significantly degrade the stability of the design. The problem is even worse when $I_{\rm OUT}$ is small, and this must be taken into consideration. To deal with the phenomenon, we have to push the complex pole beyond the unity gain bandwidth (UGF) of the LDO regulator and control the quality factor to be ideally equal to $1/\sqrt{2}$ [9].

III. Circuit Implementation

Here, the small signal stability of the proposed LDO regulator and transient optimized implementation are considered.

A. Small Signal Analysis

The open-loop small signal model of the proposed LDO regulator is shown in Fig. 2. It consists mainly of seven blocks: a first-stage amplifier, a second-stage amplifier, an output power transistor, an active feedback block, a slew-rate enhancement block, a feedforward block, and a dynamic feedforward block. The dc gain of the LDO regulator is given by the product of the gain of the first-stage amplifier, the second-stage amplifier, and the power transistor. The active feedback compensation capacitor $C_{\rm a}$ forms the dominant pole of the whole system. The active feedback block is effectively operating similar to a signal multiplier to magnify the signal passing through $C_{\rm a}$ to a larger signal [3]. This will effectively enable the reduction of the capacitor value of $C_{\rm a}$. The slew-rate enhancement block is

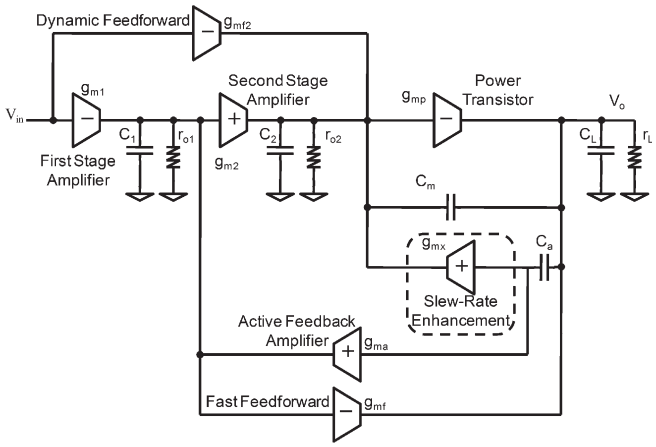

Fig. 2. Model of the proposed LDO.

designed to be kept inactive during steady state. The dynamic feedforward path $g_{\rm mf2}$ enhances the transient with a high-frequency right-half-plane zero, which is higher than the UGF and does not influence the overall stability [9]. Both modules can be neglected in the stability analysis for simplicity. To derive the open-loop transfer function $A_{\rm V}(s) = V_{\rm O}/V_{\rm IN}$ of the LDO regulator, the following assumption has been set up.

1) Input resistance $r_{\rm a}$ of the active feedback amplifier is equal to the inverse of the transconductance $g_{\rm ma}$. The compensation capacitors $C_{\rm a}$ and $C_{\rm m}$ are larger than the internal node capacitors C_1 and C_2.
2) Gains of the first-stage amplifier, the second-stage amplifier, and the active feedback amplifier are much larger than 1.
3) The slew-rate enhancement block can be viewed as an inactive path during stability analysis because the block only functions during the output transient.
4) To simplify the calculation, $C_{\rm m}$ and $C_{\rm a}$ are set in equal value.

As demonstrated in (1), shown at the bottom of the page, where

$$A_{\rm dc} = g_{\rm m1} r_{\rm o1} g_{\rm m2} r_{\rm o2} g_{\rm mp} r_{\rm L} \text{ and } p_{-3{\rm db}} = C_{\rm a} g_{\rm m2} g_{\rm mp} r_{\rm o1} r_{\rm o2} r_{\rm L}$$

the proposed system presents one dominant pole, a pair of complex poles, and one left-half-plane zero.

Since the loading condition will dramatically change the value of $g_{\rm mp}$ (the transconductance of the power transistor) and $r_{\rm L}$, the whole operating range has been divided into three different operating conditions and analyzed individually.

1) Heavy-load condition (above 10 mA).
   With large loading current, $g_{\rm mp}$ is large, but $g_{\rm mp} r_{\rm L}$ is small. The denominator of the transfer function can be approximately reduced to the following form:

$$(1 + sC_{\rm a} g_{\rm m2} g_{\rm mp} r_{\rm o1} r_{\rm o2} r_{\rm L}) \times \left[1 + \frac{C_1}{g_{\rm m2}}\left(1 + \frac{1}{g_{\rm mp} r_{\rm L}}\right)s + \frac{C_{\rm a} C_1}{g_{\rm ma} g_{\rm m2}}\left(1 + \frac{1}{g_{\rm mp} r_{\rm L}}\right)s^2\right]. \quad (2)$$

$$A_{\rm V}(s) = \frac{V_{\rm o}}{V_{\rm in}} \approx \frac{A_{\rm dc}(1 + sC_{\rm a} r_{\rm a})}{\left(1 + \frac{s}{p_{-3{\rm db}}}\right)\left[1 + \left(\frac{C_1}{g_{\rm m2}} + \frac{C_1}{g_{\rm m2} g_{\rm mp} r_{\rm L}} + \frac{C_{\rm a}(g_{\rm mf} - g_{\rm m2})}{g_{\rm m2} g_{\rm mp}}\right)s + \left(\frac{C_{\rm a} C_1}{g_{\rm ma} g_{\rm m2}} + \frac{C_{\rm a} C_1}{g_{\rm ma} g_{\rm m2} g_{\rm mp} r_{\rm L}} + \frac{C_1 C_{\rm L}}{g_{\rm m2} g_{\rm mp}}\right)s^2\right]} \quad (1)$$

The corresponding nondominant pole and Q factors are

$$|p_{\mathrm{H2,3}}| = \sqrt{\frac{g_{\mathrm{ma}} g_{\mathrm{m2}} g_{\mathrm{mp}} r_{\mathrm{L}}}{C_{\mathrm{a}} C_1 (1 + g_{\mathrm{mp}} r_{\mathrm{L}})}} \tag{3}$$

$$Q_{\mathrm{H}} = \sqrt{\frac{C_{\mathrm{a}} g_{\mathrm{m2}} g_{\mathrm{mp}} r_{\mathrm{L}}}{g_{\mathrm{ma}} C_1 (1 + g_{\mathrm{mp}} r_{\mathrm{L}})}}. \tag{4}$$

2) Medium-load condition (around 100 μA–10 mA).

The transconductance of the power transistor decreases, and the structure starts to work as a three-stage amplifier with large g_{mp}. Therefore, g_{mp} is assumed to be large compared with g_{m1} and g_{m2}, while $g_{\mathrm{mp}} r_{\mathrm{L}}$ increases to a large value. The denominator of the transfer function is approximately reduced to

$$(1 + sC_{\mathrm{a}} g_{\mathrm{m2}} g_{\mathrm{mp}} r_{\mathrm{o1}} r_{\mathrm{o2}} r_{\mathrm{L}}) \left[1 + \frac{C_1}{g_{\mathrm{m2}}} s + \frac{C_1}{g_{\mathrm{m2}}} \left(\frac{C_{\mathrm{a}}}{g_{\mathrm{ma}}} + \frac{C_{\mathrm{L}}}{g_{\mathrm{mp}}} \right) s^2 \right] \tag{5}$$

with

$$|p_{\mathrm{M2,3}}| = \sqrt{\frac{g_{\mathrm{ma}} g_{\mathrm{m2}} g_{\mathrm{mp}}}{C_1 (C_{\mathrm{a}} g_{\mathrm{mp}} + C_{\mathrm{L}} g_{\mathrm{ma}})}} \tag{6}$$

$$Q_{\mathrm{M}} = \sqrt{\frac{g_{\mathrm{m2}} (g_{\mathrm{mp}} C_{\mathrm{a}} + C_{\mathrm{L}} g_{\mathrm{ma}})}{g_{\mathrm{ma}} g_{\mathrm{mp}} C_1}}. \tag{7}$$

3) Light-load condition (below 100 μA).

The power transistor drain current decreases, and, eventually, the power transistor operates in the cutoff region. g_{mp} is assumed to be small, while $g_{\mathrm{mp}} r_{\mathrm{L}}$ becomes very large. In this case, the denominator of the transfer function can be simplified to

$$(1 + sC_{\mathrm{a}} g_{\mathrm{m2}} g_{\mathrm{mp}} r_{\mathrm{o1}} r_{\mathrm{o2}} r_{\mathrm{L}}) \times \left[1 + s \left[\frac{C_{\mathrm{a}} (g_{\mathrm{mf}} - g_{\mathrm{m2}})}{g_{\mathrm{m2}} g_{\mathrm{mp}}} + \frac{C_1}{g_{\mathrm{m2}}} \right] + s^2 \frac{C_1 C_{\mathrm{L}}}{g_{\mathrm{m2}} g_{\mathrm{mp}}} \right] \tag{8}$$

with

$$|p_{\mathrm{L2,3}}| = \sqrt{\frac{g_{\mathrm{m2}} g_{\mathrm{mp}}}{C_1 C_{\mathrm{L}}}} \tag{9}$$

$$Q_{\mathrm{L}} = \frac{\sqrt{C_1 C_{\mathrm{L}} g_{\mathrm{m2}} g_{\mathrm{mp}}}}{C_{\mathrm{a}} (g_{\mathrm{mf}} - g_{\mathrm{m2}}) + C_1 g_{\mathrm{mp}}}. \tag{10}$$

From the above three cases, it can be observed that the stability of medium and light loads is the most difficult to achieve because of the large overall gain of the LDO regulator and the closer proximity to the unity gain frequency of the second pole. Observing the complex pole and quality factor expression in medium-load and light–load conditions (6), (7), (9), and (10), we may conclude that, in general, we can increase g_{ma}, g_{mf}, and C_{a} to stabilize the LDO regulator, that is, by setting the complex pole to twice the gain bandwidth with quality factor equal to $1/\sqrt{2}$ [9].

In the medium-load condition, it gives

$$C_{\mathrm{a}} = \frac{\sqrt{2} g_{\mathrm{m1}} C_1}{g_{\mathrm{m2}}}. \tag{11}$$

In light load, the value of C_{a} is given by

$$C_{\mathrm{a}} = \frac{\sqrt{2 C_1 C_{\mathrm{L}} g_{\mathrm{m2}} g_{\mathrm{mp}}} - C_1 g_{\mathrm{mp}}}{(g_{\mathrm{mf}} - g_{\mathrm{m2}})}. \tag{12}$$

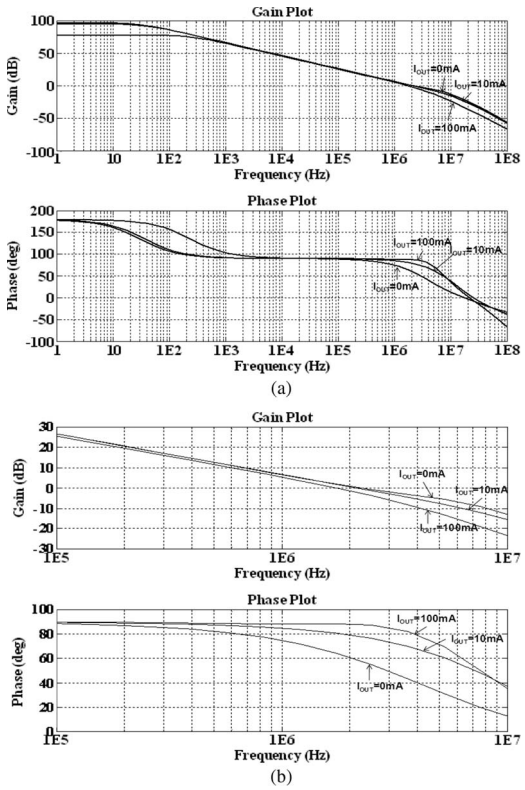

Fig. 3. (a) Open-loop response of the proposed LDO at $V_{\mathrm{DD}} = 1.8$ V and $V_{\mathrm{OUT}} = 1.6$ V. (b) Zoomed-in view of the open-loop response.

Together with the stability condition of light load of

$$g_{\mathrm{mf}} > g_{\mathrm{m2}} \quad \text{and} \quad \sqrt{2 C_1 C_{\mathrm{L}} g_{\mathrm{m2}} g_{\mathrm{mp}}} > C_1 g_{\mathrm{mp}} \tag{13}$$

the values of C_{m}, C_{a}, g_{ma}, and g_{mf} can be found.

In heavy-load and medium-load conditions, both C_{a} and g_{ma} may be used to achieve stability with high UGF. C_{a} can be used to locate the dominant pole location with increments of g_{ma} to decrease the complex pole peaking. In the light-load range, g_{ma} is no longer effective in decreasing the complex pole peaking. g_{mf} should be increased to suppress the Q value at the expenses of extra quiescent current draining from the power transistor to the ground.

The location of the left-half-plane zero is required to be set outside the UGF in order not to influence the stability of the proposed design. To fulfill the stability condition in light load, (13) has to be satisfied. The zero will be effectively located at four times of the UGF. The extra phase improvement by the zero is [8]

$$\tan^{-1} \left(\frac{g_{m1}}{g_{ma}} \right) = \tan^{-1} \left(\frac{1}{4} \right) = 14^{\circ}. \tag{14}$$

An open-loop-gain simulation has been performed to study the stability of the proposed LDO regulator. The simulation is based on a 0.35-μm CMOS model from Austria Mikro System Group (AMS). The power line is modeled as a resistor in parallel with a capacitor of 100 pF. C_{a} and C_{m} are chosen to be 1 and 6 pF, respectively. To guarantee stability for loading current down to zero, g_{mf} has been set to be three times of g_{m2}. The g_{mf} current also sets the minimum current passing through the power transistor and its minimum g_{mp}. From the simulation results in Fig. 3, the proposed LDO regulator is stable for load

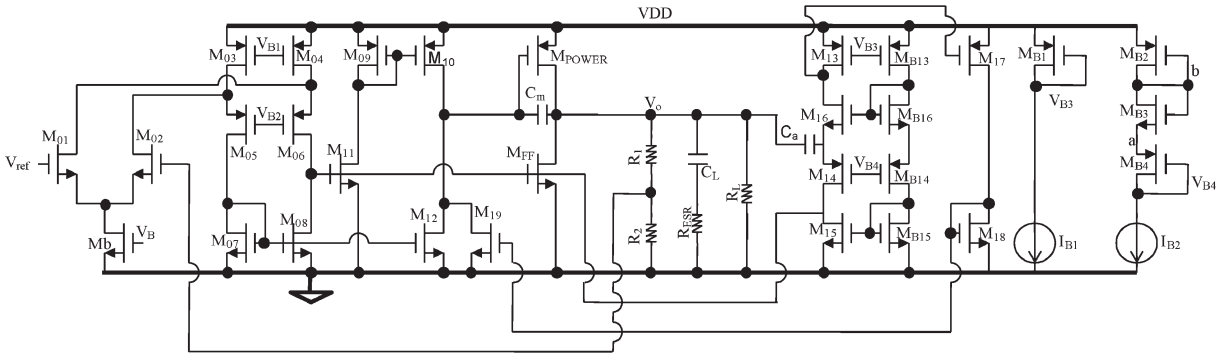

Fig. 4. Schematic of the proposed LDO.

current values ranging from 0 to 100 mA with a phase margin of more than 60°.

B. Transient Optimized Implementation

The transistor-level implementation of the proposed active-feedback LDO regulator with slew-rate enhancement is shown in Fig. 4. Transistors M_{01} to M_{08} form the first-stage amplifier, while M_{09} to M_{11} form the second-stage positive $g_{\rm m}$ amplifier. The power transistor is labeled as $M_{\rm POWER}$. The fast feedforward path is constructed by $M_{\rm FF}$ for control of the quality factor and reduction of complex poles peaking. The active feedback amplifier is constructed by $C_{\rm a}$ and M_{14}. M_{16} to M_{19} form the slew-rate enhancement block for transient signal improvement. $C_{\rm m}$ and $C_{\rm a}$ are the required compensation capacitors fabricated on-chip. R_1 and R_2 are the resistive feedback network.

Ensuring wide UGF of the regulator does not necessarily ensure a fast LDO regulator design because the response will be slew-rate-limited at the gate of the power transistor. This will be more severe in the case of large maximum output current and small quiescent current. To solve the problem, a careful construction of fast feedforward and nonlinear slew-rate enhancement has been implemented.

In the proposed realization, the fast feedforward path is formed by $M_{\rm FF}$ with the drain connected to $V_{\rm O}$ and the gate connected to the input of the second-stage amplifier. Effectively, it forms a weak push–pull output stage. One of the considerations of a push–pull output is the difficulties in the control of the quiescent current. In the proposed design, the drain current of fast feedforward transistor $M_{\rm FF}$ is controlled at about 4 μA across different supply voltages and loading conditions in the steady state. This can be achieved because the gate of $M_{\rm FF}$ is connected to the input of the second-stage amplifier. Thus, the drain current of $M_{\rm FF}$ will be multiples of M_{11}, which can be accurately controlled. The weak push–pull output can increase the current draining capability at the $V_{\rm O}$ node and reduce overshoot during the transient. The maximum draining capability of $M_{\rm FF}$ is controlled by the gains M_{14} and $M_{\rm FF}$. In the proposed design, the simulated $M_{\rm FF}$ drain current during the transient can be increased up to the milliampere range. Furthermore, the existence of a draining path can extend the stable output current of the LDO regulator down to zero because the minimum drain current of power transistor $M_{\rm POWER}$ is guaranteed.

A slew-rate enhancement feature has been implemented to reduce the undershoot of the proposed LDO regulator. During the output transient, M_{17} will be turned on, and the slew-rate enhancement circuit will be activated when the undershoot appears. The resulting extra path consisting of $g_{\rm mx}$ can provide extra current for discharging the large gate capacitor of $M_{\rm POWER}$.

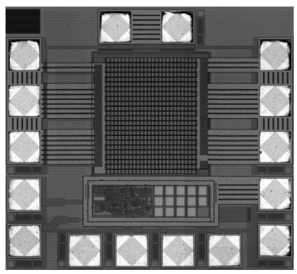

Fig. 5. Chip micrograph of the proposed LDO.

As stated during the open-loop analysis section, the slew-rate enhancement block is normally inactive during steady states and only provides current in the transient situation. This will keep the drain current of M_{17} to M_{19} low during the steady-state operation. To ensure stability after the output current transient, the maximum transconductance formed by M_{17} to M_{19} must be set smaller than $g_{\rm m2}$. In the design, it is achieved by restricting the maximum drain current of M_{19} to be smaller than M_{12} by reducing the size of M_{19}.

To ensure that M_{17} is not turned on during the steady state, $V_{\rm B4}$ has to be carefully chosen to be high enough so that $V_{\rm SG}$ of M_{17} is normally less than the threshold voltage of M_{17}. The realization of $V_{\rm B4}$ is shown in Fig. 4. By assuming $|V_{\rm TP}| = V_{\rm TN} = V_{\rm T}$ and neglecting the body effect

$$V_{\rm B4} = V_{\rm DD} - V_{\rm SG(MB2)} - V_{\rm GS(MB3)} - V_{\rm SG(MB4)}. \quad (15)$$

The gate voltage of M_{17} will be

$$V_{\rm B4} + V_{\rm SG(M14)} + V_{\rm DSSAT(M16)}. \quad (16)$$

Therefore, $V_{\rm SG(MB2)} + V_{\rm GS(MB3)} + V_{\rm SG(MB4)} - V_{\rm SG(M14)} - V_{\rm DSSAT(M16)}$ has to be smaller than $V_{\rm T}$. To achieve this, $I_{\rm B2}$ needs to be set smaller than $I_{\rm B1}$, and $M_{\rm B2}$ to $M_{\rm B4}$ have to be biased at the subthreshold region. In the proposed design, $V_{\rm G(M17)}$ is set only 400 mV below $V_{\rm DD}$ (with $V_{\rm TP} \sim -700$ mV) to counter for process variation.

IV. Experimental Results

The proposed LDO regulator has been fabricated with AMS 2P4M 0.35-μm CMOS technology. The die photo is shown

TABLE I
PERFORMANCE SUMMARY

V_{DD}		1.8-4.5V
V_{DO}		0.2V
Output Current		0-100mA
I_Q	No load:	20μA@V_O=1.6V, V_{DD}=1.8V 36.1μA@V_O=3.1V, V_{DD}=3.3V
	Full load:	20.9μA@V_O=1.6V, V_{DD}=1.8V 37.7μA@V_O=3.1V, V_{DD}=3.3V
Line Regulation		57.4μV/mV@V_O=1.6V, I_{OUT}=100mA, V_{DD}=1.8-3.3V
Load Regulation		109μV/mA@V_O=1.6V, V_{DD}=1.8V
PSRR		40dB@10kHz

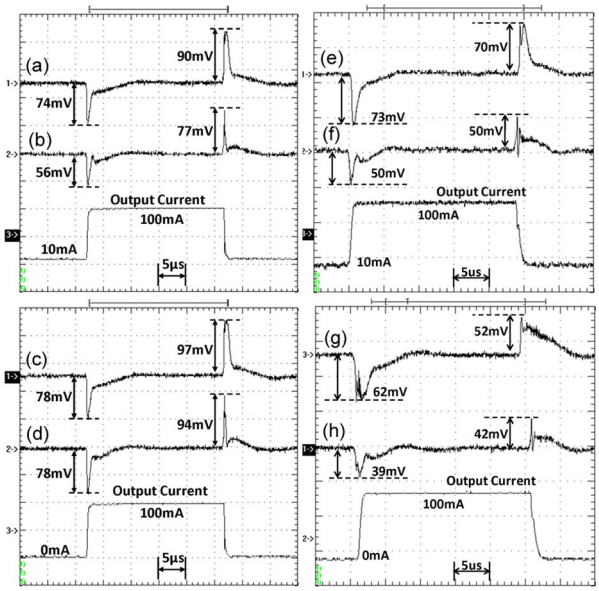

Fig. 6. Measured load transient with a 100-pF output capacitor. (a) $V_{\rm DD} = 1.8$ V, $V_{\rm O} = 1.6$ V. (b) $V_{\rm DD} = 3.3$ V, $V_{\rm O} = 3.1$ V. (c) $V_{\rm DD} = 1.8$ V, $V_{\rm O} = 1.6$ V. (d) $V_{\rm DD} = 3.3$ V, $V_{\rm O} = 3.1$ V. (e) $V_{\rm DD} = 1.8$ V, $V_{\rm O} = 1.6$ V. (f) $V_{\rm DD} = 3.3$ V, $V_{\rm O} = 3.1$ V. (g) $V_{\rm DD} = 1.8$ V, $V_{\rm O} = 1.6$ V. (h) $V_{\rm DD} = 3.3$ V, $V_{\rm O} = 3.1$ V.

TABLE II
COMPARISON OF RESULT

	Ref [10]	Ref [11]	Ref [12]	Ref [13]	Ref [14]	This work
Year	2003	2005	2007	2007	2008	2009
Technology [μm]	0.6	0.09	0.35	0.35	0.35	0.35
I_{OUT} [mA]	100	100	50	100	50	100
V_{DO} [mV]	200	300	200	200	200	200
V_{OUT} [V]	1.3	0.9	2.8	1	1	1.6
C_{COMP} [F]	12p	N.A.	21p	6p	N.A.	7p
C_{OUT} [F]	>20p	600p	0-100p	100p	>20p	100p
I_Q [mA]	0.038	6	0.065	0.1	0.095	0.02
Loop gain [dB]	90-110	>43	55-62	<50	<60	78-98
ΔV_{OUT}(full load) [mV]#	<100	90	<90	<50	≈180	<97
Settling Time [μs]	≈2	N/A	≈15	≈30	≈0.3	<9
Active Chip Area [mm^2]	0.307	0.0002	0.289	0.125	0.045	0.145
FOM* [ns]	38μ†	32m	234μ	50μ	136μ	19.4μ

* FOM = (C_{OUT}×ΔV_{OUT}×I_Q)/I_{MAX}^2[11] in capacitor-less condition.
† 100pF has been used to model output filtering capacitor
# Maximum output voltage overshoot/undershoot for fastest capacitor-less full load transient.

in Fig. 5 with an active area of 319 μm × 453 μm, excluding testing pads. The dc characteristics of the LDO regulator have been summarized in Table I. An off-chip 100-pF capacitor is added at the output to model the power line capacitance for all measurements. The quiescent current is measured by subtracting the loading current from the total input current.

Fig. 6 shows the measured load transient response of the fabricated LDO regulator. In waveforms (a–d), the loading current level changes between low and high within 100 ns. For waveforms (e–h), the loading current level changes in 1 μs. The output voltage fully recovers ($< 1\%$) in 9 μs. A performance comparison with recent published capacitor-less or capacitor-free LDO regulators is given in Table II.

V. CONCLUSION

An LDO regulator with an active feedback and slew-rate enhancement structure has been introduced, modeled, and experimentally verified. With the proposed technique, on-chip compensation capacitance is limited to 7 pF, and the minimum loading current is reduced to 0 μA. The output load transient variation of 0–100 mA can be recovered within 9 μs with a chip area of 0.145 mm^2 and a quiescent current of about 20 μA over a wide range of output current (0–100 mA).

REFERENCES

[1] H. Eul, "ICs for mobile multimedia communications," in *Proc. IEEE ISSCC Dig. Tech. Papers*, Feb. 2006, pp. 21–39.
[2] D. Evans, M. McConnell, P. Kawamura, and L. Krug, "SoC integration challenges for a power management/analog baseband IC for 3G wireless chipsets," in *Proc. Int. Symp. Power Semicond. Devices ICs*, May 2004, pp. 77–80.
[3] G. A. Rincon-Mora, "Active capacitor multiplier in Miller-compensated circuits," *IEEE J. Solid-State Circuits*, vol. 35, no. 1, pp. 26–32, Jan. 2000.
[4] C. K. Chava and J. Silva-Martinez, "A frequency compensation scheme for LDO voltage regulators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 6, pp. 1041–1050, Jun. 2004.
[5] I. P. Hsuan, C.-H. Cheng, C.-L. Chen, and T.-Y. Yang, "A CMOS low dropout regulator stable with any load capacitor," in *Proc. IEEE TENCON*, Nov. 2004, vol. 4, pp. 266–269.
[6] M. Al-Shyoukh, H. Lee, and R. Perez, "A transient-enhanced low-quiescent current low-dropout regulator with buffer impedance attenuation," *IEEE J. Solid-State Circuits*, vol. 42, no. 8, pp. 1732–1742, Aug. 2007.
[7] W.-J. Huang, S.-H. Lu, and S.-I. Liu, "A capacitor-free CMOS low dropout regulator with slew rate enhancement," in *Proc. Int. Symp. VLSI Des., Autom. Test*, Apr. 2006, pp. 1–4.
[8] H. Lee and P. K. T. Mok, "Active-feedback frequency-compensation technique for low-power multistage amplifiers," *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 511–520, Mar. 2003.
[9] H. Lee and P. K. T. Mok, "Advances in active-feedback frequency compensation with power optimization and transient improvement," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 9, pp. 1690–1696, Sep. 2004.
[10] K. N. Leung and P. K. T. Mok, "A capacitor-free CMOS low-dropout regulator with damping-factor-control frequency compensation," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1691–1702, Oct. 2003.
[11] P. Hazucha, T. Karnik, B. A. Bloechel, C. Parsons, D. Finan, and S. Borkar, "Area-efficient linear regulator with ultra-fast load regulation," *IEEE J. Solid-State Circuits*, vol. 40, no. 4, pp. 933–940, Apr. 2005.
[12] R. J. Milliken, J. Silva-Martinez, and E. Sanchez-Sinencio, "Full on-chip CMOS low-dropout voltage regulator," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 9, pp. 1879–1890, Sep. 2007.
[13] S. K. Lau, P. K. T. Mok, and K. N. Leung, "A low-dropout regulator for SoC with Q-reduction," *IEEE J. Solid-State Circuits*, vol. 42, no. 3, pp. 658–664, Mar. 2007.
[14] T. Y. Man, K. N. Leung, C. Y. Leung, P. K. T. Mok, and M. Chan, "Development of single-transistor-control LDO based on flipped voltage follower for SoC," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 5, pp. 1392–1401, Jun. 2008.