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A Novel Packaging Technique for Natural Voltage Balancing of Series-Connected SiC-MOSFETs

Luciano F. S. Alves, *Member, IEEE,* Pierre LEFRANC, Jean-Christophe CREBIER, *Member, IEEE*, Pierre-Olivier JEANNIN, and Benoit SARRAZIN, *Member, IEEE*

***Abstract*—This paper presents a novel packaging technique to improve the voltage sharing performances of series-connected SiC-MOSFETs. The proposed method takes advantage of the parasitic capacitance network introduced by the packaging dielectric isolation layers in order to reduce the voltage unbalancing across the series-connected devices. In a first step, the study carried out in this work explains how the parasitic capacitance networks introduced by the classic planar packaging and the gate drive circuits unbalance the voltages across the devices. Therefore, a new packaging concept is proposed in order to compensate the effects of the gate driver parasitic capacitances. The concept is introduced and analyzed thanks to equivalent models and time domain simulations. To verify the analysis, the voltage sharing between two series-connected 1.2 kV SiC-MOSFETs is tested in a pulse test setup. The experimental results confirm that the proposed voltage balancing technique can drastically improve the voltage sharing performance.**

***Index Terms*—Series-Connection, SiC-MOSFETs, Gate Driver, Parasitic Capacitances.**

I. Introduction

THE energy transition with grid integration of distributed energy resources, motor drive systems, and data centers leads to new challenges for power generation. Hence, the medium-voltage grid and direct medium-voltage applications are becoming increasingly important. Medium-voltage high-power converters have great potential for a wide variety of medium-voltage applications, such as high-voltage direct current (HVDC), medium-voltage direct current (MVDC), smart/super/micro-grids, drives for electrical machines, medium-voltage pulse generators for plasma applications, etc [1]. The common characteristic of the mentioned applications is the high voltage ratings and the search for maximizing the efficiency and output power capability of these critical systems, which can be achieved by increasing the blocking voltage of the devices. To this end, advancements in power electronic technology areas such as semiconductor devices and converter topologies have been investigated to improve the blocking voltage, power density, and efficiency, which can lower overall system cost and electricity consumption [2], [3].

Using series-connected devices is an attractive way for reaching higher blocking voltage with low-voltage devices. According to a study carried out in [4], using individual semiconductors in series results in lower cost, higher efficiency, and features better on-resistance and higher current density than using a single higher voltage device. However, series connection of power devices introduces multiple challenges related to the breakdown voltage, switching speed and switching transition location unbalance problems across each power device [5]–[8].

Substantial works have been done to analyze the causes of the power device voltage unbalance, and several techniques have been proposed to reduce this problem. The voltage unbalance is mainly due to device's parameters spread, gate-drive delay time jitter and parasitic elements, especially the one between each series connection potential and ground or reference potential [9]–[12]. Passive snubber circuits [13]–[17], active voltage clamping [18], [19], active gate control [12], [20]–[23] and natural self-voltage balancing techniques [10], [11], [24], [25], are used to improve the voltage sharing performance.

Passive snubber circuits are a common method applied for voltage balancing applications in industry due to its simple design and implementation. However, in medium-voltage high-frequency applications, passive methods lead to high power loss due to the stress of higher dv/dt rates on the passive components [26]. The cost and volume of the system can also be increased due to the additional passive components in the snubber circuits.

Active voltage clamping method is an effective way to ensure an acceptable static voltage sharing across the devices. However, the cost and volume of the system can be increased due to the additional passive components in the clamp circuits. Moreover, some methods require separate high-voltage rated auxiliary voltage sources to clamp each driving voltage at the desired voltage levels. Speed response can also become an issue, especially when high speed power devices are used, such as SiC devices.

Compared to passive techniques or voltage clamping methods, active gate control tends to provide less losses, and more compact footprint. On the other hand, active gate controls are more complex to be implemented.

The main idea of natural self-voltage balancing methods is to work on the parasitic capacitances of the switching cell to mitigate the voltage unbalancing across the series-connected devices. In such a way, passive or active clamping techniques can be sized down and ideally removed.

In [25], a compact series-connected SiC-MOSFET module using a single external gate driver is proposed. The proposed

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technique takes advantage of the layout capacitances related to the gate terminals to improve the voltage sharing performance and achieve the energy storage units. In [11], [27], a multi-step packaging concept was introduced for series-connected SiC-MOSFETs. The proposed natural self-voltage balancing concept considers optimal dielectric isolation for each device in the stack leading to a multi-step geometry. It has a significant impact on the parasitic capacitances introduced by the packaging structure, which is responsible for voltage balancing problems. However, the proposed package does not solve the voltage balancing problems caused by the gate driver parasitic elements. In such a way, the package is not sufficient since the parasitic capacitance introduced by the gate drive circuitry is one of the main causes of voltage unbalancing [10]. In the experimental set-up, the authors use batteries to supply the gate drivers, mitigating the effects of the parasitic capacitances introduced by the gate drive power supplies. Furthermore, the voltage sharing performance under different load conditions is not analyzed.

Based on the study carried out in [11], a novel package geometry is analyzed in this paper. The natural self-voltage balancing technique takes advantage of parasitic capacitances introduced by a new package geometry to compensate the impacts of the parasitic capacitances introduced by gate drive power supplies.

The paper is organized as follows. In Section II, theoretical analyses are done to investigate the impact of the parasitic capacitances introduced by the classical planar packaging and gate drive circuits. Section III presents a novel concept of packaging and explains how the proposed package can improve the voltage balancing across the series-connected SiC-MOSFETs. In Section IV, the proposed packaging is experimentally validated. Section V presents the conclusions of this paper.

II. Impact of Gate Driver and Packaging/Layout Parasitic Capacitances on Voltage Sharing Performance

A. Gate Drive Power Supply Parasitic Capacitance

In Fig. 1 is shown the classical gate drive circuitry where are highlighted the parasitic capacitances introduced by DC-DC power supplies (C_{ps}) and signal transmission functions of gate drivers (C_{iso}). The parasitic capacitances C_{ps} and C_{iso} have the same dynamic influence on the system. However, in the present work, it is considered that the capacitance C_{iso} is negligible in relation to C_{ps} since in the experiments, isolated signals are implemented by optical fibers. In Fig. 2 is shown the parasitic elements of the gate drive power supply and its connections, where Z_p and Z_s are, respectively, the impedances on the primary and secondary sides of gate driver isolation barriers. As can be seen, two reference potentials are presented in classical switching cells [28], [29], i.e., the ground or reference potential of the remote control circuit (GND) and the reference potential of the power circuit (-VDC). Both GND and -VDC are isolated from each other. Therefore, isolated power converters are implemented in order to enable the isolation dedicated to the power supply parts, and optocouplers or optical fibers are used to isolate the paths for the control signals. It is important to note that, for security reasons the heatsink is usually attached to the reference potential of the remote control circuit (GND), not to -VDC.

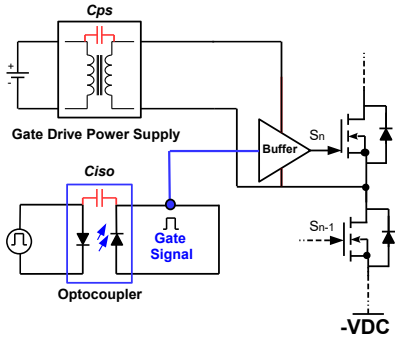

Fig. 1. Parasitic capacitances introduced by gate drive circuits.

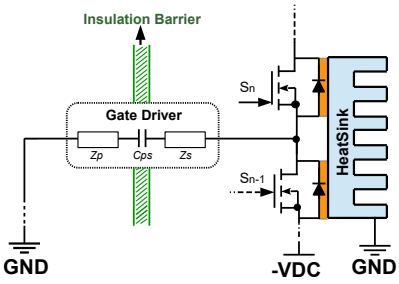

Fig. 2. Parasitic elements of the gate drive power supply and its connections.

Because of the high dv/dt during the switching transients, high charge/discharge currents through the parasitic capacitors C_{ps} are generated. Such charge/discharge currents have the same influence that the load and gate currents during the switching transient, impacting the dynamic behaviors of the series-connected SiC-MOSFETs [30].

B. Packaging/Layout Parasitic Capacitance

To analyze the influence of parasitic capacitances introduced by the classical packaging/layout, a cross section of a simplified planar package and its main elements are shown in Fig. 3, which includes a base-plate, a DBC substrate, and two vertical series-connected SiC-MOSFETs. In terms of voltage balancing and switching speed performances, the drain attached copper trace to ground parasitic capacitance (C_{pac}) introduced by the packaging, is critical. This parasitic capacitance is a key point in the voltage balancing analysis performed in this work. As shown in Fig. 3, two series-connected devices are considered in a traditional planar package. Therefore, two parasitic capacitances (C_{pac1} and C_{pac2}) are introduced, which represent the modeling of the copper traces attached to the drain in relation to the baseplate.

In Fig. 4 is shown an electrical scheme of two SiC-MOSFETs connected in series, where C_{pac1} and C_{pac2} are the drain attached copper trace to ground (heatsink) parasitic capacitances associated to the devices S1 and S2, respectively. C_{DC+} and C_{DC-} are the parasitic capacitances from the DC

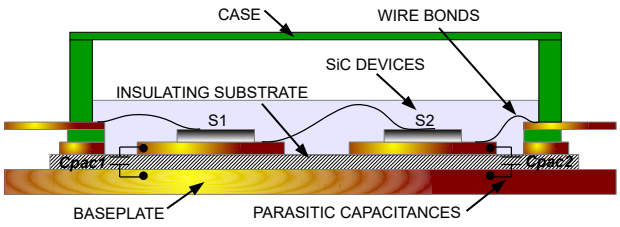

Fig. 3. Cross-section of a simplified standard 2D planar package with two dies connected in series.

bus to the ground, and C_Y are the Y-capacitors often used to suppress the EMI issues [31]–[33]. C_Y are usually placed between + VDC and GND, and - VDC and GND.

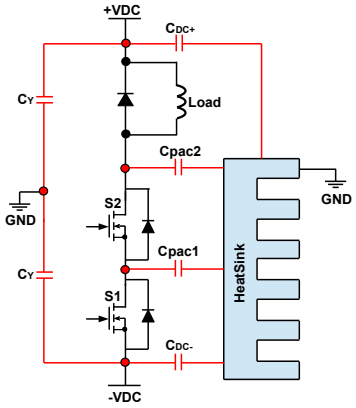

Fig. 4. Equivalent electrical scheme of two SiC-MOSFETs connected in series in a 2D planar package.

The capacitors C_{pac1} and C_{pac2} shown in Figs. 3 and 4 are roughly all the same. However, the dv/dt applied to each of them is different with respect to the position of the device in the stack. Therefore, each parasitic capacitor carries a parasitic current that is getting greater and greater with the device number in the stack (starting from the bottom). The currents that circulate through C_{pac} can drastically impact the dynamic behavior of SiC devices [34], [35]. The capacitors C_{pac} can be estimated based on the planar capacitance formula (1).

$$C_{pac} = \epsilon \frac{A}{d} \tag{1}$$

Where ϵ is the absolute permittivity of the isolated substrate, A is the area of the copper trace where the SiC device is attached, and d is the distance between the copper plate and the baseplate.

C. Impact of Parasitic Capacitances on Voltage Balancing

In Fig. 5 is shown the parasitic capacitance networks introduced by the classical packaging (yellow zone) and gate drive circuits (blue zone) for two series-connected SiC-MOSFETs. The capacitances C_s are the equivalent drain-source intrinsic parasitic capacitances of devices, which are considered all identical. As shown in Fig. 6, a high frequency equivalent circuit can be achieved by short-circuiting the DC-bus terminals and CY capacitors. As can be seen, two parasitic

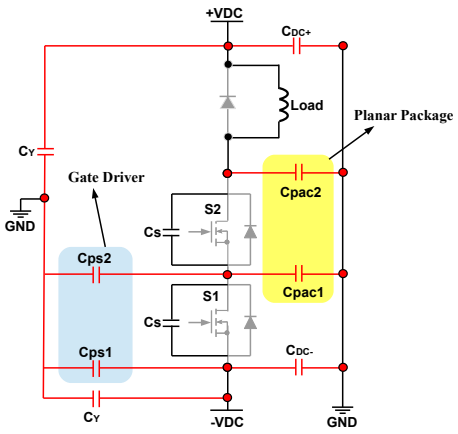

Fig. 5. Equivalent electrical scheme of two SiC-MOSFETs connected in series: 2D planar package and gate drive circuitry.

capacitance networks impact the voltage sharing performance, i.e., the gate driver parasitic capacitance network (blue zone), and the package/layout parasitic capacitance network (yellow zone).

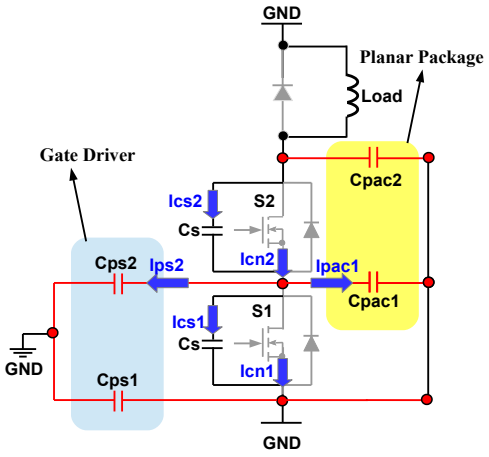

Fig. 6. High frequency equivalent electrical scheme of two series-connected SiC-MOSFETs in a 2D planar package.

To prove that these parasitic capacitance networks unbalance the voltages across series-connected SiC-MOSFETs, a simple proof by contradiction can be done. Consider the current distribution shown in Fig. 6, and the following equations:

$$I_{cn2} + I_{cs2} = I_{cn1} + I_{cs1} + I_{ps2} + I_{pac3} \tag{2}$$

Where I_{csi} is the current that flows through C_s of the device i, I_{cni} is the channel current of the device i, I_{ps2} is the current that circulates through the gate driver capacitance C_{ps2} and I_{pac1} is the current that flows through package parasitic capacitance C_{pac1}.

Applying the proof by contradiction, it can be considered that the V_{ds} voltages across the devices are perfectly balanced. Therefore, the following conditions can be applied:

- 1) the devices experiment equal drain-to-source dv_{ds}/dt. It implies that $I_{cs2} = I_{cs1} = I_{cs}$ since the devices are considered identical.

- 2) the channel currents I_{cn2} and I_{cn1} are identical.

Applying these conditions to Eq. (2):

$$I_{ps2} + I_{pac1} = 0 \tag{3}$$

According to Eq. (3) and Fig. 6, the voltages across the series-connected devices are perfectly balanced, if and only if, $I_{pac1} = I_{ps2} = 0$. However, the greater is the switching speed transition, the greater are I_{pac1} and I_{ps2}. In other words, in a switching cell composed by SiC-MOSFET devices, these currents are always greater than zero. Therefore, even if there is no delay between the gate signals and no mismatch between device characteristics, the V_{ds} voltages will be unbalanced due to the parasitic capacitances of gate driver and package/layout.

III. A Novel Multi-Step Packaging Concept

To compensate the parasitic currents that flow into the gate drive circuitry, a novel Multi-Step Packaging (MSP) concept is proposed in this work. In Fig. 7 is shown the proposed package, which has the following characteristics:

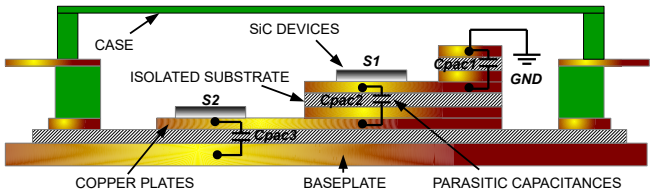

Fig. 7. Novel Proposed Multi-Step Packaging.

- The parasitic capacitors introduced by the packaging (C_{pac}) are located between two subsequent copper layers.
- The devices are placed in the bottom-to-top direction SN→...→S2→S1, where SN is the device connected to the switching cell middle-point.
- For N devices connected in series, it is necessary to have N+1 steps. As shown in Fig. 7, for two series-connected devices, three steps are implemented. The third stage is introduced to generate the parasitic capacitance C_{pac1} between the drain attached bottom device and the ground.
- The number of parasitic capacitances introduced by the packaging is equal to N+1. As shown in Fig. 7 for two series-connected devices, three parasitic capacitances are introduced.

In Fig. 8 is shown the electrical circuit configuration of the parasitic capacitances of the proposed MSP geometry and gate drive circuitry. The green zone represents the parasitic capacitance network introduced by the MSP, where the capacitances C_{pac} are located between the drain and source terminals of each device. The blue zone represents the gate driver parasitic capacitance network.

As shown in Fig. 9, a high frequency equivalent circuit can be achieved by short-circuiting the DC-bus terminals and C_Y capacitors. The main idea of the proposed package/layout is to modify the parasitic capacitance C_{pac} values to compensate the impact of the gate driver parasitic capacitors C_{ps}. In this case, the impacts of C_{pac} and C_{ps} will be nullified by each other. To this end, consider that all the gate drivers in Fig. 9 are

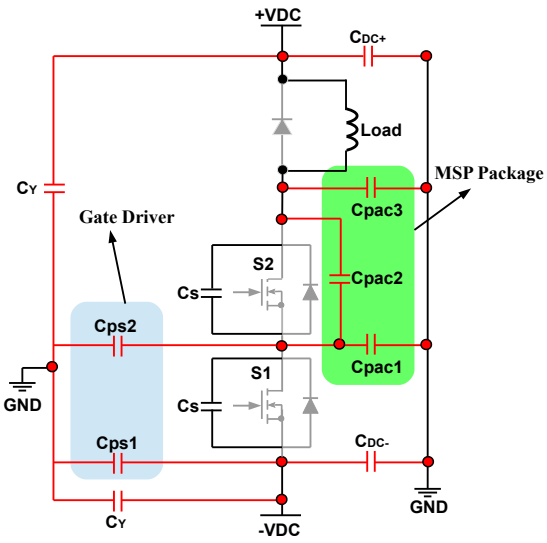

Fig. 8. Equivalent electrical scheme of MSP packaging and gate drive circuitry.

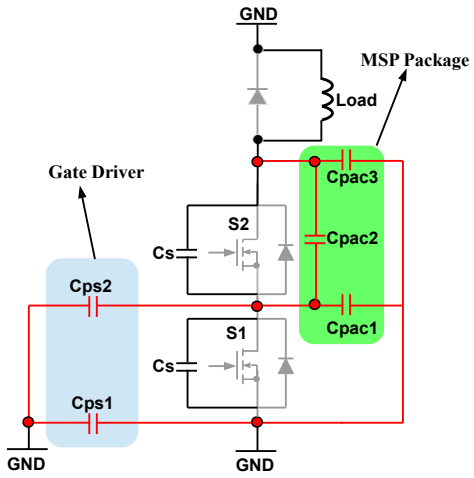

Fig. 9. High frequency electrical scheme of MSP packaging and gate drive circuitry.

identical, i.e., $C_{ps1} = C_{ps2} = C_{ps}$. Therefore, the electrical scheme shown in Fig. 9 can be simplified as shown in Fig. 10, where:

$$C_{eqi} = C_s + C_{paci} \tag{4}$$

To find the appropriate values of C_{pac} that compensate the influence of capacitances C_{ps}, it can be supposed that the voltages across the series-connected devices in Fig. 10 are perfectly balanced, and find the C_{pac} values that ensure this supposition. Based on this assumption, it can be considered that 1) the SiC-MOSFET channel currents are identical, 2) the drain potential of the device N experiments N-times the $\frac{dv}{dt}$ of the drain potential of the device S1 (bottom device) and 3) the series-connected devices have the same drain-to-source $\frac{dv_{ds}}{dt}$. Therefore, according to the mentioned considerations and the current distribution shown in Fig. 10, the following equation

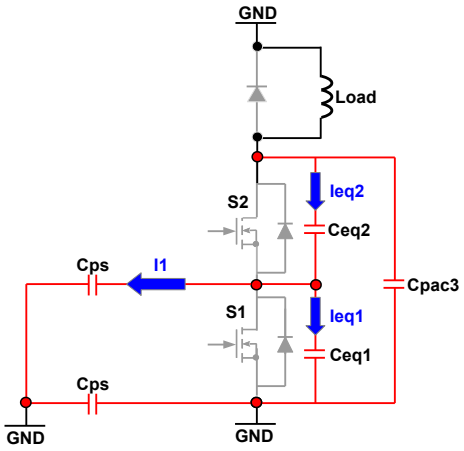

Fig. 10. Current distribution in the MSP and gate drive electrical circuits.

can be written:

$$I_{eq2} = I_1 + I_{eq1} = C_{ps}\left(\frac{dV_{ds}}{dt}\right) + C_{eq1}.\frac{dV_{ds}}{dt} = C_{eq2}.\frac{dV_{ds}}{dt} \quad (5)$$

From Eqs. (4) and (5), the following equation can be written:

$$C_{eq2} = C_{ps} + C_{eq1} = C_s + C_{pac2} = C_{ps} + C_s + C_{pac1} \quad (6)$$

Therefore, the relation between C_{ps}, C_{eq1} and C_{eq2} can be expressed by Eq. (7).

$$C_{pac2} = C_{ps} + C_{pac1} \quad (7)$$

The Eq. (7) is enough to find the appropriate values of C_{pac} that compensate the C_{ps} influence on the voltage balancing for two series-connected devices.

The mathematical recurrence, expressed by Eq. (8) can be written to find the appropriate values of C_{pac} that compensate the C_{ps} influence on the voltage balancing for N-series-connected devices.

$$C_{pacN} = (N-1)C_{ps} + C_{pac(N-1)} \quad (8)$$

As can be seen, to use the recurrence formula, it is necessary to know the values of the gate driver parasitic capacitance C_{ps} and define one of the parasitic capacitances C_{pac}. According to the Eq. (8), higher is the position of the device in the stack, the greater is its associated parasitic capacitance C_{pac}.

Taking a specific case of study where two series-connected devices are driven by gate drivers that introduce parasitic capacitances C_{ps} equal to 15 pF, the values of C_{pac} that compensate the influence of C_{ps} on voltage balancing can be found as follows:

- Number of series-connected devices N = 2.
- Choosing C_{pac1} equal to 15 pF.
- Calculating C_{pac2} (N =2) :
  C_{pac2} = $(2-1)C_{ps}$ + $C_{pac(2-1)}$ = 30 pF

Therefore, if each gate driver introduces a parasitic capacitance C_{ps} equal to 15 pF, and the package/layout is designed to introduce parasitic capacitors of 15 pF (C_{pac1}) and 30 pF (C_{pac2}), the impacts of the gate driver power supply capacitances and package/layout capacitors can be nullified by each other. This theoretical approach is experimentally demonstrated in the next section.

IV. Experimental Analyses

As shown in Fig. 11, a switching cell with two series-connected SiC-MOSFETs C2M0080120D (1200 V, 36 A), and one diode STPSC40H12CWL (1200V, 20A) has been used to investigate the influence of the proposed package concept on the voltage balancing under a total blocking voltage of 1 kV. The DC-DC converter implemented to supply each gate driver used in the experiment is a Murata ^{TM} MGJ6D242005SC that has a parasitic capacitance C_{ps} = 15 pF. Optical fibers are used to achieve gate signal isolation.

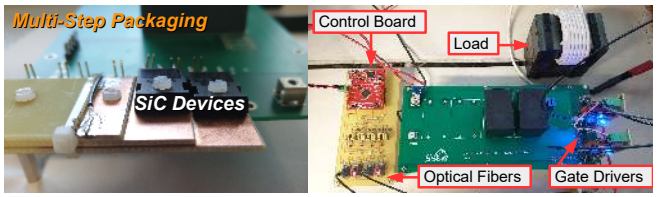

Fig. 11. Switching cell prototype: MSP package and gate drive circuitry.

To validate the theoretical approach, two simplified prototypes have been developed. In these prototypes, the MSP concept is emulated thanks to stacked FR4 layers to account for the package steps. Since the two packages, made out of FR4 materials are unable to dissipate power, the series association is tested in pulsed mode. The developed MSP prototype meets the following requirements:

- The copper plates where the bottom and the top SiC devices are attached, have the following areas: A (bottom device) = 5 cm^2 and A (top device) = 10 cm^2.
- The FR4 dielectric thicknesses between two copper plates, which generate each C_{pac} are all the same, d = 1.5 mm.
- The isolated substrates are made of the same FR4 material and they have the same absolute permittivity, ϵ = 45 pF/m.
- The measured parasitic capacitances for the MSP prototype are $C_{pac1} \approx 15$ pF and $C_{pac2} \approx 30$ pF.
- The traditional packaging introduces parasitic capacitances C_{pac} of around 30 pF.

A specific calibration process is implemented to mitigate the delay between the V_{gs} voltages. An adaptive open-loop external delay control circuit is used to reduce the gate signal delays to low levels ($<$1 ns). During this process, the devices are left with no connection to the FR4 package. After synchronizing the gate signals, the developed package prototypes are attached to the switching, and their impact on the voltage balancing performance are analyzed.

In Fig. 12 is shown the voltage balancing across the power devices when the traditional packaging is used. A pulse train is applied to analyze the voltage balancing under different load currents. The pulse train changes the load current from 0 A to 40 A with a current step of around 6 A. As can be seen in Fig. 12, the parasitic capacitances introduced by the traditional planar package and gate drive circuitry produce

an exacerbated voltage unbalancing that increases with the load current. In Fig. 13 is illustrated the voltage difference between the two V_{ds} voltages. As it is well known, the load current has a proportional influence on the switching speed [36], which in turns lead to great differences between V_{ds2} and V_{ds1}. In other words, when the load current goes up, the gate driver and package capacitances (C_{ps} and C_{pac}) have more and more impact on the voltage balancing. As can be seen, a voltage difference between the top device voltage (V_{ds2}) and the bottom device voltage (V_{ds1}) of around 800 V can be observed when the load current is approximately 40 A. If no voltage balancing method is used, the series-connected devices can be seriously damaged.

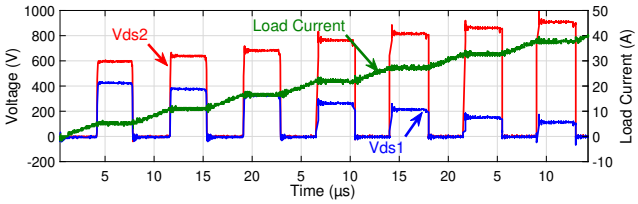

Fig. 12. Experimental results. Voltage unbalancing across two series-connected SiC-MOSFETS; classical planar package.

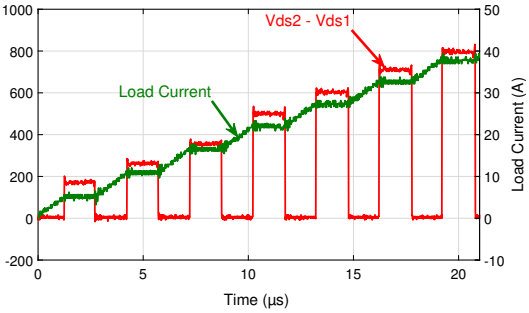

Fig. 13. Experimental results. Voltage difference between the top device voltage (V_{ds2}) and the bottom device voltage (V_{ds1}); classical planar package.

In Fig. 14 is shown the experimental results when the traditional packaged is replaced by the MSP one, which is tested under the same conditions that the traditional packaging. As can be seen, the voltage unbalancing is drastically reduced since C_{ps} and C_{pac} are compensated by each other. However, analyzing the voltage balancing across the series-connected SiC-MOSFETs as shown in Fig. 15, it can be seen that the voltage sharing has a small variation with the load current. This is due to the gate signal delay that although it is less than 1 ns, it can still unbalance the voltages. Furthermore, the mismatch between the device intrinsic capacitances can also be the cause of the voltage unbalancing seen in Fig. 15.

In Fig. 16 are zoomed the dynamic voltage balancing for three different values of load current, i.e., I_L= 12, 18 and 26 A. In all the cases, the two series-connected SiC-MOSFETs have similar dv/dt as predicted by the theoretical analyses presented in Section III. Note that, the mismatch between device dv/dts is more visible for a load current equal to 26 A. At this point, the voltage unbalancing causes have more impact

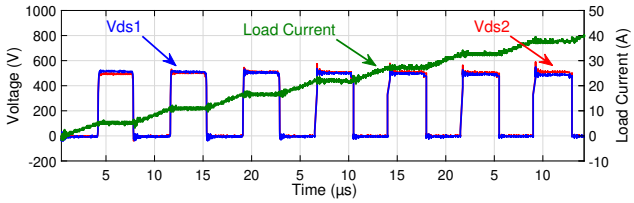

Fig. 14. Experimental results. Voltage balancing across two series-connected SiC-MOSFETS; proposed MSP package.

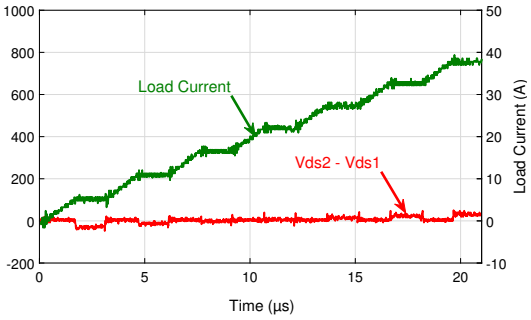

Fig. 15. Experimental results. Voltage difference between the top device voltage (V_{s2}) and the bottom device voltage (V_{s1}); proposed MSP package.

since the switching speed starts to increase considerably when compared to the previous switching points ($I_L < 18\ A$). A small dynamic and static voltage difference, during the turn-off and turn-on transitions, can be observed at I_L = 26 A.

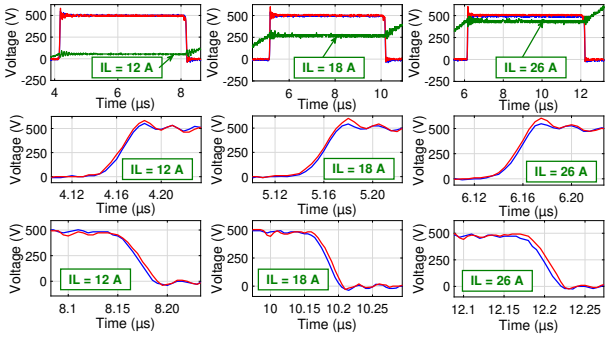

Fig. 16. Experimental results. Voltage balancing across two series-connected SiC-MOSFETs as a function of the load current; proposed MSP package. Full waveforms (top), zoom on turn-off (middle) and turn-on (bottom) switching transitions.

The measured dv/dt as a function of the load current are shown in Fig. 17. As can be seen, the switching speed of the devices, during the turn-off transients (solid lines), increases as a function of the load current. During the turn-on (dash lines) and turn-off (solid lines) transients, both series-connected devices (S_1 and S_2) have approximately the same dv/dt no matter the load current value. The middle point switching cell experiments high dv/dt, which reaches approximately 60 V/ns for I_L = 40 A during the turn-off transient. According to the SiC-MOSFETs C2M0080120D (1200 V, 36 A) datasheet, the fall and rise times for each individual device, is 14 and

22 ns, respectively. The values are based under tests with blocking voltage of 800 V, load current of 20 A and external gate resistances of 2.5 Ω. It means that the proposed MSP package has low negative impacts on the switching cell dv/dt since only two "capacitors" of 15 and 30 pF are added by the MSP package. In other words, the proposed MSP is an effective way to reduce voltage balancing problems without slowing down the switching speed of the devices. The impact of the MSP on the dv/dt depends on C_{pac} values. The higher is C_{pac} values, the more it slows down the switching speed. On the other hand, high values of C_{pac} increases the MSP performance in terms of voltage balancing since the mismatch between device intrinsic capacitances can be nullified by the capacitances C_{pac}.

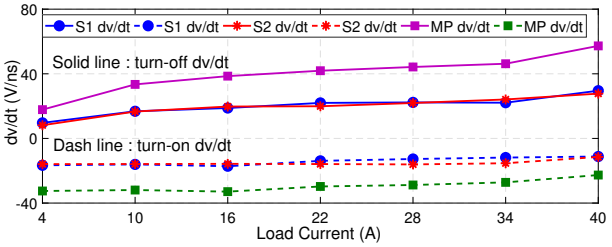

Fig. 17. Experimental results. dv/dt as a function of the load current; proposed MSP package. Turn-on (dash lines) and turn-off (solid lines) transients.

As can be seen, the proposed self-voltage balancing technique takes advantage of the parasitic capacitances introduced by a novel packaging geometry in order to improve the voltage sharing performance of series-connected SiC-MOSFETs. If the delay between the gate signals and the mismatch between the devices characteristics are considerably small, the proposed technique can provide acceptable voltage balancing across the devices without any other voltage balancing method.

In [27], thermal management considerations have been discussed for a similar MSP package. MSP geometries introduce non homogeneous propagation paths for the heat flux from each device to ambient. The addition of several dielectric layers, along with the number of steps, brings an increase of the junction to ambient thermal resistance, which produces an increase of junction temperature for the devices "above" with respect to the "bottom" device, the one located closer to the heat sink. However, the study presented in [27] reveals that if the additional dielectric layers have small thermal resistances with respect to the other thermal resistance on the path of the heat flux, than, the MSP geometry has a limited impact on the distribution of the junction temperatures of the devices implemented on each step of the package.

V. Conclusion

In this paper is analyzed a novel natural self-balancing voltage technique for series-connected SiC-MOSFETs. The propose method takes advantage of the parasitic capacitances introduced by a multi-step package to compensate the parasitic capacitances introduced by the gate driver circuitry and to reduce the voltage unbalancing across the power devices. In a first step, basics and concepts are explained using mathematical analysis. The package concept is compared to the traditional planar solution in terms of voltage sharing performance. The study is performed by theoretical and experimental analyses. As expected, the proposed package shows better performance than the traditional planar package in terms of voltage balancing. The present study demonstrates that if the delay between gate signals and device parameter mismatch are significantly reduced, the proposed package can provide an acceptable voltage sharing performance without needing other voltage balancing techniques. Furthermore, the proposed technique can be applied in conjunction with other voltage balancing methods. The authors believe that the proposed packaging can be applied as a preventive solution. In this case, when the proposed technique is applied in conjunction with clamp circuits or active gate control techniques, less stress on the passive devices and less switching losses will be present. This concept will be analyzed in future works.

References

[1] G. F. Reed, B. M. Grainger, M. J. Korytowski, and E. J. Taylor, "Modeling, analysis, and validation of a preliminary design for a 20 kv medium voltage dc substation," in *IEEE 2011 EnergyTech*, May 2011, pp. 1–8.

[2] L. F. S. Alves, P. Lefranc, P. Jeannin, and B. Sarrazin, "Review on sic-mosfet devices and associated gate drivers," in *2018 IEEE International Conference on Industrial Technology (ICIT)*, Feb 2018, pp. 824–829.

[3] L. F. S. Alves, R. C. M. Gomes, P. Lefranc, R. De A. Pegado, P. Jeannin, B. A. Luciano, and F. V. Rocha, "Sic power devices in power electronics: An overview," in *2017 Brazilian Power Electronics Conference (COBEP)*, Nov 2017, pp. 1–8.

[4] A. Bolotnikov, P. Losee, A. Permuy, G. Dunne, S. Kennerly, B. Rowden, J. Nasadoski, M. Harfman-Todorovic, R. Raju, F. Tao, P. Cioffi, F. J. Mueller, and L. Stevanovic, "Overview of 1.2kv-2.2kv sic mosfets targeted for industrial power conversion applications," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2015, pp. 2445–2452.

[5] T. Van Nguyen, P. Jeannin, E. Vagnon, D. Frey, and J. Crebier, "Series connection of igbt," in *2010 Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Feb 2010, pp. 2238–2244.

[6] S. Buonomo, F. Distefano, A. Gaito, R. Scollo, F. Chimento, A. Raciti, S. Tomarchio, and D. Armenia, "Series connection of power switches in high input voltage with wide range power supply for gate driving application," in *2011 IEEE Energy Conversion Congress and Exposition*, Sep. 2011, pp. 2985–2992.

[7] G. Belverde, A. Galluzzo, M. Melito, S. Musumeci, and A. Raciti, "Snubberless voltage sharing of series-connected insulated-gate devices by a novel gate control strategy," *IEEE Transactions on Power Electronics*, vol. 16, no. 1, pp. 132–141, Jan 2001.

[8] L. F. S. Alves, V. Nguyen, P. Lefranc, J. Crebier, P. Jeannin, and B. Sarrazin, "A cascaded gate driver architecture to increase the switching speed of power devices in series connection," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, pp. 1–1, 2020.

[9] S. Parashar and S. Bhattacharya, "A novel gate driver for active voltage balancing in 1.7kv series connected sic mosfets," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2019, pp. 2773–2779.

[10] L. F. S. Alves, V. Nguyen, P. Lefranc, B. Sarrazin, P. Jeannin, A. Derbey, and J. Crebier, "Gate driver architectures impacts on voltage balancing of sic mosfets in series connection," in *2018 20th European Conference on Power Electronics and Applications (EPE'18 ECCE Europe)*, Sep. 2018, pp. P.1–P.9.

[11] L. F. S. Alves, P. Lefranc, P. Jeannin, B. Sarrazin, and J. Crebier, "Multi-step packaging concept for series-connected sic mosfets," in *2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe)*, Sep. 2019, pp. P.1–P.10.

[12] A. Marzoughi, R. Burgos, and D. Boroyevich, "Active gate-driver with dv/dt controller for dynamic voltage balancing in series-connected sic mosfets," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 4, pp. 2488–2498, 2019.

[13] F. Zhang, X. Yang, W. Chen, and L. Wang, "of series-connected sic mosfets by using energy recovery snubber circuits," *IEEE Transactions on Power Electronics*, pp. 1–1, 2020.

[14] Y. Ren, X. Yang, F. Zhang, K. Wang, W. Chen, L. Wang, and Y. Pei, "A compact gate control and voltage-balancing circuit for series-connected sic mosfets and its application in a dc breaker," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 10, pp. 8299–8309, Oct 2017.

[15] Y. Ren, X. Yang, F. Zhang, F. Wang, L. M. Tolbert, and Y. Pei, "A single gate driver based solid-state circuit breaker using series connected sic mosfets," *IEEE Transactions on Power Electronics*, vol. 34, no. 3, pp. 2002–2006, March 2019.

[16] R. Wang, L. Liang, Y. Chen, and Y. Kang, "A single voltage-balancing gate driver combined with limiting snubber circuits for series-connected sic mosfets," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 1, pp. 465–474, March 2020.

[17] V. N. Jakka, A. Kumar, S. Parashar, S. K. Rastogi, N. Kolli, R. Jaiswal, and S. Bhattacharya, "Voltage balancing of series connected clamping diodes in medium voltage npc converter enabled by gen-3 10 kv sic mosfets for asynchronous micro-grid power conditioning system (ampcs)," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019, pp. 5798–5804.

[18] X. Wu, S. Cheng, Q. Xiao, and K. Sheng, "A 3600 v/80 a series–parallel-connected silicon carbide mosfets module with a single external gate driver," *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2296–2306, May 2014.

[19] A. B. Jørgensen, "Analysis of cascaded silicon carbide mosfets using a single gate driver for medium voltage applications," *IET Power Electronics*, vol. 13, pp. 413–419(6), February 2020. [Online]. Available: https://digital-library.theiet.org/content/journals/10.1049/iet-pel.2019.0573

[20] I. Lee and X. Yao, "Active gate control for series connected sic mosfets," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2019, pp. 453–457.

[21] C. Yang, Y. Pei, Y. Xu, F. Zhang, L. Wang, M. Zhu, and L. Yu, "A gate drive circuit and dynamic voltage balancing control method suitable for series-connected sic mosfets," *IEEE Transactions on Power Electronics*, vol. 35, no. 6, pp. 6625–6635, 2020.

[22] T. Wang, H. Lin, and S. Liu, "An active voltage balancing control based on adjusting driving signal time delay for series-connected sic mosfets," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 1, pp. 454–464, 2020.

[23] C. Liu and Q. Lei, "Current source gate driver for series connected silicon-carbide (sic) mosfets," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2019, pp. 991–997.

[24] T. Van Nguyen, P. Jeannin, E. Vagnon, D. Frey, and J. Crebier, "Series connection of igbts with self-powering technique and 3-d topology," *IEEE Transactions on Industry Applications*, vol. 47, no. 4, pp. 1844–1852, July 2011.

[25] L. Pang, T. Long, K. He, Y. Huang, and Q. Zhang, "A compact series-connected sic mosfets module and its application in high voltage nanosecond pulse generator," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 12, pp. 9238–9247, Dec 2019.

[26] F. V. Robinson and V. Hamidi, "Series connecting devices for high-voltage power conversion," in *2007 42nd International Universities Power Engineering Conference*, Sep. 2007, pp. 1205–1210.

[27] L. F. Alves, P. Lefranc, P.-O. Jeannin, B. Sarrazin, and J.-C. Crebier, "Analysis of the multi-steps package (msp) for series-connected sic-mosfets," *Electronics*, vol. 9, no. 9, p. 1341, 2020.

[28] R. Herzer, "New gate driver solutions for modern power devices and topologies," in *CIPS 2016; 9th International Conference on Integrated Power Electronics Systems*, March 2016, pp. 1–11.

[29] B. B. Kennedy, "Implementing an isolated half-bridge gate driver," 2012.

[30] P. Lefranc, L. F. S. Alves, P. Jeannin, B. Sarrazin, V. Nguyen, and J. Crebier, "A predictive model to investigate the effects of gate driver on dv/dt in series connected sic mosfets," in *PCIM Europe 2019; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, May 2019, pp. 1–8.

[31] S. Guo, L. Zhang, Y. Lei, X. Li, W. Yu, and A. Q. Huang, "Design and application of a 1200v ultra-fast integrated silicon carbide mosfet module," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2016, pp. 2063–2070.

[32] K. Klein, E. Hoene, R. Reiner, and R. Quay, "Study on packaging and driver integration with gan switches for fast switching," in *CIPS 2016; 9th International Conference on Integrated Power Electronics Systems*, 2016, pp. 1–6.

[33] O. Kreutzer, B. Eckardt, and M. Maerz, "Optimum gate driver design to reach sic-mosfet's full potential - speeding up to 200 kv/us," in *2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2015, pp. 41–46.

[34] D. N. Dalal, N. Christensen, A. B. Jorgensen, J. K. Jorgensen, S. Beczkowski, S. Munk-Nielsen, and C. Uhrenfeldt, "Impact of power module parasitic capacitances on medium voltage sic mosfets switching transients," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, pp. 1–1, 2019.

[35] X. Lin, L. Ravi, Y. Zhang, D. Dong, and R. Burgos, "Analysis of parasitic capacitors' impact on voltage sharing of series-connected sic mosfets and body-diodes," in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2020, pp. 208–215.

[36] X. Huang, S. Ji, J. Palmer, L. Zhang, L. M. Tolbert, and F. Wang, "Parasitic capacitors' impact on switching performance in a 10 kv sic mosfet based converter," in *2018 IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2018, pp. 311–318.