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A charge-density-wave oscillator based on an integrated tantalum disulfide–boron nitride–graphene device operating at room temperature

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The charge-density-wave (CDW) phase is a macroscopic quantum state consisting of a periodic modulation of the electronic charge density accompanied by a periodic distortion of the atomic lattice in quasi-1D or layered 2D metallic crystals^{1–4}. Several layered transition metal dichalcogenides, including 1T-TaSe₂, 1T-TaS₂ and 1T-TiSe₂ exhibit unusually high transition temperatures to different CDW symmetry-reducing phases^{1,5,6}. These transitions can be affected by the environmental conditions, film thickness and applied electric bias¹. However, device applications of these intriguing systems at room temperature or their integration with other 2D materials have not been explored. Here, we demonstrate room-temperature current switching driven by a voltage-controlled phase transition between CDW states in films of 1T-TaS₂ less than 10 nm thick. We exploit the transition between the nearly commensurate and the incommensurate CDW phases, which has a transition temperature of 350 K and gives an abrupt change in current accompanied by hysteresis. An integrated graphene transistor provides a voltage-tunable, matched, low-resistance load enabling precise voltage control of the circuit. The 1T-TaS₂ film is capped with hexagonal boron nitride to provide protection from oxidation. The integration of these three disparate 2D materials in a way that exploits the unique properties of each yields a simple, miniaturized, voltage-controlled oscillator suitable for a variety of practical applications.

The 1T polytype of TaS₂ undergoes the transition from a normal metallic phase to an incommensurate CDW (IC-CDW) phase at 545 K, to a nearly commensurate CDW (NC-CDW) phase at 350 K and, finally, to a commensurate CDW (C-CDW) phase at 180 K (refs 7–11). Each phase transition is accompanied by a lattice reconstruction, which results in strong modifications to the material's electrical properties. In 1T-TaS₂, the C-CDW phase drives a Mott–Hubbard metal-to-insulator transition (MIT) that results in a Mott insulating state. Intercalation and doping, the ambient pressure, the thickness of the quasi-2D films, optical excitation and the applied electric source–drain and gate bias can modify the transitions to different CDW phases^{7–16}. For example, when the thickness of the 1T-TaS₂ film is <10 nm, the C-CDW–NC-CDW transition at 180 K disappears, whereas the NC-CDW–IC-CDW transition at 350 K persists¹⁰. A source–drain voltage can trigger the phase transition. In the case of 1T-TaS₂ the electrical conductivity abruptly increases when the applied electric field exceeds 20 kV cm^{−1}, which is attributed to the insulator-to-metal transition (IMT)¹⁴. A reverse MIT is revealed when the voltage is

swept back¹⁴. Despite great recent interest in the CDW properties of quasi-2D transition metal dichalcogenides^{10–12,14,17}, neither the IMT nor the MIT induced by an electric field have been observed above room temperature. Correspondingly, no devices that use CDW transitions as the basis of their operation have been demonstrated at or near room temperature.

In this work, we show that an abrupt change in the electrical conductivity and hysteresis observed at the IMT and MIT transitions associated with the transition between the NC-CDW and IC-CDW phases in a quasi-2D 1T-TaS₂ channel can be used to construct an oscillator that operates at room temperature and up to 320 K. A second quasi-2D material, hexagonal boron nitride (h-BN), provides environmental protection against oxidation and preserves the CDW phase. A third integrated 2D material, graphene, provides a transistor with a current density and load resistance that closely match to TaS₂, allowing precise voltage control of the oscillator frequency. The voltage-controlled oscillator (VCO) demonstrated here does not require a complicated biasing circuit and could lead to inexpensive technologies for communication systems and other applications.

High-quality 1T-TaS₂ crystals were prepared by the chemical vapour transport method (see Methods). The prototype devices were fabricated with exfoliated thin films. To protect the exfoliated 1T-TaS₂ from oxidation we used an h-BN capping layer positioned on top of the CDW channel^{18,19}. The fabricated devices consisted of 1T-TaS₂ channels with depth in the range of 6–9 nm and Pd/Au (15/60 nm) contacts. An optical image of a typical device is shown in an inset in Fig. 1b (see also Supplementary Figs 1–6). Figure 1a shows the current–voltage (*I*–*V*) characteristics of such TaS₂–BN devices in the temperature range from 78 to 395 K, which includes the 1T-TaS₂ phase transition from the NC-CDW to IC-CDW states. Below 320 K, we observe a prominent abrupt current jump as the voltage exceeds a certain value, denoted here as *V*_H. This behaviour is also referred to as threshold switching between the low and high conductivity states. When the voltage is swept back to zero, a reverse threshold switch occurs at a lower voltage *V*_L that corresponds to a smaller critical electric field. The difference between these two voltages forms a hysteresis window. Details extracted from Fig. 1a are shown in Supplementary Fig. 4. It is important to note that the threshold switching effect in our device exists throughout the temperature range from 78 to 320 K. As the temperature is increased to 345 K, slightly below the transition from NC-CDW to IC-CDW at 350 K, threshold switching becomes weak (inset, Fig. 1a). Increasing the temperature above 350 K

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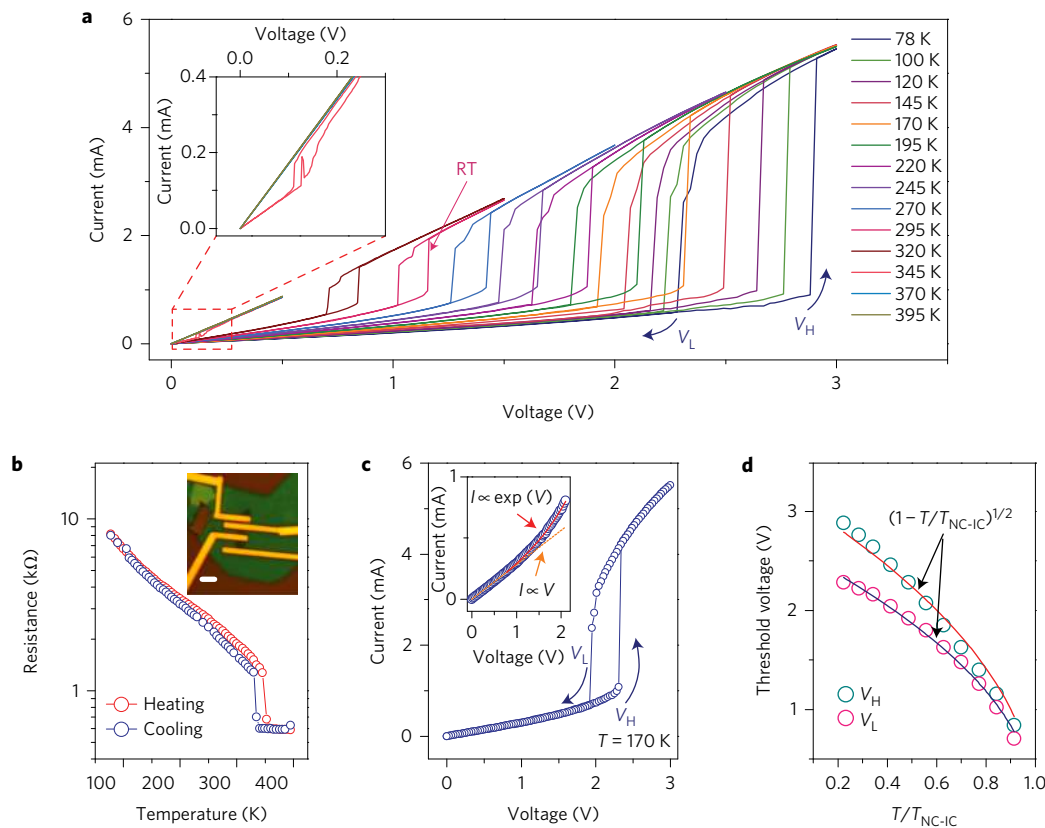


Figure 1 | Electrical characteristics of thin-film 1T-TaS₂. **a**, I - V characteristics of thin-film 1T-TaS₂ at different temperatures from 78 to 395 K. The threshold switching effect is prominent from 78 to 320 K. The blue arrows indicate the voltage sweep direction for the measurement at 78 K. For all other temperatures V_H is always higher than V_L . The hysteresis window is defined as $V_H - V_L$. The threshold switching is prominent up to 320 K, and becomes less pronounced as the temperature approaches the NC-CDW-IC-CDW transition at 350 K. As shown in the inset, at 345 K the threshold switching is still measurable. As the temperature exceeds 350 K, the I - V slope becomes linear. **b**, Temperature-dependent resistance measurements for a 9-nm-thick 1T-TaS₂ film. The NC-CDW-IC-CDW and IC-CDW-NC-CDW transitions happen at 350 and 340 K during the heating and cooling processes, respectively. The resistance is measured at a low voltage ($V = 20$ mV). Inset: An optical image of a typical h-BN-capped 1T-TaS₂ device. The dark purple strip is the 1T-TaS₂ thin film and the larger green region is the h-BN film. Scale bar, 5 μ m. **c**, Superlinear I - V characteristics below V_H . The curve at $T = 170$ K is shown here as an example. Arrows indicate the voltage sweeping directions. Inset: The current below V_H can be fitted with an exponential component $I \propto \exp(V)$ superimposed on a linear curve $I \propto V$. **d**, Temperature-dependent threshold switching voltage. Both V_H and V_L are proportional to $(1 - T/T_{NC-IC})^{1/2}$, a dependency that is identical to that described by analytical theories of the CDW order parameter¹.

results in the disappearance of threshold switching and the I - V characteristics become linear as the 2D 1T-TaS₂ channel enters the IC-CDW phase. Figure 1b presents the temperature-dependent resistance measured with a small voltage (20 mV). The resistance decreases as temperature increases until the NC-CDW-IC-CDW transition point near 350 K is reached, where the resistance drops abruptly. After the transition the resistance becomes almost constant with temperature. In the cooling cycle, the resistance jump occurs at 340 K, forming a temperature hysteresis. The absence of a C-CDW to NC-CDW phase transition at 180 K in very thin films (<9 nm) of 1T-TaS₂ is consistent with a recent report¹⁰.

Another interesting observation is that the resistance value after electrically induced switching is the same for all temperatures, as seen from the similar slopes of the I - V curves at high field in Fig. 1a. The resistance extracted from the slope is 580 Ω , which matches the low-field temperature-dependent resistance of 590 Ω presented in Fig. 1b at $T > 350$ K. In addition, the low-field resistances extracted at lower temperatures from the I - V slopes in Fig. 1a are also in agreement with the measured resistance in Fig. 1b, shown in Supplementary Fig. 8. This equivalence in resistance values is consistent with the picture of voltage-controlled switching driving the 1T-TaS₂ between the NC-CDW and the IC-CDW phases. Another possibility is that the applied field and

the resulting current destroy the Mott insulating state within the individual CDW domains while leaving the lattice in the NC-CDW phase. We also note that the threshold switching voltage scales linearly with the channel length (Supplementary Fig. 5). The critical fields E_H and E_L are 28.8 and 22.8 kV cm^{-1} at 78 K and decrease to 11.2 and 10.2 kV cm^{-1} at room temperature. The length scaling suggests a possibility of further reductions of the threshold voltage for devices with shorter channels.

We observe that the I - V characteristics below V_H do not have a simple linear dependence. Instead there is an extra exponential component as shown in Fig. 1c. The temperature dependence of the threshold voltages V_H (V_L) follows the relation $(1 - T/T_{NC-IC})^{1/2}$ below the NC-CDW-IC-CDW transition temperature of 350 K (see Fig. 1d). This temperature dependence is the same as that described by analytical theories of the CDW order parameter¹ and has recently been observed in 2H-TaS₂ (ref. 20).

By connecting this 1T-TaS₂ device with an off-chip $R_L = 1$ k Ω load resistor (see the schematic in Fig. 2a), we observe stable voltage oscillation at the node between these two components when applying a d.c. bias V_{DC} . These voltage oscillations, monitored by an oscilloscope, are shown in Fig. 2b. The initiation of oscillations requires V_{DC} values within a certain range. When V_{DC} is below 3.8 V no oscillations occur. As V_{DC} increases, the oscillations

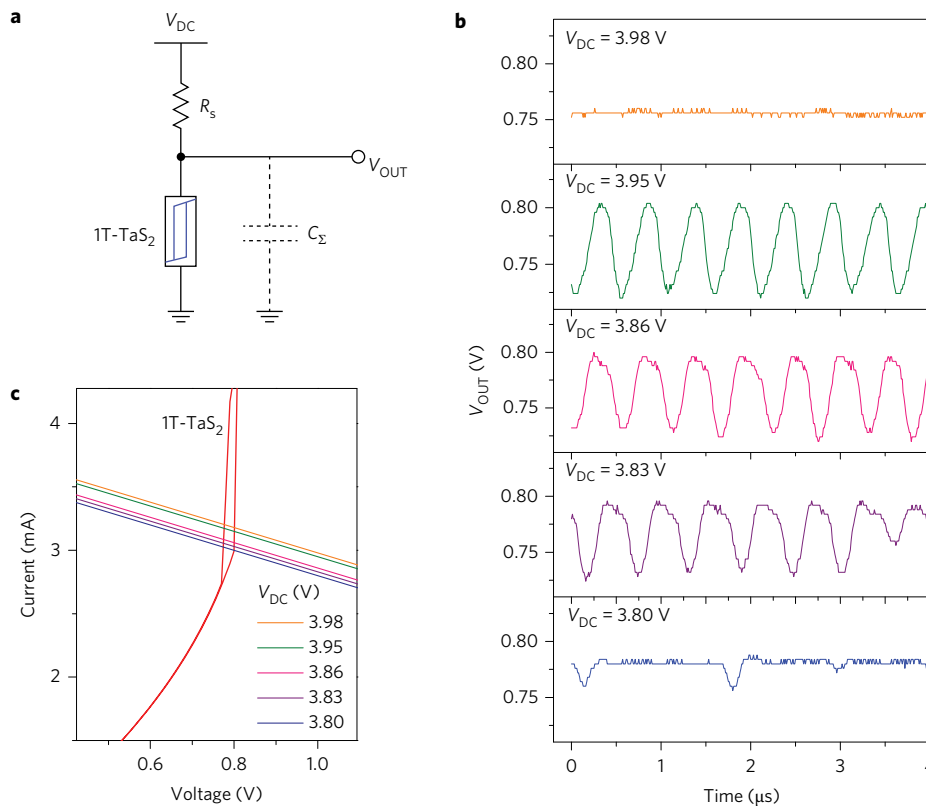


Figure 2 | Oscillator circuit of a 1T-TaS₂ film with an off-chip load resistor. **a**, The circuit diagram of the oscillator consists of the 1T-TaS₂ film, a series-connected load resistor and a lumped capacitance C_{Σ} from the output node V_{OUT} to ground. The load resistance is 1 k Ω . The output terminal is monitored by an oscilloscope. **b**, Voltage oscillations under different V_{DC} values. The circuit oscillates when V_{DC} is within the range of 3.83 V to 3.95 V. The oscillation frequencies are approximately 1.77, 1.85 and 2 MHz when V_{DC} is 3.83, 3.86 and 3.95 V, respectively. **c**, Load lines of the resistor at different V_{DC} values. The blue line, which represents $V_{DC} = 3.8$ V, intersects with V_H of 1T-TaS₂. This is the condition at which the circuit is about to oscillate.

become sinusoidal. The oscillation frequency, f , is dependent on V_{DC} . In this specific device f was tuned from 1.77 to 2 MHz as V_{DC} changed from 3.83 to 3.95 V. When V_{DC} becomes greater than 3.98 V, the oscillation stops. The oscillation mechanism can be understood as the switching of the 1T-TaS₂ device between the IMT and MIT states with the negative feedback from the load resistor R_L . When V_{DC} is large enough, the d.c. voltage across the 1T-TaS₂ channel reaches V_H and triggers the IMT. The sudden increment in current results in a large voltage increase across the load resistor and increasing the voltage across 1T-TaS₂, driving it back into its metallic state. As long as this voltage can increase to a level higher than V_H the cycle keeps repeating. Figure 2c provides further explanation. The intersection of the 1T-TaS₂ curve with the load line is the operation d.c. voltage at the output. The line representing $V_{DC} = 3.8$ V is on the edge of V_H , where the oscillations just start. As the oscillation is triggered by IMT–MIT processes, it also can be observed at lower temperature (Supplementary Fig. 6).

Voltage control of an oscillator frequency using simple circuitry is highly desirable for numerous miniaturized electronic systems. Conventional VCOs usually require multiple transistors and resistors for biasing^{21,22}. By monolithically integrating a top-gate graphene field-effect transistor (G-FET) with an h-BN capped 1T-TaS₂ device, we demonstrate a VCO operating at room temperature. The gate and contact electrodes for this 2D integrated TaS₂–h-BN–graphene oscillator were fabricated with electron beam lithography, dry etching and metal evaporation (Supplementary Fig. 3). The device structure and SEM image are presented in

Fig. 3a (bottom),b, respectively. The equivalent circuit and the biasing scheme are shown in Fig. 3a (top). The d.c. bias is applied across the integrated structure whereas the gate voltage of the G-FET is used to change R_L and hence tune the oscillation frequency. Note that both the 1T-TaS₂ and graphene sides of the channel are contacted from the edge, forming quasi-1D contacts^{18,23}. The h-BN entirely covers the 1T-TaS₂ and graphene sides of the channel to protect against environmental exposure.

The resulting device demonstrates excellent control of the oscillations using the gate voltage, V_G , of the G-FET. The gate voltage can turn oscillations on and off and tune f monotonically. As shown in Fig. 3c, no oscillations occur at the output when V_G is set at zero. As V_G increases to 0.68 V, the device starts to produce stable oscillations. For V_G values varying from 0.68 to 1.80 V the frequency can be tuned monotonically from 1.42 to 1.04 MHz. As V_G increases above 1.80 V the oscillations begin to show missing cycles, indicating that the bias setting exceeds the oscillation requirement. V_{DC} is set at 3.65 V for these measurements. The tuning mechanism can be understood by examining the load line. As the slope of the load line changes with V_G and falls within the red hatched region in Fig. 3d, oscillations appear at the output. The transfer characteristic of the G-FET is shown in the inset to Fig. 3d. Note that V_{DS} is biased at 2.4 V, close to the value of the voltage drop across the G-FET when the circuit operates at $V_{DC} = 3.65$ V. The charge neutrality point in this case is at 2.4 V, shifted by the large source–drain voltage of G-FET (V_{DS}). As V_G increases from zero to 2.1 V, the resistance of the graphene channel monotonically increases, resulting in the oscillation frequency decreasing due to the increased RC time constant, where R and C are the effective resistance and capacitance, respectively. Figure 3e shows the gate

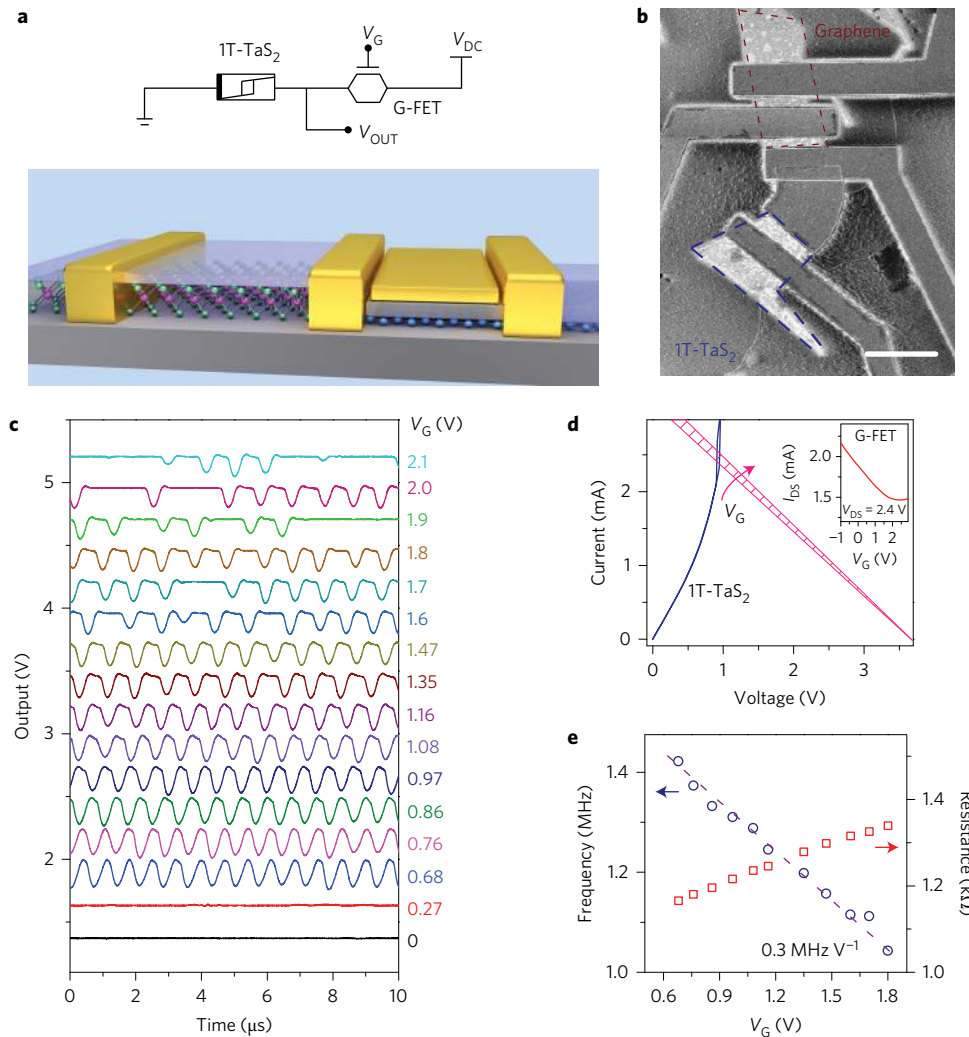


Figure 3 | The integrated 1T-TaS₂-BN-graphene VCO. **a**, Bottom: The device structure of the integrated oscillator consists of a G-FET series connected to 1T-TaS₂. Both the graphene and TaS₂ are fully covered with h-BN, which acts as a protective layer against oxidation for the 1T-TaS₂ and as a gate dielectric for the G-FET. The equivalent circuit and biasing set-up is shown in the top panel. The V_{DC} bias is applied at the drain terminal of the G-FET and the V_G bias is connected to the gate terminal of G-FET. The ground is connected to one terminal of 1T-TaS₂ device and the output port is common to both devices. **b**, The SEM image of the integrated 1T-TaS₂-BN-graphene VCO. The graphene and the TaS₂ are highlighted by dashed lines. Scale bar, 4 μm. **c**, Output waveforms at different gate biases when V_{DC} is fixed at 3.65 V. The oscillation frequency is tunable with gate biases in the range of 0.68 V to 1.8 V. The different waveforms are vertically offset by 0.25 V for clarity. **d**, The load line representing the resistance range of the G-FET intersects with the I-V curve of the 1T-TaS₂ device. The arrow indicates the slope change of the load line with V_G. The inset shows the transfer characteristics (source-drain current, I_{DS}, as function of V_G) of the G-FET under a source-drain bias at 2.4 V. **e**, The dependence of the oscillation frequency on the gate bias. Blue circles show the frequency of the oscillation under an increased gate bias. The frequency can be adjusted monotonically with a tuning sensitivity of 0.3 MHz V⁻¹. The red squares are the resistance values of the G-FET under different gate biases with V_{DC} = 2.4 V.

voltage tunability of the oscillator frequency. The tuning sensitivity is 0.3 MHz V⁻¹, and the oscillation amplitude V_{pp} is ~0.2 V. Control of both characteristics will improve dramatically as the technology for handling 2D materials advances.

The monolithic integration of a quasi-2D CDW channel with graphene has several advantages. The current carrying capacity of G-FETs²⁴ makes graphene a well-matched load to the low-resistance TaS₂. The oscillations occur when the IMT is triggered in 1T-TaS₂ in the mA range (for the 1–2 μm wide samples). With similar dimensions to 1T-TaS₂, graphene provides a well-matched current density and resistance. Owing to the linear resistance tunability with the gate voltage of the G-FET at high V_{DS} and high carrier concentrations, the frequency of the oscillator can be tuned linearly by V_G over a wide range. The tuning linearity of VCOs is required for many practical applications²¹. An extra advantage of the CDW-G-FET integrated device is that G-FETs have been demonstrated to

operate at very high frequencies of hundreds of GHz^{25,26}, which allows for increased oscillation frequencies. In our proof-of-concept measurements, the frequency is limited by the extrinsic RC time constants of the probe station. The intrinsic resistances and capacitances can be reduced by scaling. The graphene and h-BN layers in the device structure also act as heat spreaders owing to their high thermal conductivity^{27,28}.

From the circuit models in Figs 2a or 3a, the frequency is determined by the charging and discharging time of the capacitance, which is given by

$$1/f = T = C [(R_s/R_{di}) \ln(\alpha_i) - (R_s/R_{dm}) \ln(\alpha_m)] \quad (1)$$

where $\alpha_{m,i} = [V_{DC} - (1 + R_s/R_{dm,di})V_L] / [V_{DC} - (1 + R_s/R_{dm,di})V_H]$, m and i represent metallic and insulating states, respectively, R_{di} is the resistance of TaS₂ in the insulating state, R_{dm} is the resistance of

TaS₂ in the metallic state, R_s is the load resistance of either the resistor or the G-FET and C is the lumped capacitance between the output node and the ground (Supplementary Fig. 7). R_s/R_{di} is the parallel resistance of the R_s and R_{di} . The intrinsic geometric capacitances and the resistivities of the 1T-TaS₂ film and the load resistor or transistor set the upper frequency limit of oscillation. The sheet resistivities of the 1T-TaS₂ in the high and low resistance states are $3 \text{ k}\Omega \square^{-1}$ and $740 \Omega \square^{-1}$, respectively. These values are relatively low, allowing for extremely small RC time constants. Considering only the parallel plate capacitance to ground of the TaS₂ and graphene, the intrinsic RC-limited frequency given by equation (1) for the $\sim 1 \mu\text{m}$ scale device shown in Fig. 3b is in the THz regime.

As the RC-limited frequency is so high, the intrinsic fundamental limit on the maximum frequency may be set by the time constants determined by the microscopic switching mechanism between the low- and high-resistance states. The voltage or current driven switching could result from the destruction of the Mott insulating state in the individual NC-CDW domains while leaving the lattice in the NC-CDW state (process a), or it could be accompanied by a reconstruction of the lattice from the NC-CDW state to the I-CDW state (process b). Process a is a purely electronic process and is therefore extremely fast. The speed of process b is governed by the time constant associated with the relaxation of the lattice. Available femtosecond ARPES data at room temperature suggest a time constant of 700 fs, which provides an upper frequency limit on the order of 1 THz (ref. 29). A lower frequency limit would result from a thermally induced switching mechanism whereby the current heats up the device sufficiently to induce the NC-CDW to IC-CDW transition. Such a mechanism is considered to be the most likely scenario in VO₂ devices^{30,31}. At a fixed temperature, the NC-CDW to IC-CDW transition in samples of different lengths occurs at approximately constant electric fields and constant current densities (and therefore constant power densities). This indicates that thermal effects also play a role in the switching in our device. A study of V₂O₃ devices found that thermally induced switching could occur at subnanosecond timescales, resulting in GHz frequencies³². In either case, VCOs operating even at lower frequencies (for example, MHz in radio) are important devices with various applications³³. Compact VCOs can also be used as elements in oscillator-based pattern-recognition neural networks^{34,35}.

The physical principles behind the operation of 1T-TaS₂ VCOs are different from those in the MITs used in VO₂ devices^{36–42}. The transition in VO₂ is from the low-temperature monoclinic structure to the rutile structure^{43–45}. The origin of the transition (Peierls versus Mott–Hubbard types) is under debate^{43–45}. The transition in our 1T-TaS₂ devices is from NC-CDW to IC-CDW⁴⁶. As VO₂ is a 3D material, the attempts to deposit it as thin films with small thicknesses ($H < 10 \text{ nm}$) resulted in excessive strain and correspondingly reduced the phase transition temperature^{47,48}. The phase transition from NC-CDW to IC-CDW in 6–9-nm-thin films of 1T-TaS₂ is almost the same as it is in the bulk ($\sim 350 \text{ K}$), well above room temperature¹⁰.

Methods

Methods and any associated references are available in the [online version of the paper](#).

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Author contributions

A.A.B. coordinated the project and contributed to the experimental data analysis; R.K.L. led the theoretical analysis; T.T.S. supervised the material synthesis and contributed to the characterization of the materials; G.L. designed, fabricated and tested the devices and analysed the experimental data; T.R.P. synthesized TaS₂ crystals; B.D. conducted computer simulations. All authors contributed to writing the manuscript.

Additional information

Supplementary information is available in the [online version of the paper](#). Reprints and permissions information is available online at www.nature.com/reprints. Correspondence and requests for materials should be addressed to A.A.B.

Competing financial interests

The authors declare no competing financial interests.

Methods

1T-TaS₂ crystal growth. TaS₂ crystals were grown by an adapted chemical vapour transport method, where the 1T polytype can be isolated by fast quenching from the crystal growth temperature (875–975 °C; ref. 49). Elemental tantalum (20.4 mmol, Sigma-Aldrich 99.99% purity) and sulfur (41.1 mmol, J.T. Baker >99.9% purity) were ground with mortar and pestle and placed in a 17.8 × 1.0 cm fused quartz ampoule (cleaned by soaking overnight in nitric acid followed by annealing at 900 °C for 24 h). Elemental iodine (J.T. Baker 99.9% purity) was added (~88 mg for an ampoule with a volume of ~14.0 cm³). The ampoule was evacuated and backfilled three times with argon, with cooling to mitigate I₂ sublimation. Next the ampoule was flame-sealed and heated in a two-zone tube furnace at 10 °C min⁻¹ to 975 °C (the hot zone) and 875 °C (the cool zone). These temperatures were held for one week. Then the ampoule was removed from the hot furnace and immediately quenched in a water–ice–NaCl bath. The resulting golden crystals, shown in Supplementary Fig. 1, were characterized as detailed below. The as-grown crystals and their atomic

structure are shown in Supplementary Fig. 1. The structure and phase purity were verified by powder X-ray diffraction (shown in Supplementary Fig. 2) and the stoichiometry was confirmed with energy dispersive spectroscopy and electron probe microanalysis (shown in Supplementary Fig. 3 and Supplementary Table 1).

Electrical characteristics of the 1T-TaS₂ devices. All *I*–*V* characteristics were measured in the Lakeshore cryogenic probe station TTPX with a semiconductor analyser (Agilent B1500). The oscillator of the waveform is collected by an oscilloscope (LeCroy WaveAce1012) whereas the d.c. voltage supply of the circuit is biased with a BK Precision 1787B.

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