Open access • Proceedings Article • DOI:10.1109/SBCCI.2018.8533233

# A Charge-Sharing Bandpass Filter Topology with Boosted Q-Factor in 40-NM CMOS



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**Published on:** 01 Aug 2018 - Symposium on Integrated Circuits and Systems Design

**Topics:** Band-pass filter, Electronic filter, Bandwidth (signal processing), Q factor and Intermediate frequency

# A Charge-Sharing Bandpass Filter Topology with Boosted Q-Factor in 40-nm CMOS

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***Abstract*—This paper presents a detailed design of an innovative discrete-time charge-sharing bandpass filter with a feedback technique for boosting its quality factor. The design is implemented in 40-nm bulk CMOS, and it was integrated in silicon as part of a complete super-heterodyne receiver. In the proposed topology, cross-connected transconductors are used to boost the quality factor. The resulting selectivity of the complex filter is equivalent to a higher order filter but without the power consumption burden. The passive filter is fully programmable, which allows for an intermediate frequency selection in the range of 20 MHz to 100 MHz. The consequent variable bandwidth enables its use for either narrowband or wideband applications. The passive filter, with transconductance amplification and clock generation, occupies an area of 0.24 x 0.28 mm$^2$ with a power consumption of 8 mW when operating with a 500 MHz sampling frequency.**

***Index Terms*—charge-sharing bandpass filter, discrete-time, noise, switched-capacitor.**

## I. Introduction

For many years, the basic choice of a receiver (RX) architecture has been direct conversion (DC) or a low-intermediate-frequency (IF) at most. The main reason for this preference has been usually the easier integration of the low-pass filters and the lack of image in the DC implementation, or the easier baseband filtering in the case of the low-IF implementation. Nevertheless, complex strategies were sometimes required to overcome the typical issues of 2$^{\text{nd}}$ order non-linearity, flicker noise and DC offsets [1]–[3].

Recently, the super-heterodyne architecture has also become an option with the advent of high-Q bandpass filter (BPF) integration, avoiding the large external filters required to solve the image proplem in the past. The introduction of N-path filters in the RF front-end led the way to the start of this new revived interest in super-heterodyne receivers [4]. The N-path "complex" implementation can successively attenuate the RF image and, most important, it benefits directly from technology scaling, as it is implemented only with MOS switches and capacitors, all controlled by digital full-swing clocks. The main drawback presented by this solution are the filter replicas at the sampling rate as a consequence of the discrete-time (DT) nature of the filter, which are then folded back to the band of interest. This "replica" folding issue was solved by the full-rate charge-sharing (CS) BPF introduced in [5]. In [6], an enhancement to the full-rate CS-BPF was introduced, which in turn allows for a sharper filtering without additional power consumption burden.

In this paper, the modified CS-BPF which was tested in [6] has its CMOS design presented in detail. Its main advantages over the traditional CS-BPF approach are discussed, and the small noise impact of the circuit modification is carefully analysed. Section II reviews and generalizes the CS-BPF DT architecture. The modified CS-BPF and the noise analysis are presented in Section III. The filter architecture, simulation results and receiver measurements are presented in Sections IV and V, and the paper conclusions are drawn in Section VI.

## II. Charge-sharing bandpass filter

The basic charge-sharing bandpass filter (CS-BPF) is synthesized from the 4$^{\text{th}}$-order Infinite Impulse Response (IIR) lowpass filter (LPF) [7]. To better understand this process, we start by the well-known first order IIR LPF with current input [8], shown in fig. 1(a). In this circuit, an input charge packet is stored in a history capacitor ($C_H$), and on phase $\phi_1$, partially transferred to a previously discharged rotating capacitor ($C_R$), acting as a lossy component. The order of the IIR LPF can be easily increased by adding more $C_H$ capacitors to share the charge stored in $C_R$ during subsequent phases, $\phi_1$, $\phi_2$ and so forth [8]. Hence, as shown in fig. 1(b), a 4$^{\text{th}}$-order IIR LPF is created by sharing the charge of $C_R$ with three other $C_H$ [9].

The basic CS-BPF is created by connecting four inputs with increasing 90-degree phase shifts, to the 4$^{\text{th}}$-order IIR LPF, as shown in fig. 1(c). Therefore, each $C_H$ stores the input charge of a different input, which is sampled by $C_R$ on one phase and shared with the next $C_H$ on the next phase [7]. In order to create a full-rate 1$^{\text{st}}$-order CS-BPF, four basic cells of the CS-BPF are connected, as shown in fig. 1(d) [7], with the four 25% duty-cycle clocks phases in fig. 1(e). In [10], a generic CS-BPF has been presented and named as M/N-phase CS-BPF, where M is the number of inputs and N the number of phases. This nomenclature will be used hereafter.

Based on the schematic of the 4/4-phase CS-BPF presented in fig. 1(d), the transfer function is given by [7]

$$H(z) = \frac{k}{(1 - az^{-1}) - e^{j\frac{\pi}{2}}(1 - a)z^{-1}}, \tag{1}$$

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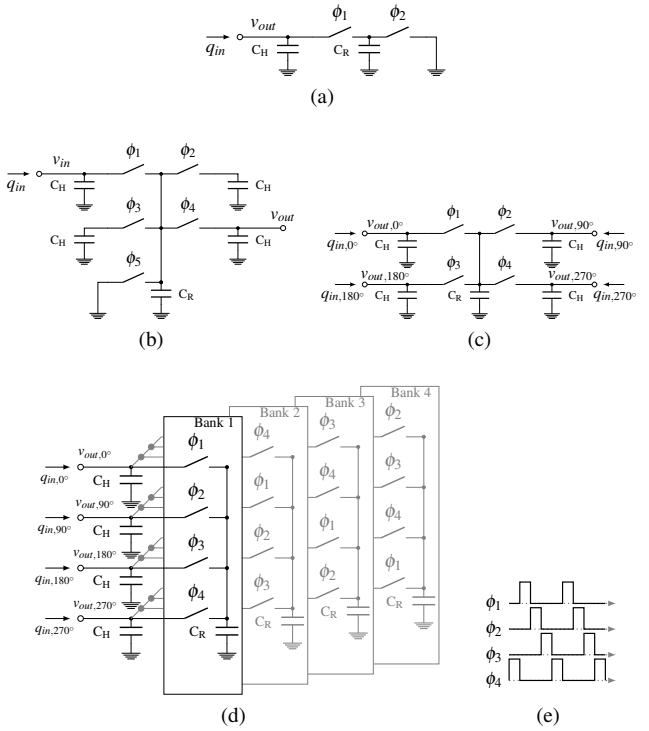



Fig. 1. (a) The 1st-order and (b) 4th order IIR LPF. (c) The CS-BPF basic cell and (d) 1st-order full-rate CS-BPF. (e) The 25% clock, which drives the 4/4-phase CS-BPF filter.

where $k = 1/(C_R + C_H)$ and $a = C_H/(C_H + C_R)$. The filter Q-factor obtained from (1) is ideally 0.5 and can be easily improved in two different ways: by increasing the number of inputs (fig. 2(a)), or by adding lowpass poles (fig. 2(b)). To include these variations, a more general CS-BPF transfer function is given by (2).

$$H(z) = \frac{k\left[(1-a)\,z^{-1}\right]^{N/M-1}}{(1-az^{-1})^{N/M} - e^{j\frac{2\pi}{M}}\left[(1-a)\,z^{-1}\right]^{N/M}}. \quad (2)$$

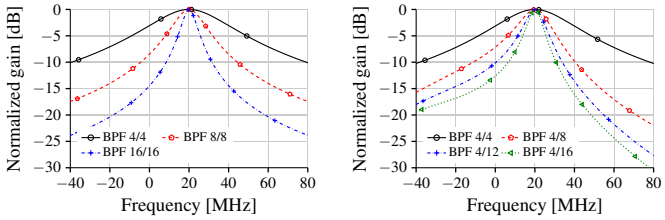



Fig. 2. (a) Filtering characteristic of 4/4-phase, 8/8-phase, and 16/16-phase CS-BPF;(b) Filtering characteristic of 4/4-phase, 4/8-phase, 4/12-phase, and 4/16-phase CS-BPF.

Based on (2), the transfer functions of two Q-factor enhancing alternatives are presented in fig. 2(a): 8/8-phase, 16/16-phase, and in fig. 2(b): 4/8-phase, 4/12-phase, and 4/16-phase CS-BPF. In comparison to the 4/4-phase CS-BPF, the 8/8-phase CS-BPF has a better filtering characteristic but the attenuation far from the central frequency is limited. This limitation is not presented by higher order filters like the 4/8, 4/12, and so forth, which can provide strong attenuation both close and far from the central frequency (fig. 2(b)). The basic cell implementations of the 8/8-phase and the 4/8-phase CS-BPF alternatives are presented in fig. 3(a) [10] and fig. 3(b) [11]. To obtain the full-rate equivalents, 8 $C_R$s are placed in parallel, in a similar fashion to fig. 1(d).

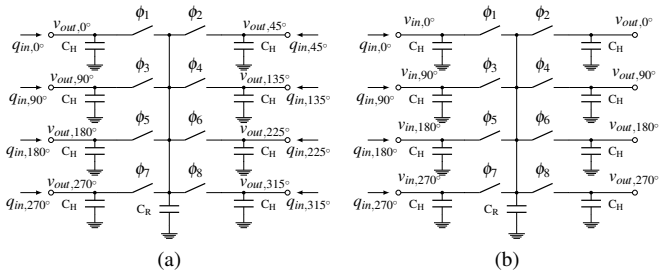



Fig. 3. (a) The schematic of a 8/8-phase CS-BPF and (b) a 4/8-phase CS-BPF.

Regardless of the number of inputs and the order, the central frequency of the CS-BPF is solely controlled by the ratio of the capacitors $C_H$ and $C_R$. This is the main advantage of the CS-BPF over the other bandpass filters since the capacitors in modern CMOS technologies are very robust to mismatch which plagues traditional topologies based on Gm-C, active-RC, or biquad. The CS-BPF central frequency is given by [10]

$$f_c = \frac{f_s}{2\pi} arctan\left[\frac{(1-a)sin(2\pi/N)}{a+(1-a)cos(2\pi/N)}\right]. \quad (3)$$

## III. Modified Charge-Sharing Bandpass Filter

Even though both methodologies are very effective to increase the Q-factor of the CS-BPF, they also increase the overall number of switches, the number of clock buffers, and consequently the power consumption. For instance, considering only the number of switches, the power consumption of the 4/8-phase BPF is 4x higher than the 4/4-phase BPF. Also, the switches of the 4/8-phase BPF work at a 2x-higher sampling rate. Hence, each of the clock generation circuits is going to consume 2x more power. Additionally, two other issues might arise from the increase of the filter order and the number of inputs. Firstly, in both cases, the sampling frequency of the CS-BPF increases. Hence, the switches must be proportionally faster, or the filter performance will decrease. Secondly, as the order of the CS-BPF increases, a secondary peak appears. This second peak is barely noticeable on the 4/8-phase CS-BPF transfer function (TF), but it already affects the symmetry of the magnitude TF. Due to the second peak, the image attenuation improves only by 5 dB from the 4/8-phase to the 4/16-phase BPF [6]. Based on these points, we conclude that increasing the order of the filter beyond two (e.g., 4/8-phase BPF) is hardly worth the cost of complexity and power consumption.

Another possibility to enhance the Q-factor is by adding a pair of cross-connected transconductors at both the in-phase (I) and quadrature (Q) inputs of the filter. In fact, this cross-connected topology works as a negative impedance. Fig. 4 shows the schematic of a 4/8 CS-BPF modified using this

negative impedance. By improving the Q-factor, both the image attenuation and the filtering of out-of-band blockers are improved. Nevertheless, since the I and Q paths are still independent, the I/Q mismatch remains affected mainly by the clock generation [6], [12].

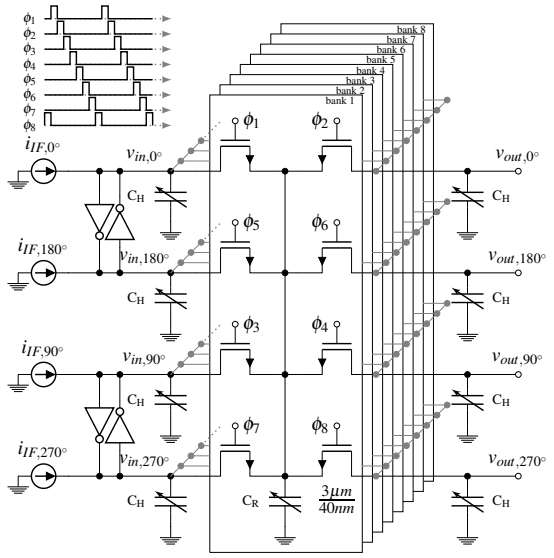



Fig. 4. Modified 4/8 phase CS BPF Schematics.

### A. Implementation of the modified 4/8-phase CS-BPF

The negative impedance was implemented with inverters as presented in fig. 4. Based on this schematic, the time-domain input and output voltages of the modified 4/8-phase BPF at $t = nT_S$ are respectively

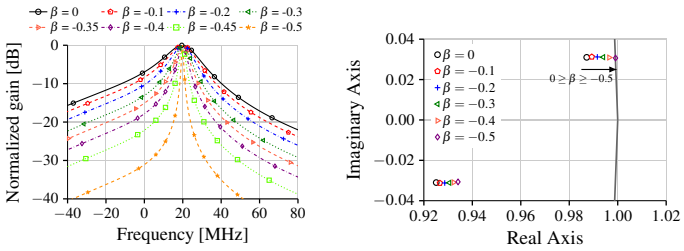
$$v_{in,i}[n] = av_{in,i}[n-1] + (1-a)v_{out,i-90°}[n-1] + kq_i[n] + \beta(1-a)v_{in,i-180°}[n], \quad (4)$$

$$v_{out,i}[n] = av_{out,i}[n-1] + (1-a)v_{in,i}[n-1], \quad (5)$$

where $i \in \{0°, 90°, 180°, 270°\}$ and represents the phase of the input or output, and $\beta$ is the gain of the feedback loop used to implement the negative impedance. By converting (4) and (5) from the time-domain to the z-domain, the transfer function below is obtained.

$$H(z) = \frac{k\,(1-a)\,z^{-1}}{(1-az^{-1})^2\left(1+\frac{1-a}{1-az^{-1}}\beta\right) - j\,(1-a)^2\,z^{-2}}, \quad (6)$$

Fig. 5(a) shows the plotted transfer function of the modified 4/8-phase CS-BPF. By setting $\beta$ to -0.5, according to the figure, an attenuation higher than 35 dB at the image frequency would be obtained, which is even better than the 4/16-phase CS-BPF case. However, $|\beta| < 0.5$ should be adopted to ensure stability [6], and the CS-BPF would operate close to the oscillation condition. Fig. 5(b) presents a zoomed version of the pole representation of (6) as $\beta$ is varied, showing that one of the poles is crossing the unit circle at $\beta = -0.5$.




(a) (b)

Fig. 5. (a) Modified 4/8-phase CS BPF transfer function;(b) Pole-zero mapping of the modified 4/8-phase CS BPF TF (6).

### B. Noise analysis of the modified charge-sharing bandpass filter

In addition to stability, noise is a concern when the negative impedance is added to the filter. Based on the noise analysis of the 4/4-phase CS-BPF presented in [7], the noise contribution of the modified 4/8-phase CS-BPF is presented hereafter.

The noise sources of the filter are the switches and the inverters of the negative impedance, with thermal noise power spectral density (PSD) given, respectively, by (7) and (8).

$$S_{sw}(f) = 4kTR_{ON} \quad (7)$$

$$S_{inv}(f) = 4kT\gamma/G_m, \quad (8)$$

where k is the Boltzmann constant, T is the absolute temperature, $R_{ON}$ is the resistance when the switch is closed, $\gamma$ is the noise parameter, and $G_m$ is the overall transconductance of the inverter. However, due to the sampling process, the noise from frequencies above $f_s/2$ is folded to the interval 0-to-$f_s/2$. Hence, after taking the folding into consideration, the sampled noise PSD of the switch and the inverter are given by (9) and (10), respectively [13].

$$S_{sw,S/H}(f) = \frac{2kT}{C_R f_s}, \quad 0 \le f \le f_s/2 \quad (9)$$

$$S_{inv,S/H}(f) = \frac{2kT\gamma}{G_m C_R f_s R_{ON}}. \quad 0 \le f \le f_s/2 \quad (10)$$

The sampled noise PSDs will be considered as the noise sources in the following analysis.

Fig. 6 shows the simplified noise model, which considers no input charge packets. The purpose of this analysis is to compare the noise of the 4/8-phase CS-BPF with and without the addition of the negative impedance. First, the noise contribution of each noise source to each output is calculated. In fact, since the circuit is symmetrical, the noise at all outputs are equal, and we need to only compute for one output.

The noise sources are uncorrelated, so superposition can be used to compute the contribution of each source to the output noise. Therefore, to calculate the output noise due to $v_{n1}$, the other noise sources are set to zero. The time-domain noise of the first output and input at $t = nT_s$ is given by

$$v_{out,0°}[n] = av_{out,0°}[n-1] + bv_{in,0°}[n-1] - bv_{n1}[n-1], \quad (11)$$

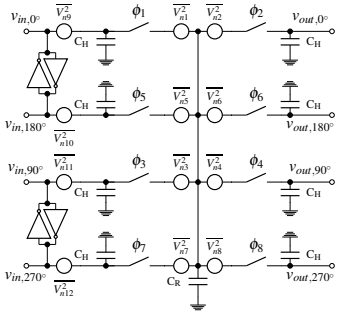



Fig. 6. Noise sources of the modified 4/8-phase CS-BPF.

$$v_{in,0^\circ}[n] = av_{in,0^\circ}[n-1] + bv_{out,270^\circ}[n-1] + \beta bv_{in,180^\circ}[n] + bv_{n1}[n], \quad (12)$$

where $b = 1 - a$, and $v_{n1} = \sqrt{\overline{V_{n1}^2}}$. The time-domain noise equations of the other three inputs and outputs are

$$v_{out,i}[n] = av_{out,i}[n-1] + bv_{in,i}[n-1], \quad (13)$$

$$v_{in,i}[n] = av_{in,i}[n-1] + bv_{out,i-90^\circ}[n-1] + \beta bv_{in,i-180^\circ}[n], \quad (14)$$

where $i \in \{90^\circ, 180^\circ, 270^\circ\}$. By converting (11) - (14) from the time-domain to the z-domain, the noise transfer function of $v_{n1}$ to each output is

$$H_1 = \frac{\left(1-az^{-1}\right)^7 bz^{-1} - \left(1-az^{-1}\right)^6 b^2 z^{-1} + A_1}{-\left(1-az^{-1}\right)^8 + b^8 z^{-8} + B_1}, \quad (15)$$

$$H_2 = \frac{\left(1-az^{-1}\right)^5 b^3 z^{-3} - \left(1-az^{-1}\right)^4 b^4 z^{-3} + A_2}{-\left(1-az^{-1}\right)^8 + b^8 z^{-8} + B_1}, \quad (16)$$

$$H_3 = \frac{\left(1-az^{-1}\right)^3 b^5 z^{-5} - \left(1-az^{-1}\right)^2 b^6 z^{-5} + A_3}{-\left(1-az^{-1}\right)^8 + b^8 z^{-8} + B_1}, \quad (17)$$

$$H_4 = \frac{\left(1-az^{-1}\right) b^7 z^{-7} - b^8 z^{-7} + A_4}{-\left(1-az^{-1}\right)^8 + b^8 z^{-8} + B_1}, \quad (18)$$

where $H_1$, $H_2$, $H_3$, and $H_4$ are the noise TFs to $v_{out,0^\circ}$, $v_{out,90^\circ}$, $v_{out,180^\circ}$, and $v_{out,270^\circ}$, respectively. Also, the terms $A_1$, $A_2$, $A_3$, $A_4$, and $B_1$ are introduced by the negative impedance and presented below:

$$A_1 = \left[-2\left(1-az^{-1}\right)+b\right]\left[\left(1-az^{-1}\right)^4 b^3\beta^2 z^{-1} + \left(1-az^{-1}\right) b^6\beta z^{-5}\right] + \left(1-az^{-1}\right)^3 b^5\beta^4 z^{-1}, \quad (19)$$

$$A_2 = -\left(1-az^{-1}\right)^3 b^5\beta^2 z^{-3} - \left(1-az^{-1}\right)^2 b^6\beta^2 z^{-3} - b^8\beta z^{-7}, \quad (20)$$

$$A_3 = -\left(1-az^{-1}\right)^5 b^3\beta z^{-1} + \left(1-az^{-1}\right)^3 b^5\beta^3 z^{-1} + \left(1-az^{-1}\right) b^7\beta^2 z^{-5}, \quad (21)$$

$$A_4 = -\left[-\left(1-az^{-1}\right)^2 - 2\left(1-az^{-1}\right)b - \beta^2 b^2\right] \left(1-az^{-1}\right)^2 \beta b^4 z^{-3}, \quad (22)$$

$$B_1 = 2\left(1-az^{-1}\right)^6 b^2\beta^2 - \left(1-az^{-1}\right)^4 b^4\beta^4 + 4\left(1-az^{-1}\right)^3 b^5\beta z^{-4}. \quad (23)$$

Hence, if these terms are considered zero, we have the noise TF of the original 4/8-phase CS-BPF.

Since the filter is symmetrical, the TFs (15) - (18) are the same for the sources $\overline{V_{n1}^2}$, $\overline{V_{n3}^2}$, $\overline{V_{n5}^2}$, and $\overline{V_{n7}^2}$. They will also be the same for the noise sources $\overline{V_{n2}^2}$, $\overline{V_{n4}^2}$, $\overline{V_{n6}^2}$, and $\overline{V_{n8}^2}$, but with an opposite sign. Finally, repeating the previous methodology, the noise transfer function of $v_{n9}$ (i.e. one inverter of the negative impedance) to each output is

$$H_5 = \frac{\left(1-az^{-1}\right)^6 b^2 z^{-1} + A_5}{\left(1-az^{-1}\right)^8 - b^8 z^{-8} + B_2}, \quad (24)$$

$$H_6 = \frac{\left(1-az^{-1}\right)^4 b^4 z^{-3} + \left(1-az^{-1}\right)^2 b^6\beta^2 z^{-3}}{\left(1-az^{-1}\right)^8 - b^8 z^{-8} + B_2}, \quad (25)$$

$$H_7 = \frac{\left(1-az^{-1}\right)^2 b^6 z^{-5} + A_6}{\left(1-az^{-1}\right)^8 - b^8 z^{-8} + B_2}, \quad (26)$$

$$H_8 = \frac{2\left(1-az^{-1}\right)^3 \beta b^5 z^{-3} + b^8 z^{-7}}{\left(1-az^{-1}\right)^8 - b^8 z^{-8} + B_2}. \quad (27)$$

where the terms $A_5$, $A_6$, and $B_2$ are

$$A_5 = -\left(1-az^{-1}\right)^4 \beta^2 b^4 z^{-1} - \left(1-az^{-1}\right)\beta b^7 z^{-5}, \quad (28)$$

$$A_6 = \beta\left(1-az^{-1}\right)^5 b^3 z^{-1} - \beta^3\left(1-az^{-1}\right)^3 b^5 z^{-1}, \quad (29)$$

$$B_2 = \left[-2\left(1-az^{-1}\right)^3\beta + \left(1-az^{-1}\right) b^2\beta^3 - 4b^3 z^{-4}\right] \times \left(1-az^{-1}\right)^3 \beta b^2. \quad (30)$$

Similary to (15) - (18), the TFs (24) - (27) are the same for the sources $\overline{V_{n9}^2}$, $\overline{V_{n10}^2}$, $\overline{V_{n11}^2}$, and $\overline{V_{n12}^2}$ because the filter is symmetrical.

The differential discrete-time output noise is composed by noise components of all these sources as shown below:

$$\begin{aligned}\overline{V_{on}^2} = {} & (H_1-H_3)^2\overline{V_{n1}^2} + (H_4-H_2)^2\overline{V_{n3}^2} + (H_3-H_1)^2\overline{V_{n5}^2} \\ & + (H_2-H_4)^2\overline{V_{n7}^2} + (H_3-H_1)^2\overline{V_{n2}^2} + (H_2-H_4)^2\overline{V_{n4}^2} \\ & + (H_1-H_2)^2\overline{V_{n6}^2} + (H_4-H_2)^2\overline{V_{n8}^2} + (H_5-H_7)^2\overline{V_{n9}^2} \\ & + (H_8-H_6)^2\overline{V_{n10}^2} + (H_7-H_5)^2\overline{V_{n11}^2} \\ & + (H_6-H_8)^2\overline{V_{n12}^2}. \end{aligned} \quad (31)$$

Since the 8 switches are equal and the 4 inverters are also equal, the previous equation can be further simplified to

$$\begin{aligned}\overline{V_{on}^2} = {} & 4\left[(H_1-H_3)^2 + (H_4-H_2)^2\right]\overline{V_{n1}^2} \\ & + 2\left[(H_5-H_7)^2 + (H_5-H_7)^2\right]\overline{V_{n9}^2}. \end{aligned} \quad (32)$$

After that, by plotting (32) and the $\overline{V_{on}^2}$ of the original 4/8-phase CS-BPF, we can evaluate how the negative impedance affects the noise of the filter. In order to perform this comparison, a 4/8-phase CS-BPF with $C_R = 4$ pF, $C_H = 19$ pF, and $f_s = 1$ GHz, and a negative impedance with $\beta = -0.2$ are considered. Fig. 7 shows the output noise of the filter with and without the negative impedance. Additionally, the dashed and dashed-dotted lines show the composition of the filter output noise with negative impedance, i.e., the noise contribution

of the switches and inverters. Since the negative impedance enhances the gain of the filter, a slight reduction of the noise is observed, and a small impact in the overall RX noise figure is expected.

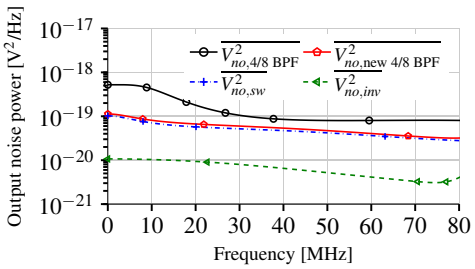



Fig. 7. The output noise PSD calculation of the 4/8-phase BPF with and without negative impedance are presented with solid lines. Dashed and dashed-dotted lines show the output noise of the switches and inverters of the modified 4/8-phase BPF.

## IV. Circuit Implementation

The modified 4/8-phase CS-BPF was implemented and measured as the second filtering stage of a complete receiver presented in fig. 8 [6].

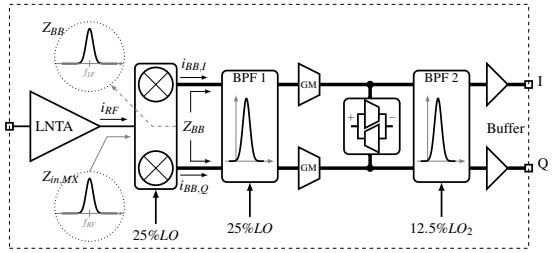



Fig. 8. Simplified block diagram of the complete implemented receiver.

The receiver in fig. 8 is composed of two basic stages: a RF front-end and a intermediate frequency (IF) filtering stage.

The RF front-end is composed of wideband LNTA, 25% duty-cycle sampling mixer, 4/4 full-rate CS-BPF which operates at the mixer sampling rate, and clock generation circuits. The front-end is a super-heterodyne architecture covering the frequency range from 500 MHz to 4 GHz, with variable intermediate frequency (IF) and adjustable channel pass-band. It is mainly in charge of low-noise amplification and out-of-band filtering, and was presented in detail in [6].

The second stage is composed of a basic "inverter-like" transconductor (Gm-cell) stage detailed in fig. 9 and a modified 4/8-phase CS-BPF (fig. 4) operating at a fixed 500-MHz sampling rate. The Gm-cell gives a gain of 12.8 dB when combined with the filter input resistance.

The eight 12.5% duty-cycle clock phases required by the filter are generated by the frequency divider-by-4 (fig. 10(a)). The latches presented in fig. 10(b) are implemented using tri-state inverters (fig. 10(c)) in order to achieve sharp transitions.

## V. Results

The DT filter was implemented in silicon as part of the receiver designed and fabricated in TSMC 40-nm CMOS

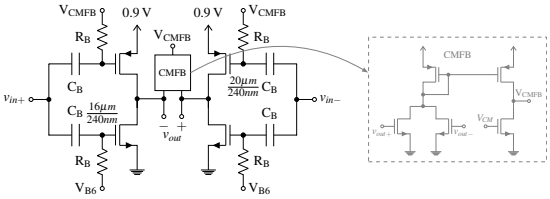
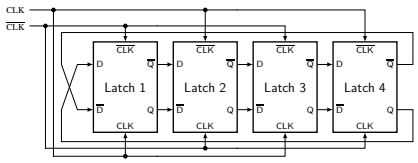
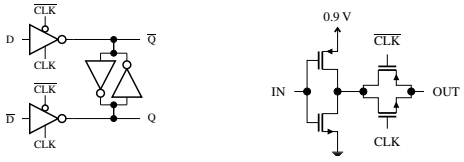



Fig. 9. "Inverter-like" transconductor.




(a)




(b) (c)

Fig. 10. (a) The divider-by-4 that generates the 12.5% non-overlaping clock, (b) the tristate latchs, and (c) the tristate circuit.

(fig. 11) [6]. The filter, the Gm-cell and the 8-phase clock generation circuit jointly occupy a slicon area of 0.24 x 0.28 mm$^2$.

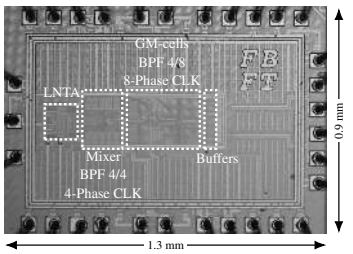



Fig. 11. Chip micrograph.

The filter implementation is detailed in fig. 4. The feedback gain $\beta$ is implemented as $G_m$ x $R_{in}$, where $G_m$ is the inverter transcondutance, and $R_{in}$ is the input resistance of the filter, $R_{in} \approx 1/f_s C_R$. $C_H$ and $C_R$ are implemented using 8-bit binary-programmed capacitor banks, ranging from 600 fF to 9 pF and 25 fF to 375 fF, respectively. According to (3), the resolution of the capacitor banks allow for center frequency programming in the range of 20 MHz to 60 MHz, which creates a variable passband characteristic due to the constant quality-factor presented by our filter design. Consequently, the filter is suitable for both wideband and narrowband applications. For instance, the 20 MHz bandwidth required by 791 - 821 MHz and 3600 - 3800 MHz LTE bands can be easily achieved by moving the IF to -40 MHz as shown in the extracted simulations (fig. 12).

Fig. 13(a) shows the improvement in selectivity of the $\beta = -0.2$ modified filter vs the traditional 4/8-phase CS-BPF approach. The feedback is used here to compensate for losses

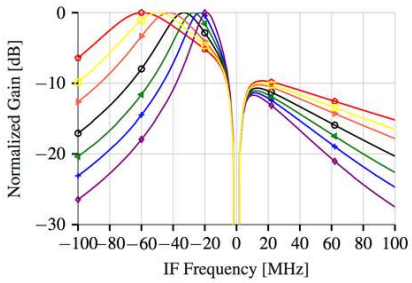
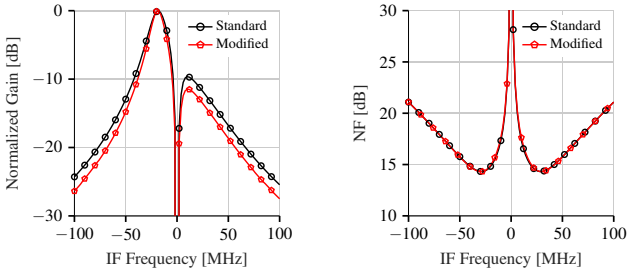



Fig. 12. Extracted simulation of the Gm and the modified 4/8-phase CS-BPF center frequency programming.

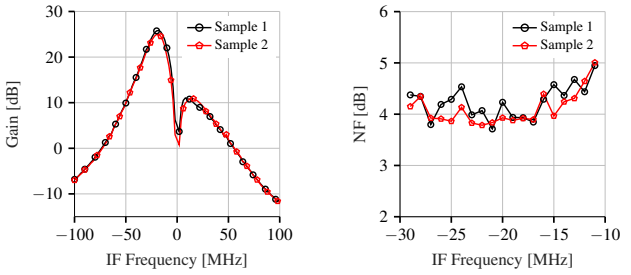
in the CS-BPF implementation, which brings the filter transfer function closer to the ideal implementation. As expected by the noise analysis, noise figure is not strongly impacted by the modification (fig. 13(b)).




(a) (b)

Fig. 13. (a) Normalized gain and (b) Noise figure of the standard and modified 4/8-phase CS-BPF with $|\beta| = 0.2$.

Fig. 14(a) and fig. 14(b) present measured gain and noise, respectively, for two chip samples of the complete receiver. Good selectivity as well as good matching characteristics are shown, resulting from the modified CS-BPF, as can be easily observed in the figure with an attenuation of about 16 dB at the image frequency. The measured power consumption of the Gm-cell with 12.8 dB of gain and the clock generation circuits operating at 500 MHz are 2.7 mW and 5.35 mW respectively, from a 0.9V power supply.




(a) (b)

Fig. 14. (a) Gain and (b) Noise Figure measurement results with 1 GHz LO frequency for the complete implemented RX.

## VI. Conclusion

This paper presented a detailed analysis of a newly modified charge-sharing bandpass filter. The discrete-time filter is fully-programmable, which allows for both intermediate frequency and passband adjustments. This flexibility makes this technique a good candidate for narrowband and wideband RF transceiver applications. The charge-sharing bandpass filter topology is modified using cross-connected transconductors at the filter inputs which enables higher selectivity without increasing complexity, noise and power consumption. The filter is implemented in 40-nm bulk CMOS and it occupies an area of 0.24 x 0.28 mm$^2$, considering the transconductor amplifier, and the clock generation circuit area altogether. The three blocks consume 8 mW from a 0.9V DC power supply.

## Acknowledgment

The authors would like to thank the CNPq, CAPES, and FAPERGS Agencies for partially funding this research.

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